Moore's Law in 2014: Implications to System-on-a-Chip (SoC) Design

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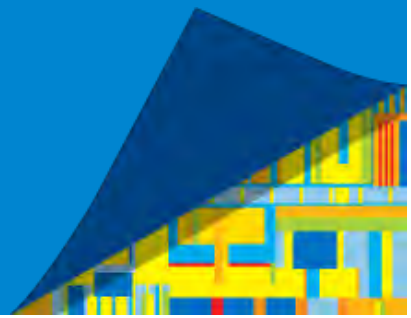
September 2014

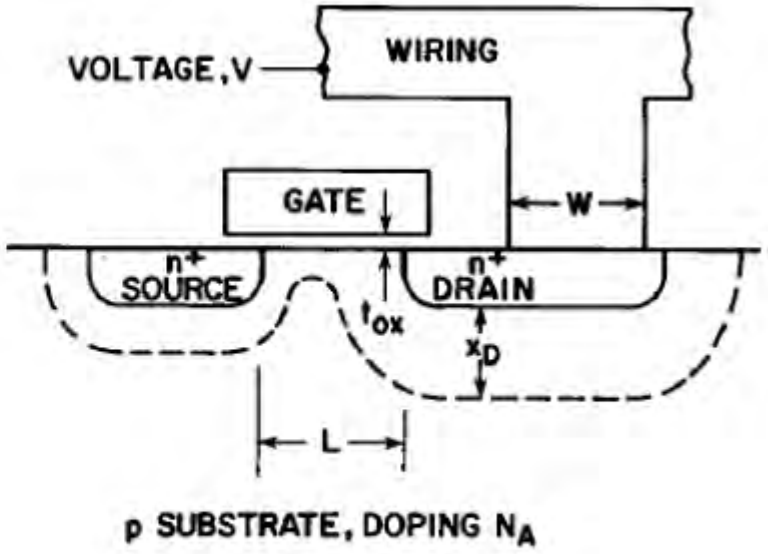


Agenda

- Silicon technology
- Introduction to SoC

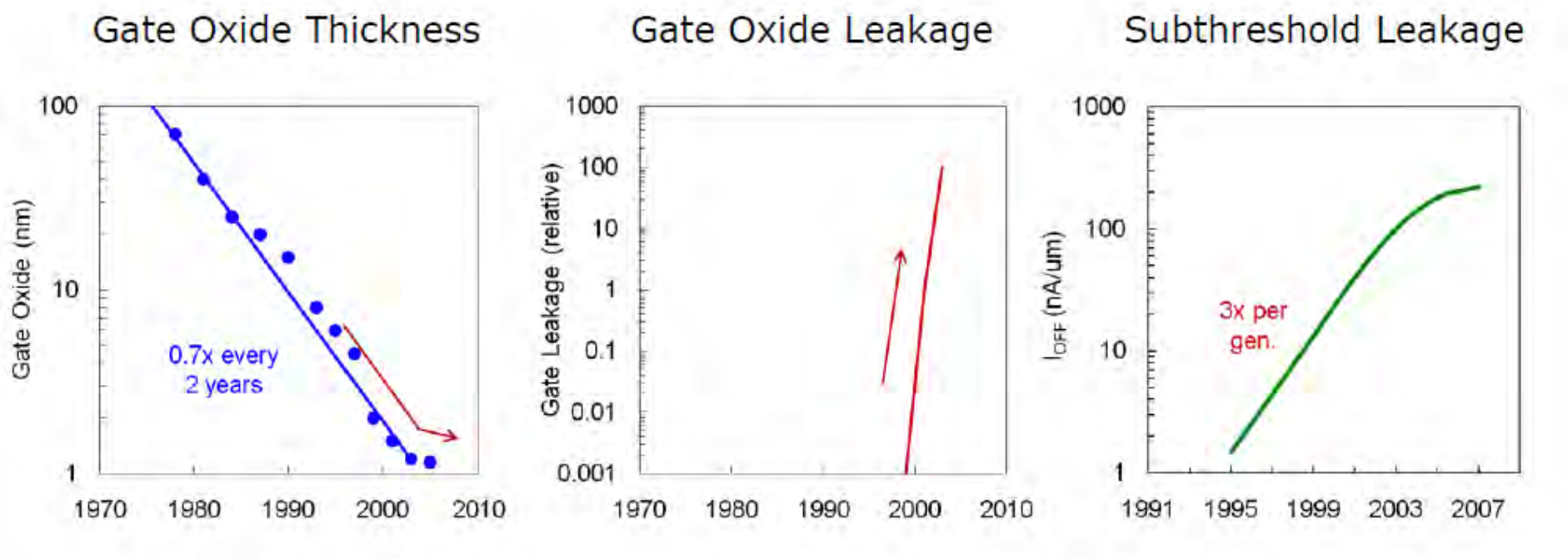
Traditional MOSFET scaling

Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	$1/\kappa$
Doping concentration *Na*	κ
Voltage *V*	$1/\kappa$
Current *I*	$1/\kappa$
Capacitance $\varepsilon A/t$	$1/\kappa$
Delay time/circuit *VC/I*	$1/\kappa$
Power dissipation/circuit *VI*	$1/\kappa^2$
Power density *VI/A*	1



R. Dennard, IEEE JSSC, 1974

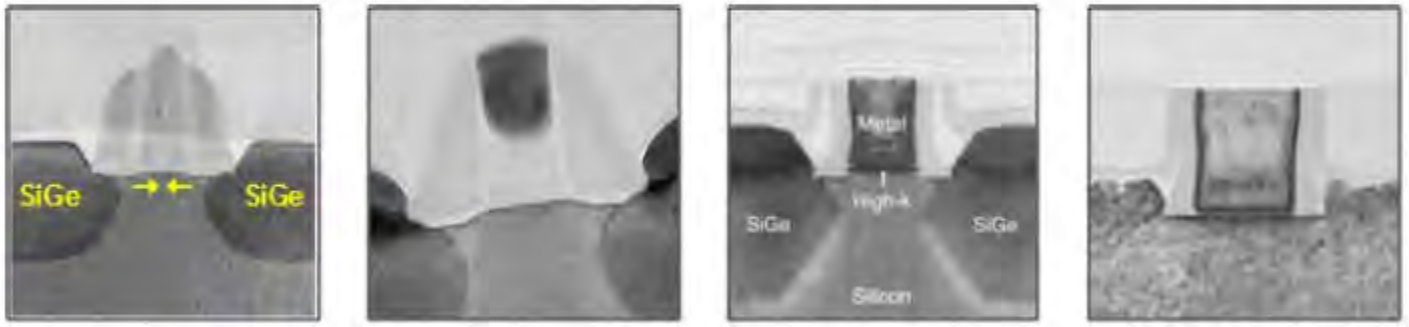
Traditional MOSFET scaling



- Traditional MOSFET scaling ran out of steam in the early 2000's
- If traditional methods don't work, then innovate!

Source: Intel

Transistor Innovation



First with Strained Silicon

2nd Generation Strained Silicon

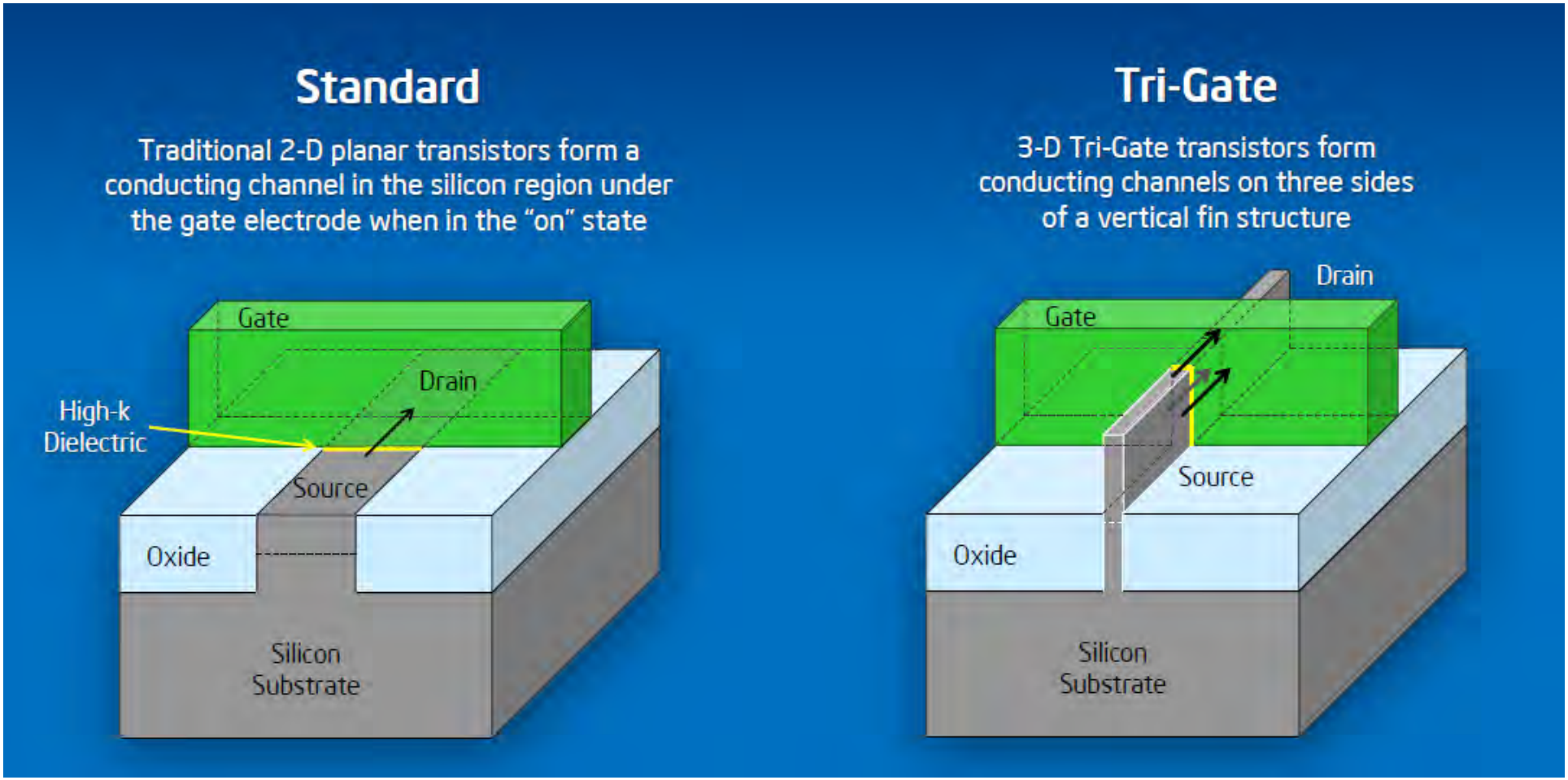
First with High-k Metal Gate

2nd Generation High-k Metal Gate

Continued innovation in transistor materials and structure are essential to continued scaling

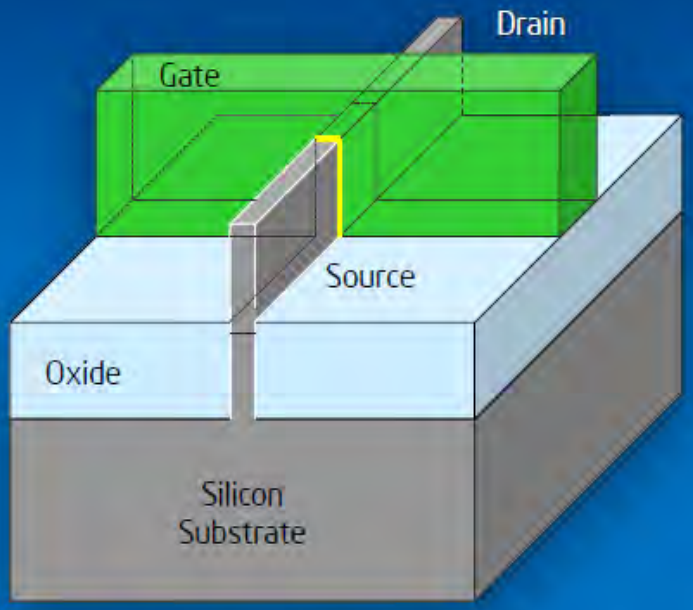
Source: Intel

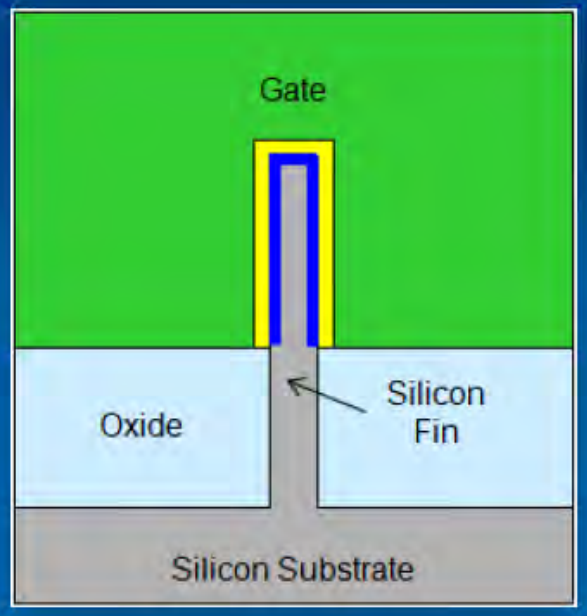
Transistors have entered the 3rd dimension



Source: Intel

Tri-gate structure enables fully depleted operation without SOI

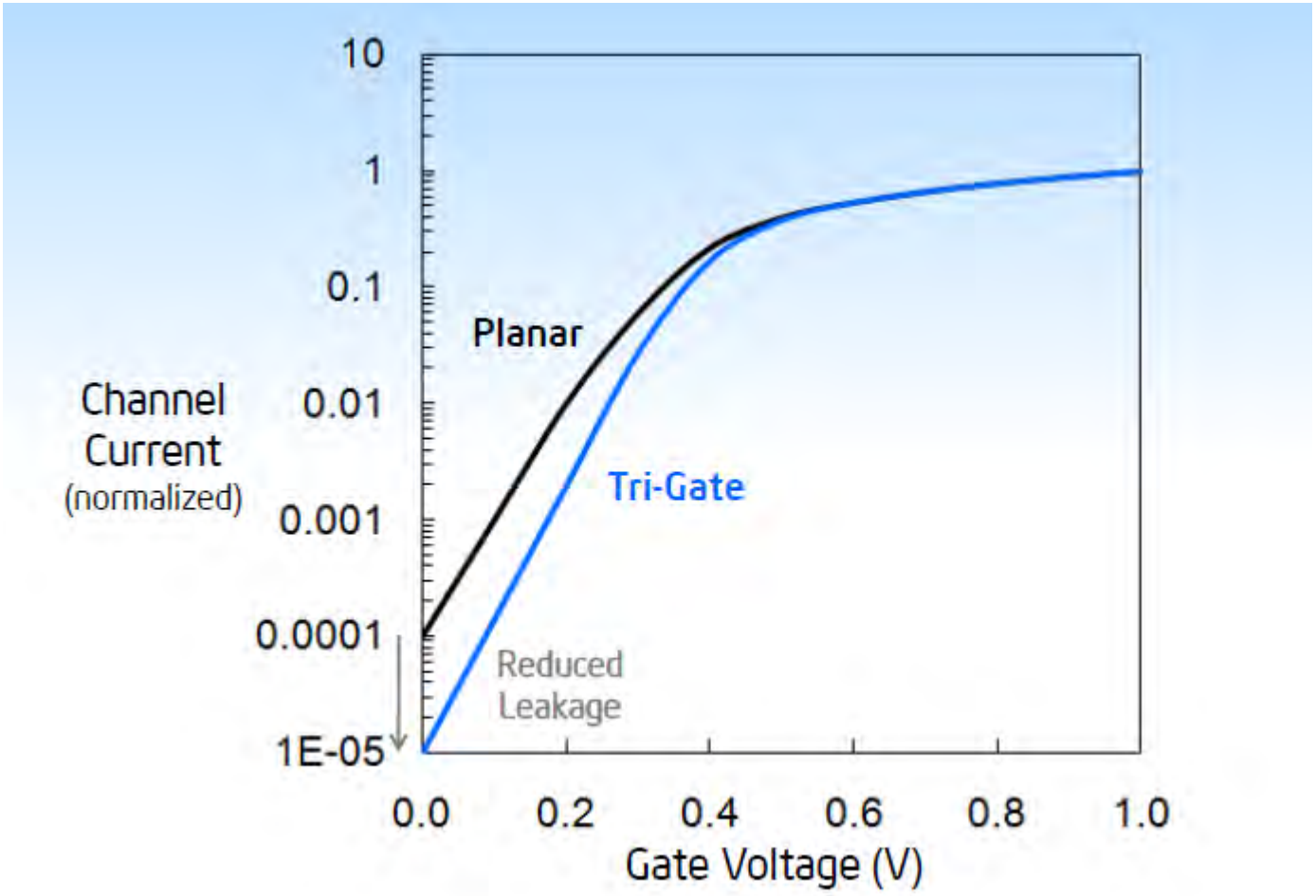




- Gate electrode controls silicon fin from three sides, providing improved sub-threshold slope
- Inversion layer area increased for higher drive current and reduced gate delay
- Process cost increased by 2-3% vs 10% for SOI wafers

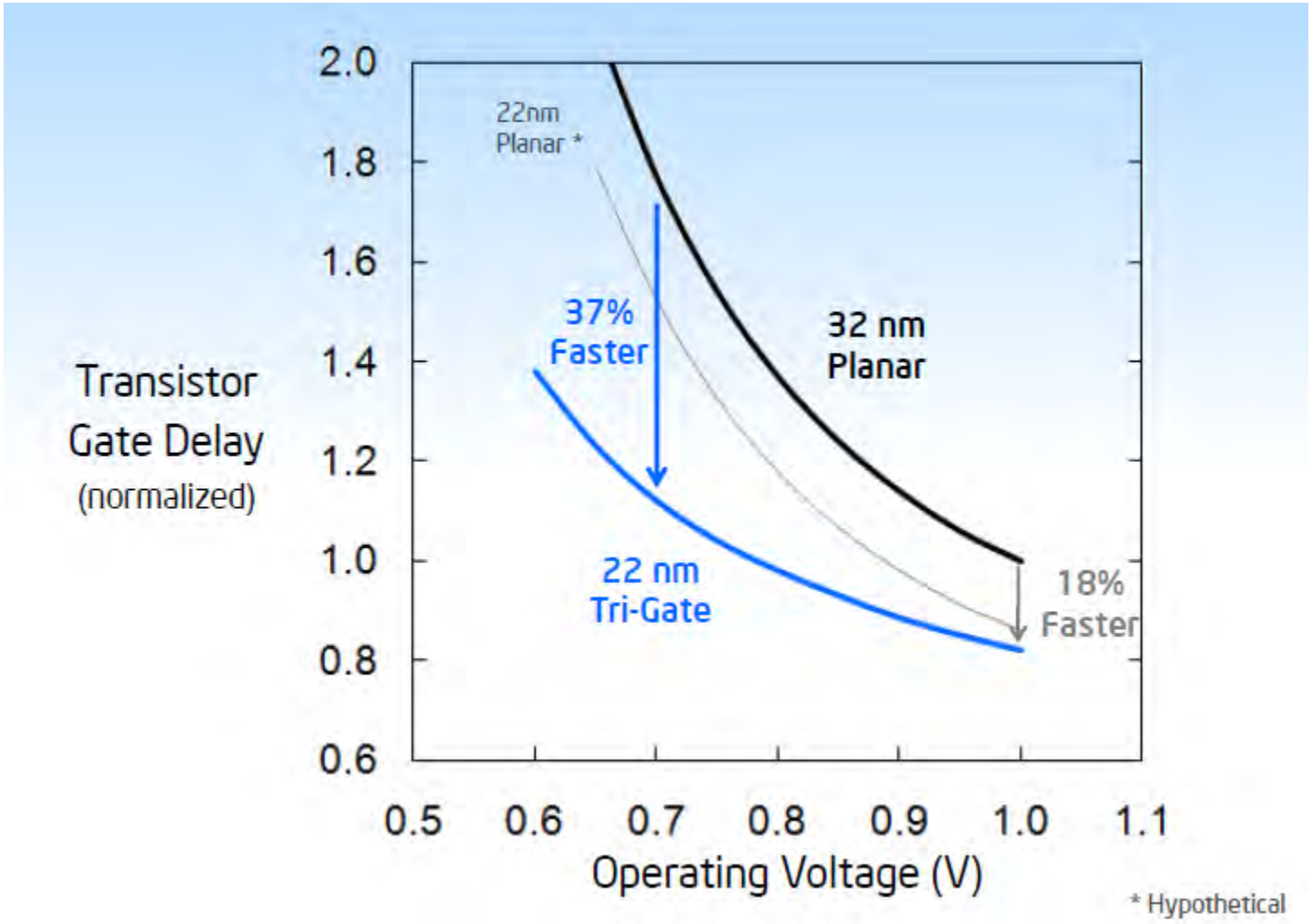
Source: Intel

Fully depleted tri-gate transistors reduce leakage current



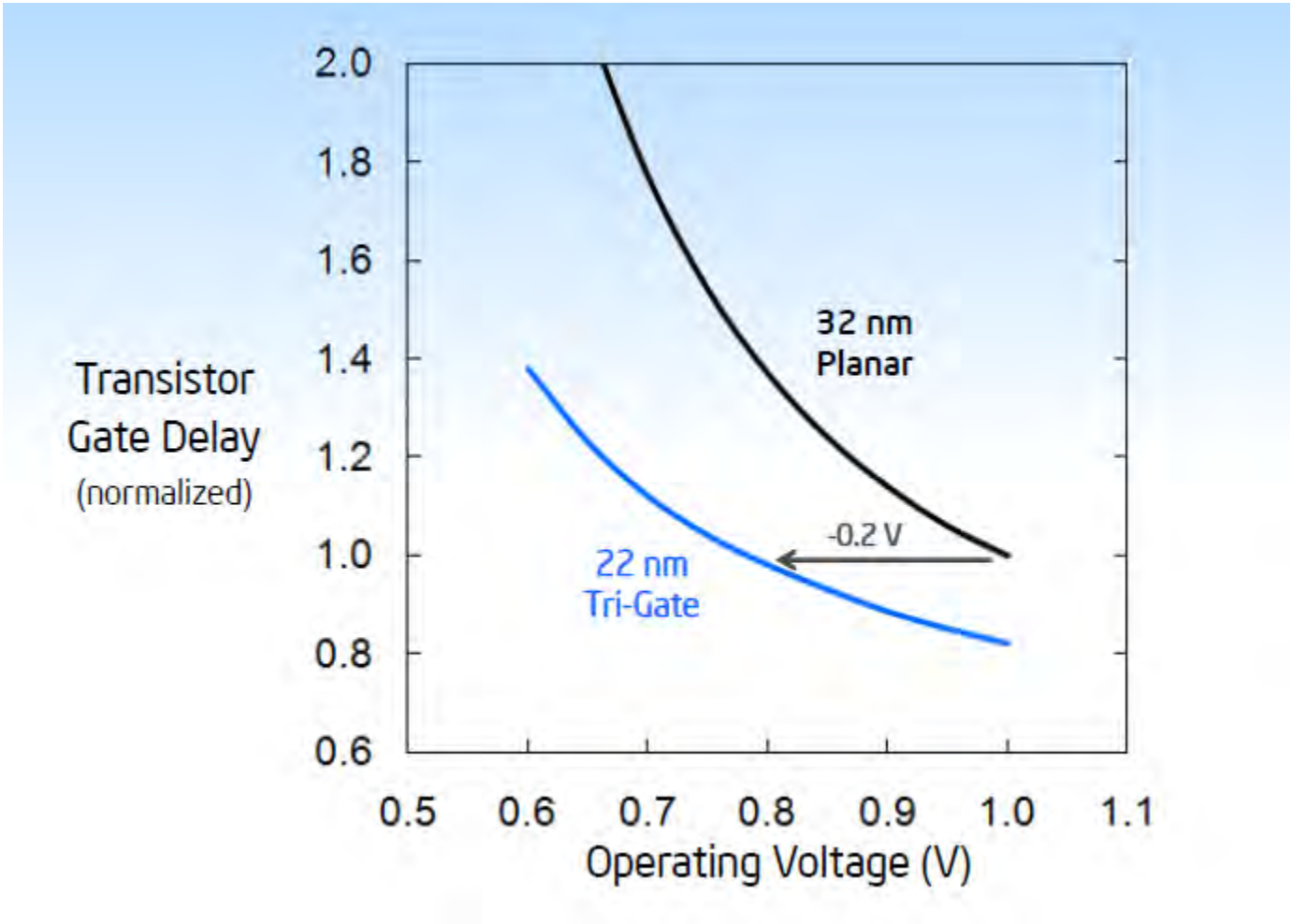
Source: Intel 2011

Improved performance at high-voltage and unprecedented performance gain at low-voltage



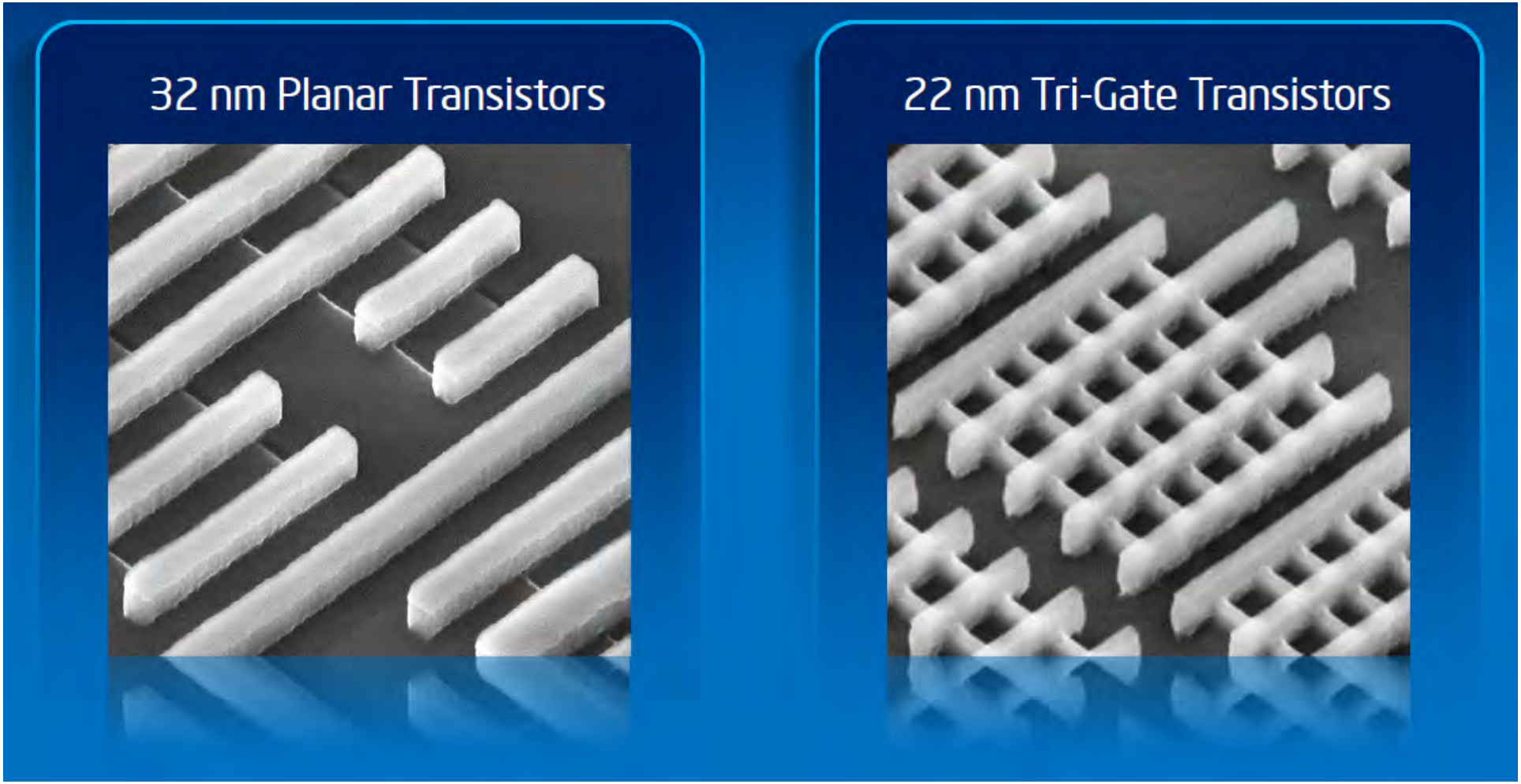
Gate delay measured via ring oscillator. Source: Intel 2011

22 nm tri-gate transistors reduce active power by up to >50%



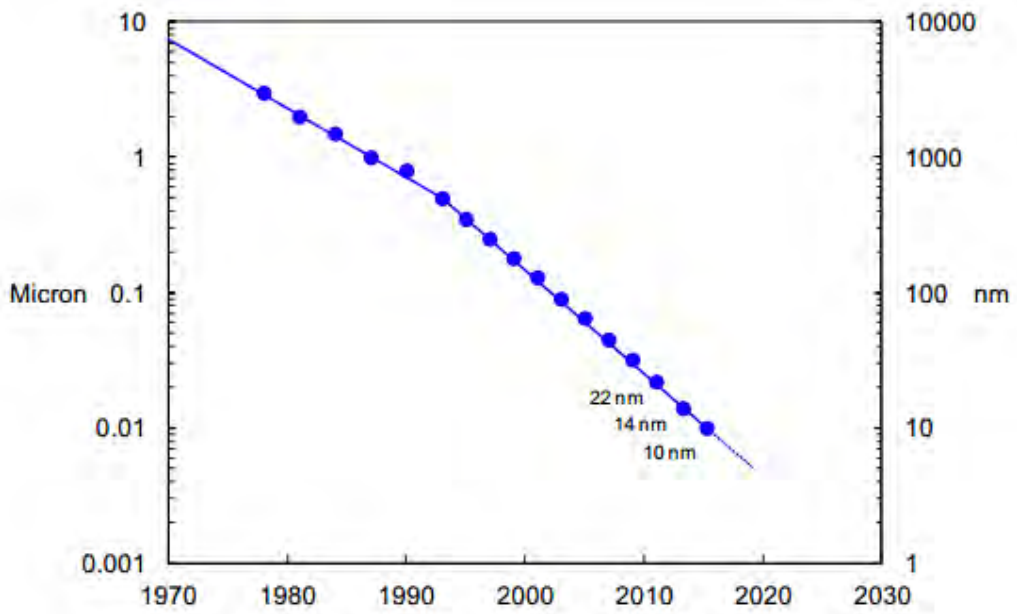
Gate delay measured via ring oscillator. Source: Intel 2011

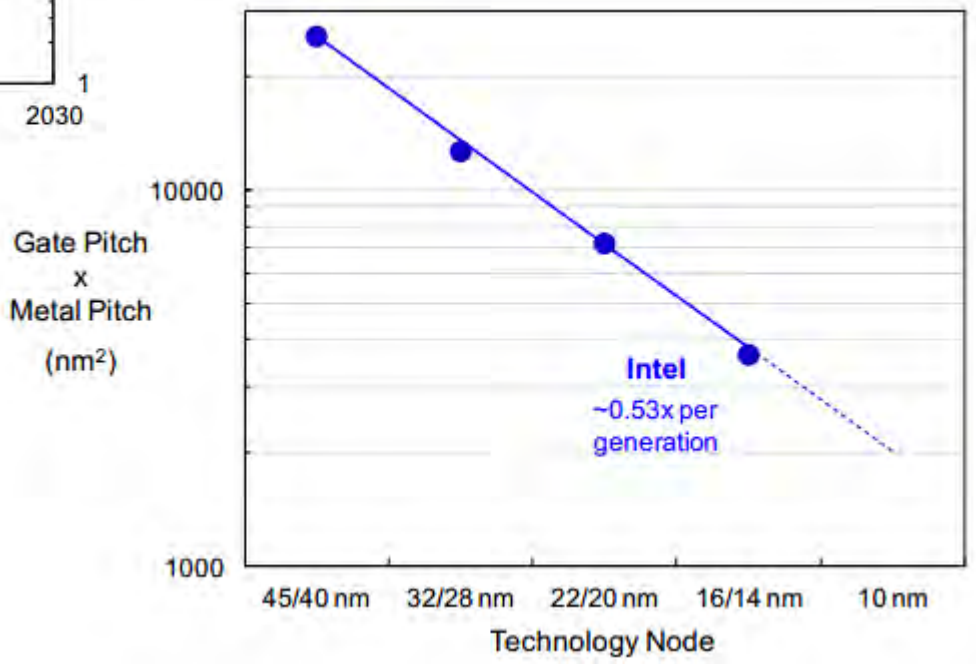
Tri-gate transistors in 22nm



Source: Intel 2011

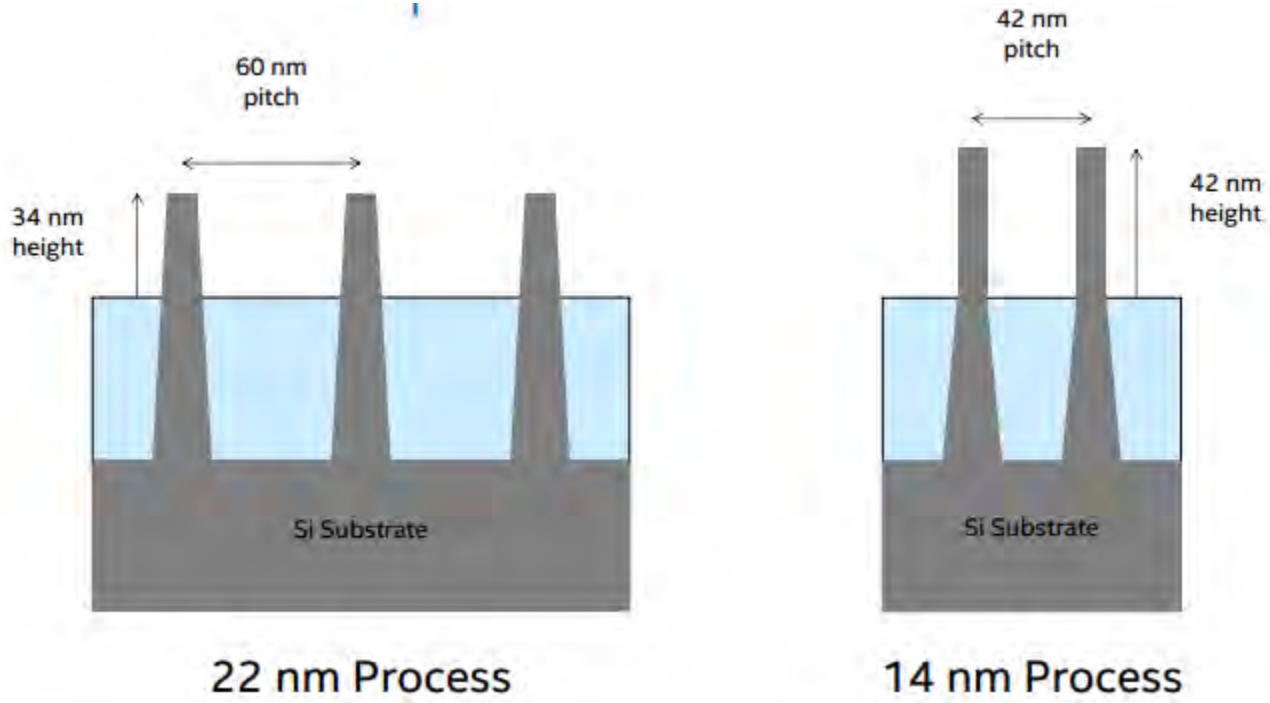
Scaling trends





Scaling trends defined by design rules. Source: Intel 2014

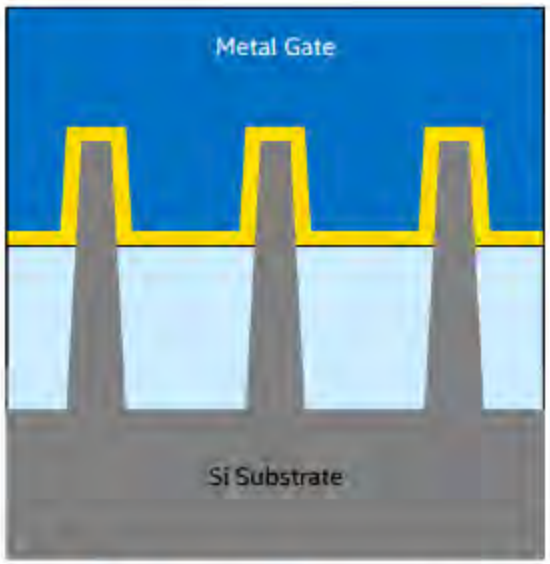
Transistor fin improvement



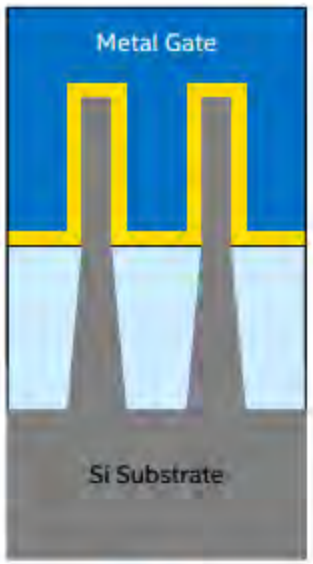
- Tighter fin pitch for improved density
- Taller and thinner fins for increased drive current and performance
- Reduced number of fins for improved density and lower capacitance

Features defined by design rules. Source: Intel 2014

Transistor fin improvement



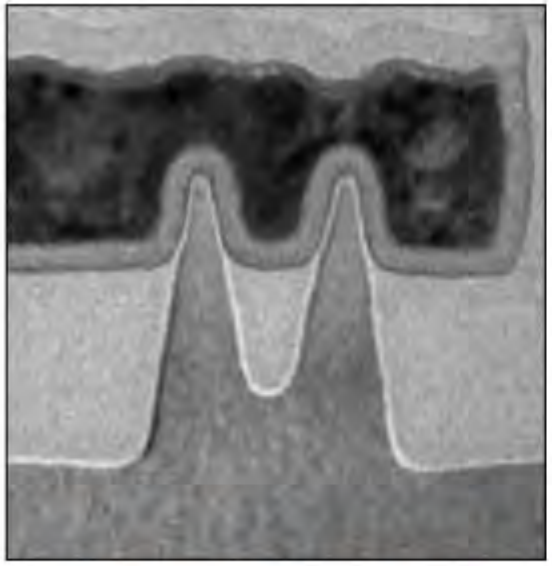
22 nm 1st Generation
Tri-gate Transistor



14 nm 2nd Generation
Tri-gate Transistor

Features defined by design rules. Source: Intel 2014

Transistor fin improvement

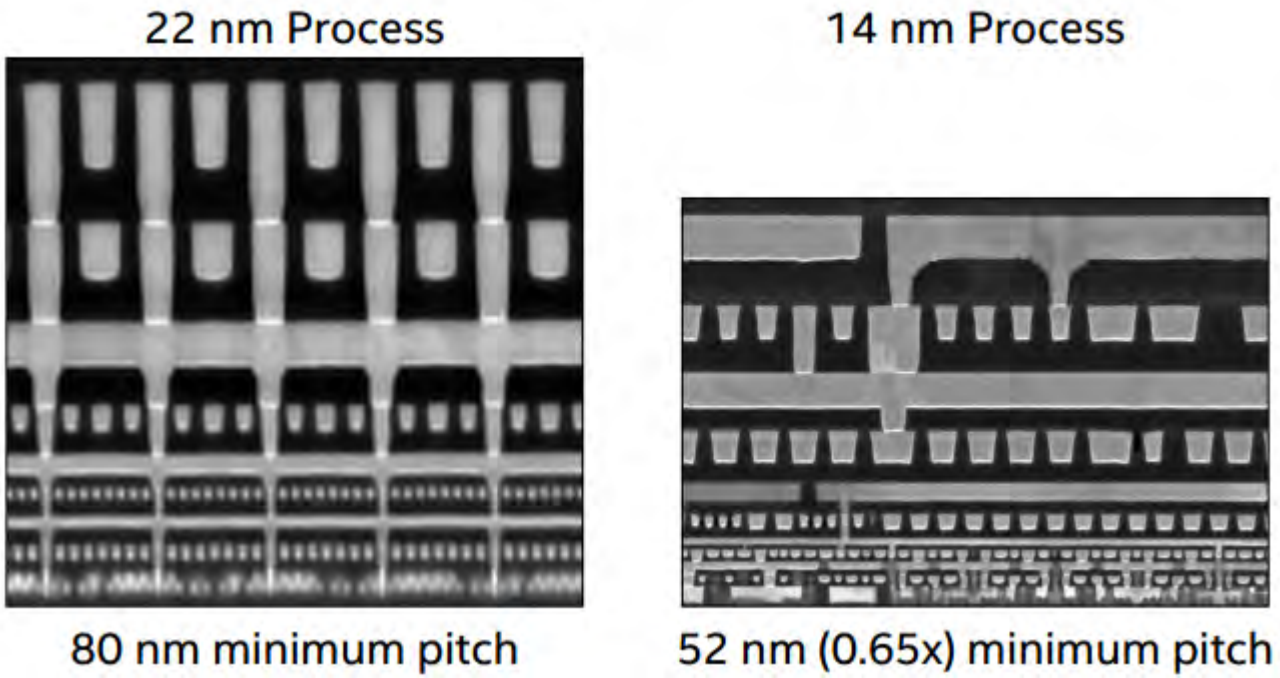


22 nm 1st Generation
Tri-gate Transistor

14 nm 2nd Generation
Tri-gate Transistor

Scanning electron microscope cross section. Source: Intel 2014

Interconnects

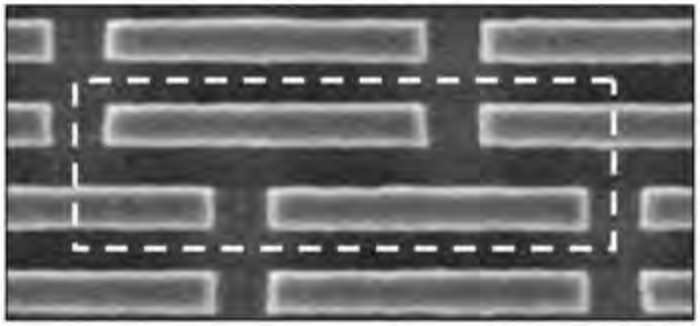


- Better than normal interconnect scaling

Features defined by design rules. Source: Intel 2014

SRAM memory cells

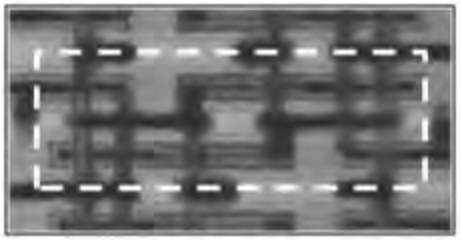
22 nm Process



.108 um²

(Used on CPU products)

14 nm Process

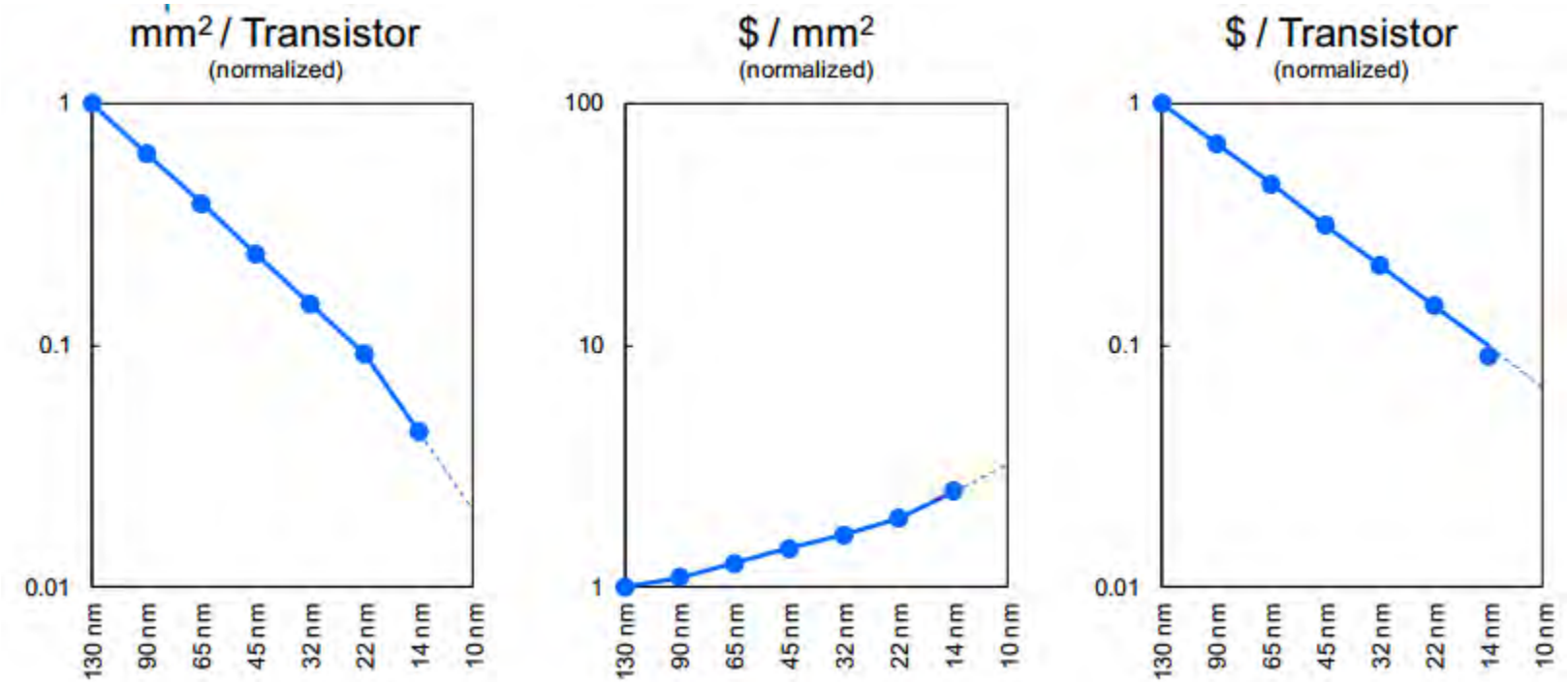


.0588 um²

(0.54x area scaling)

Features defined by design rules. Source: Intel 2014

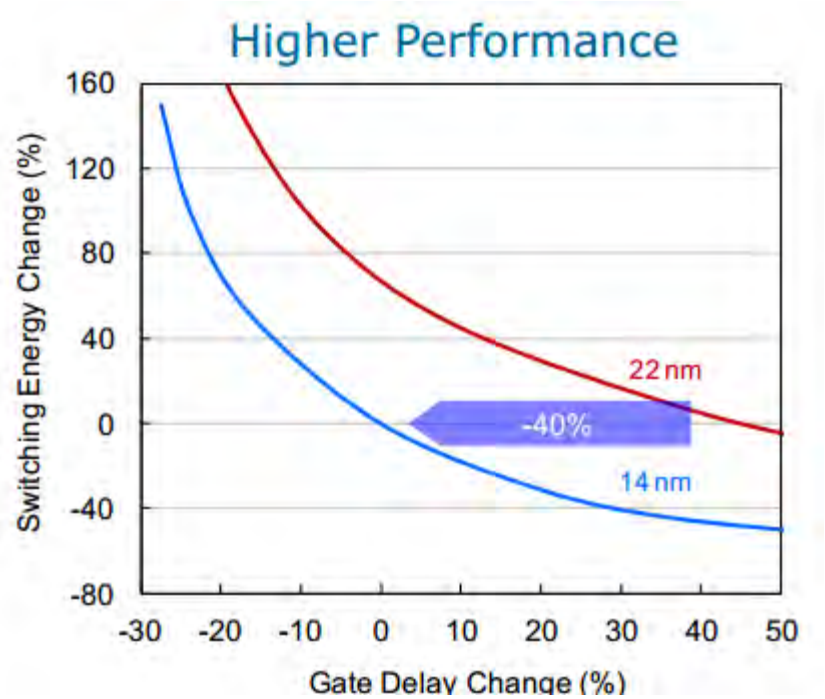
Cost per transistor

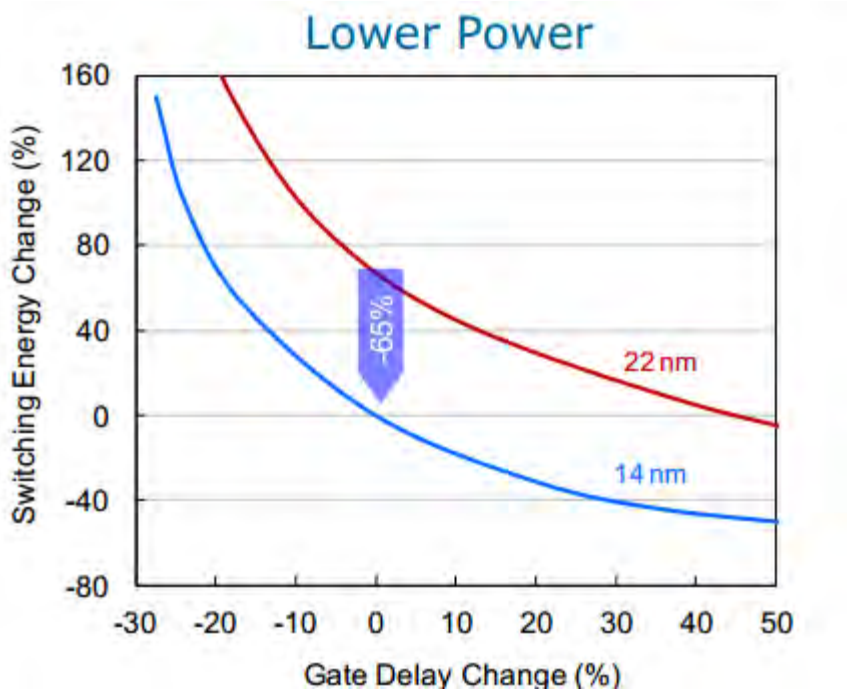


- Better than normal area scaling by using advanced double patterning techniques
- Wafer cost increasing due to added masking steps
- Still delivering lower cost per transistor

Source: Intel 2014

Transistor improvements continues in14nm





Gate delay measured via ring oscillator. Source: Intel 2014

Agenda

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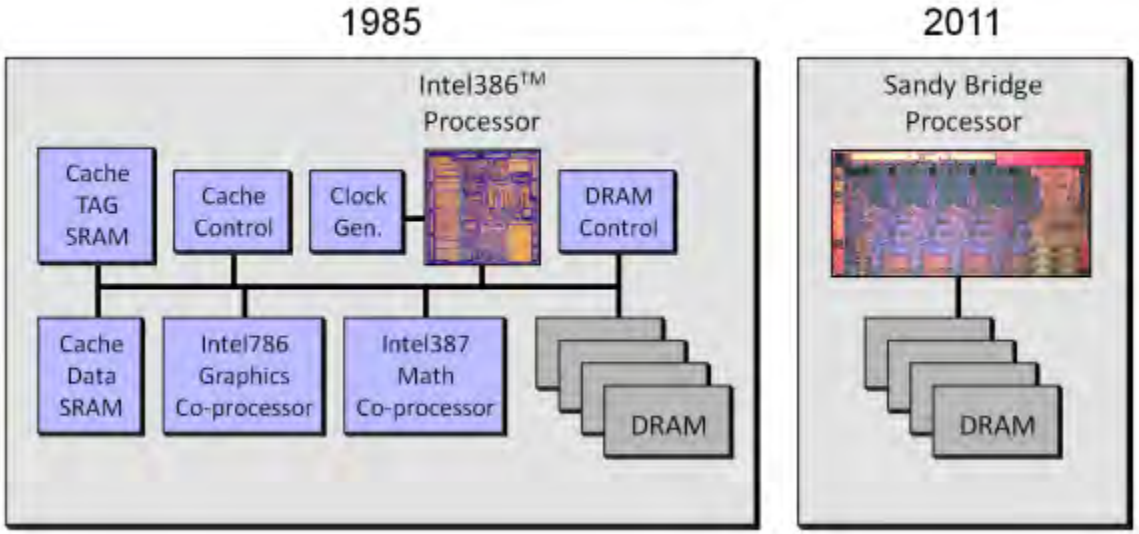
- Introduction to SoC

System integration



- Moore's law continues to enable ever increasing levels of chip complexity
- Creates a paradigm in system level HW/SW co-design

Source: Intel 2014, Cadence

What is a SoC?

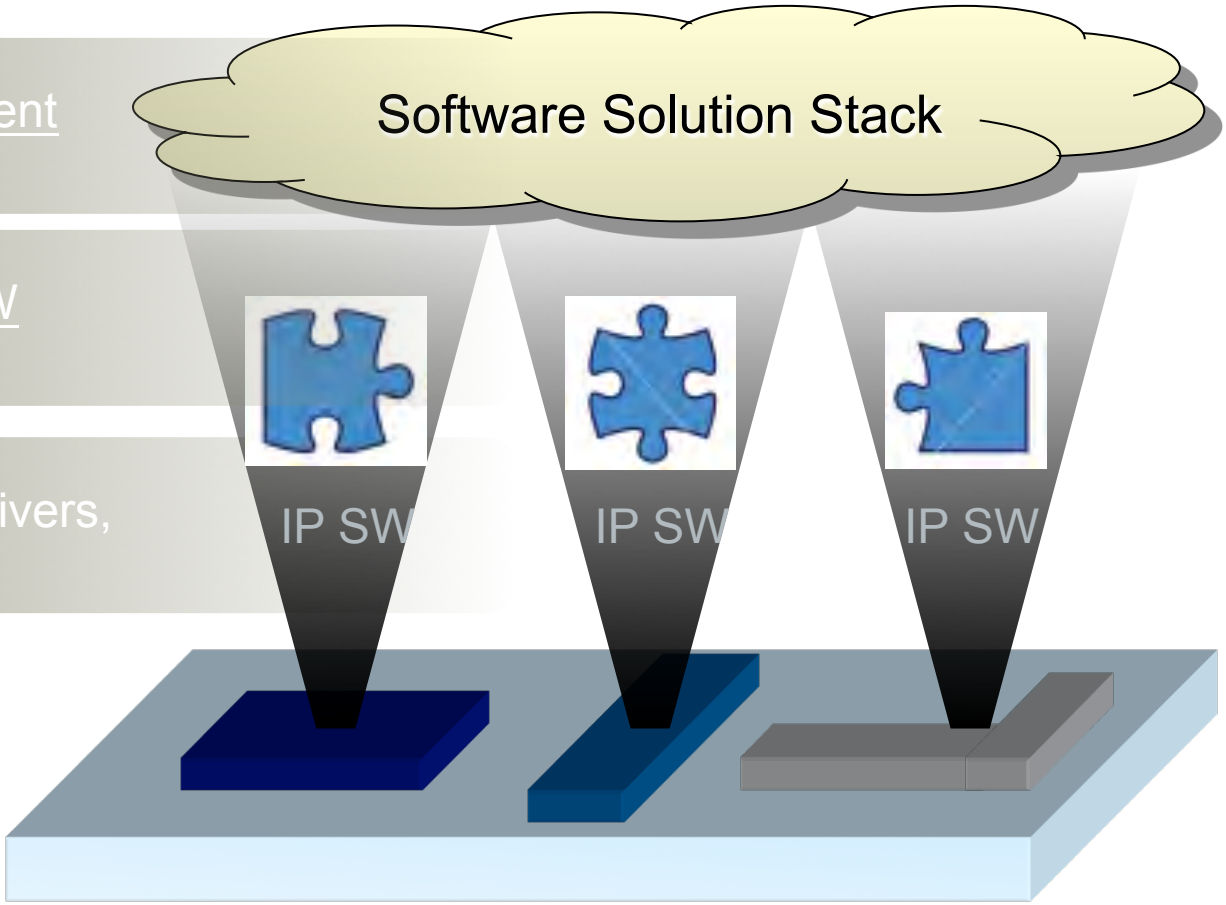
- System-on-a-chip refers to integrating all components of a computer or other electronic system into a single integrated circuit (IC) chip. It may contain digital, analog, mixed-signal, and often radio-frequency functions – all on a single chip substrate. (Wikipedia)
- This consolidation enables smaller, thinner devices while reducing the amount of power required for the device, increasing battery life and making possible always-on and always-connected functionality.
- A SoC consists of both the hardware and the software that controls the microcontroller, microprocessor or DSP cores, peripherals and interfaces.

SoC challenge #1 – beyond silicon: software and system

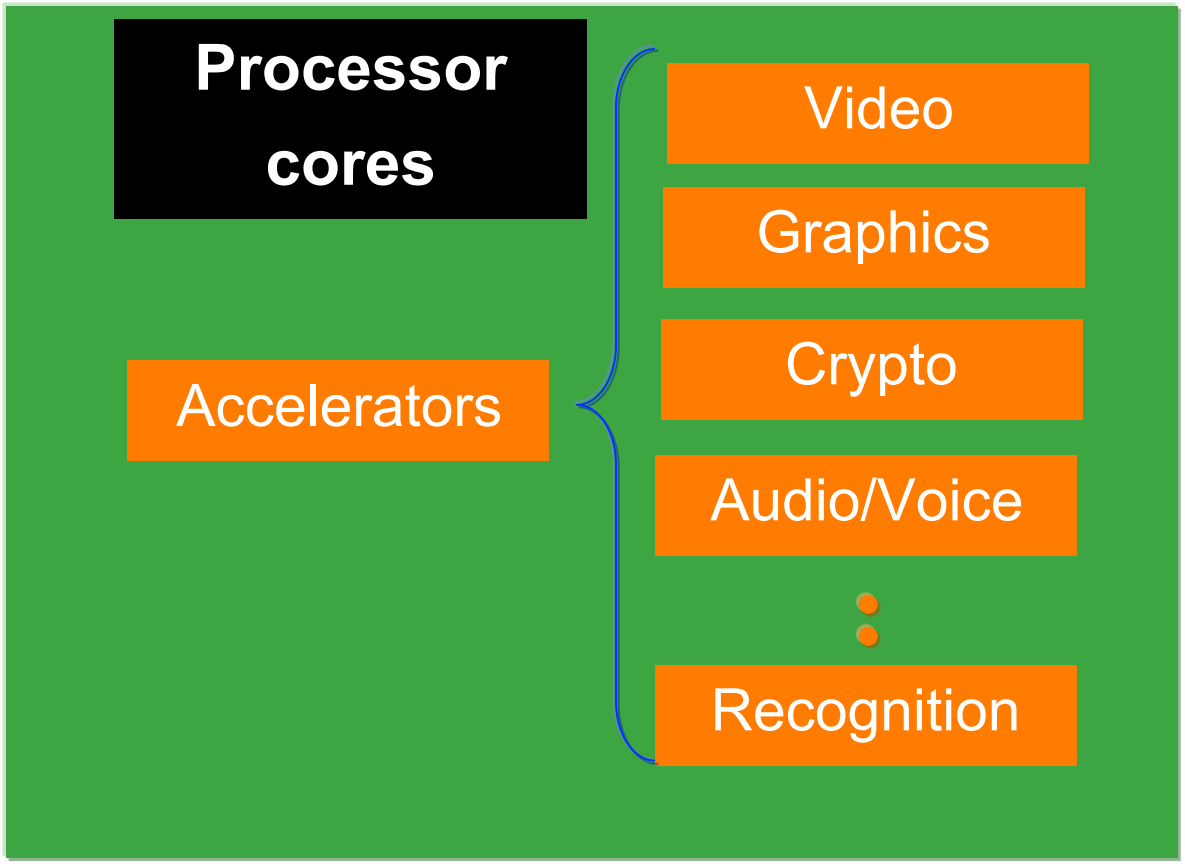
Early SW development

Well-defined system SW frameworks

Software Modularity: Drivers, Firmware



SoC challenge #2 - Dealing with heterogeneity



SoC challenge #3 – on-die interconnect

Apply tools used for off-chip networks?

- Design space: topology, switching, routing, flow control, virtualization
- Cost metrics: wire bisection, switch size, total power, total devices
- Performance Metrics: throughput, latency, traffic structure independence/robustness, hot spot performance, quality of service

Important differences -- Integration, costs, technology, workloads, energy… tradeoffs reopened

SoC challenge #4 – SoC realization

- A critical gap between SoC development process and the process of conceptualizing and analyzing designs at a system level (a high level of abstraction) without the restrictions of physical operating constraints
- Software application developers must have access to the system level implementation before the SoC is actually manufactured to test and debug the software and uncover any SoC architectural problems
- No connection between these two different levels of abstractions.

- How to ensure ***system architectural intent or design coherence***?

SoC: New Discipline

- Map the system level information to the next level of abstraction
- Need tools to guide the design from concept to implementation and ensure design coherence from one level to the next
- Must make available a complete hardware/software platform that will provide all the necessary support for end-user applications
- Need Hardware-Software Co-Design: meeting of system-level objectives by exploiting the tradeoffs between hardware and software in a system through concurrent design
- Concurrent development: Hardware and Software Developed at the same time on parallel paths
- Integrated development: Interaction between hardware and software development to produce design meeting performance criteria and functional specs.

Summary

- In 2014, Moore's law is alive and well!
  - Scaling requires continue innovation in device materials and structures
- Moore's law enabling ever increasing levels of chip complexity
- Creating a new paradigm of system level HW/SW co-design
- SoC as a new discipline driving the industry to develop new competencies and tools

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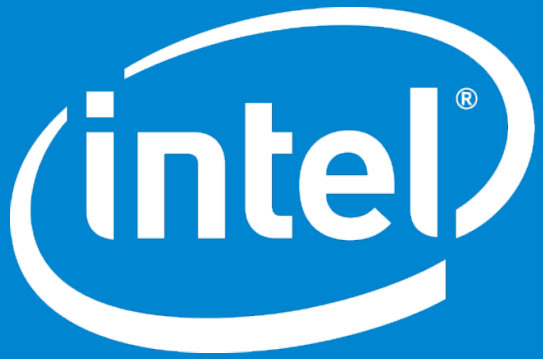
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