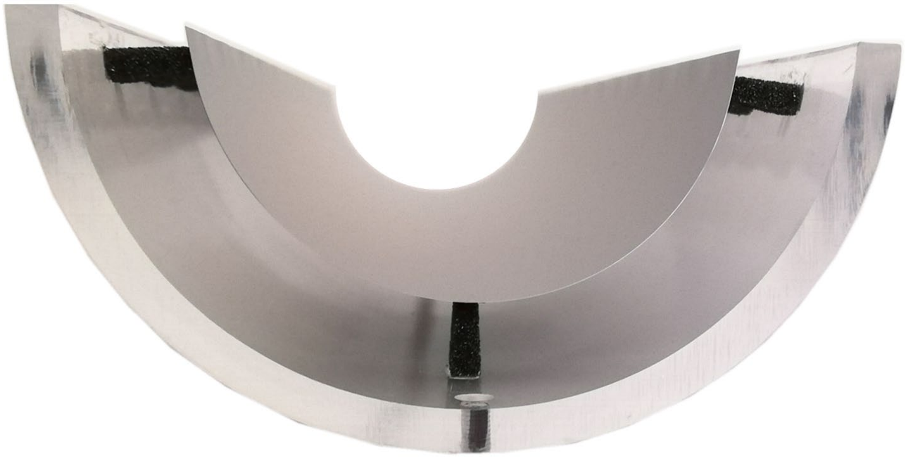
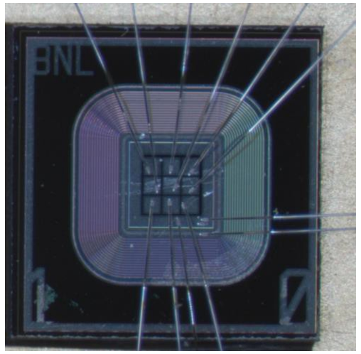
Curved, free standing MAPS…





… and fast timing

Giacomo Contin (Università and INFN Trieste)

Brown Bag Instrumentation Seminar – LBL – March 17th, 2021

Outline

- A free-standing detector based on curved silicon
  - The idea behind ALICE ITS3
  - Bent silicon performance
  - R&D highlights

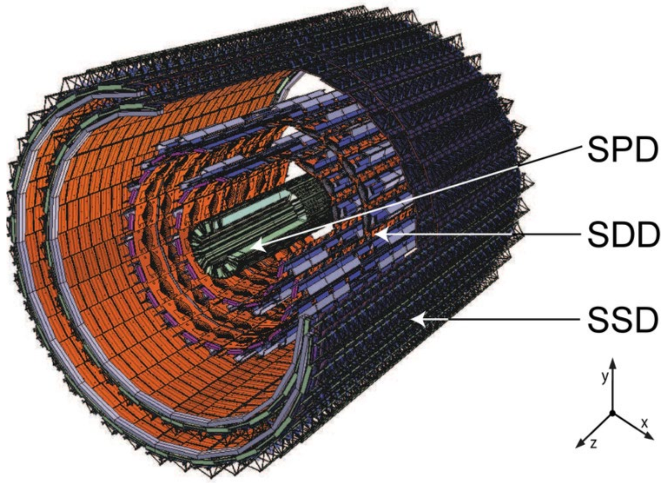
- Timing with silicon
  - LGAD, SPAD/SiPM, FD-MAPS
  - Characterization campaign towards a 20 ps resolution

Includes material and help from: M. Suljic (CERN), M. Mager (CERN), G. Giacomini (BNL), L. Pancheri (UniTN - INFN), F. Carnesecchi (UniBO – INFN), R. Preghenella (UniBO – INFN), C. Gargiulo (CERN), I. Tymchuk (LTU) and many others

Evolution of the ALICE ITS

2009-2019

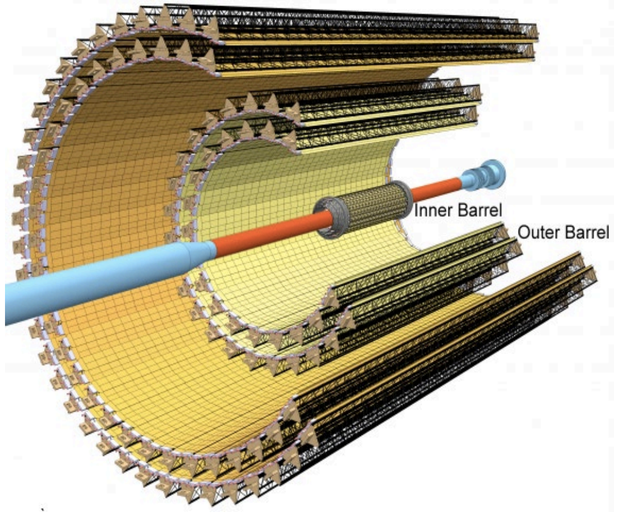
ALICE ITS-1



Readout rate: 1 kHz
Thickness of first layer: 1.14%X_0

2021+

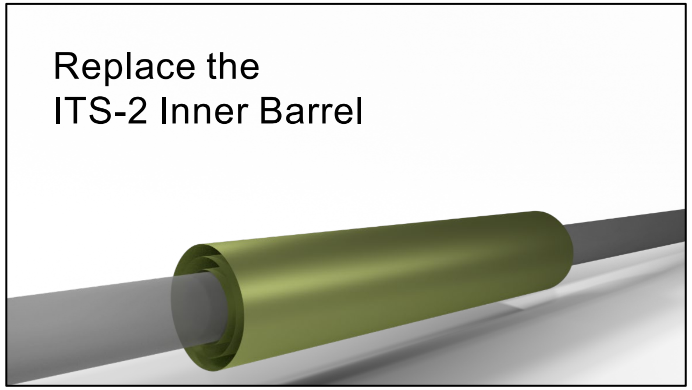
ALICE ITS-2



Integration time: <20 μs
Thickness IB layer: 0.35%X_0

2026+

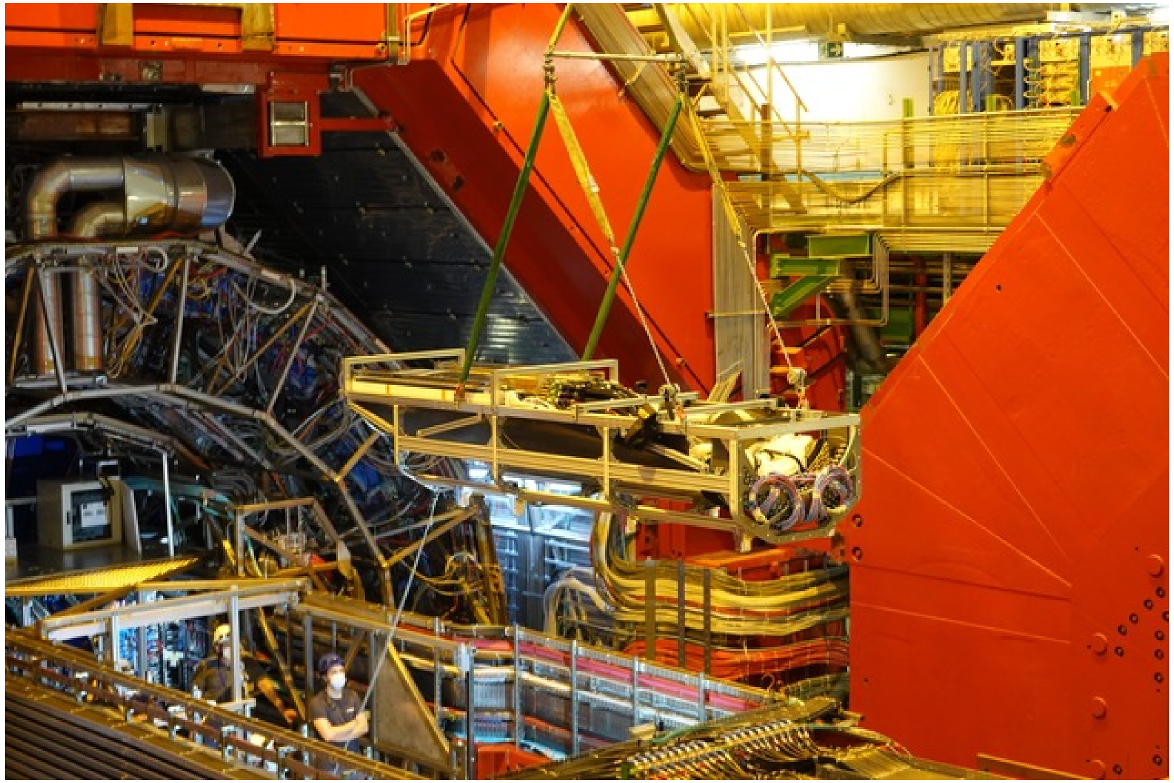
ALICE ITS-3



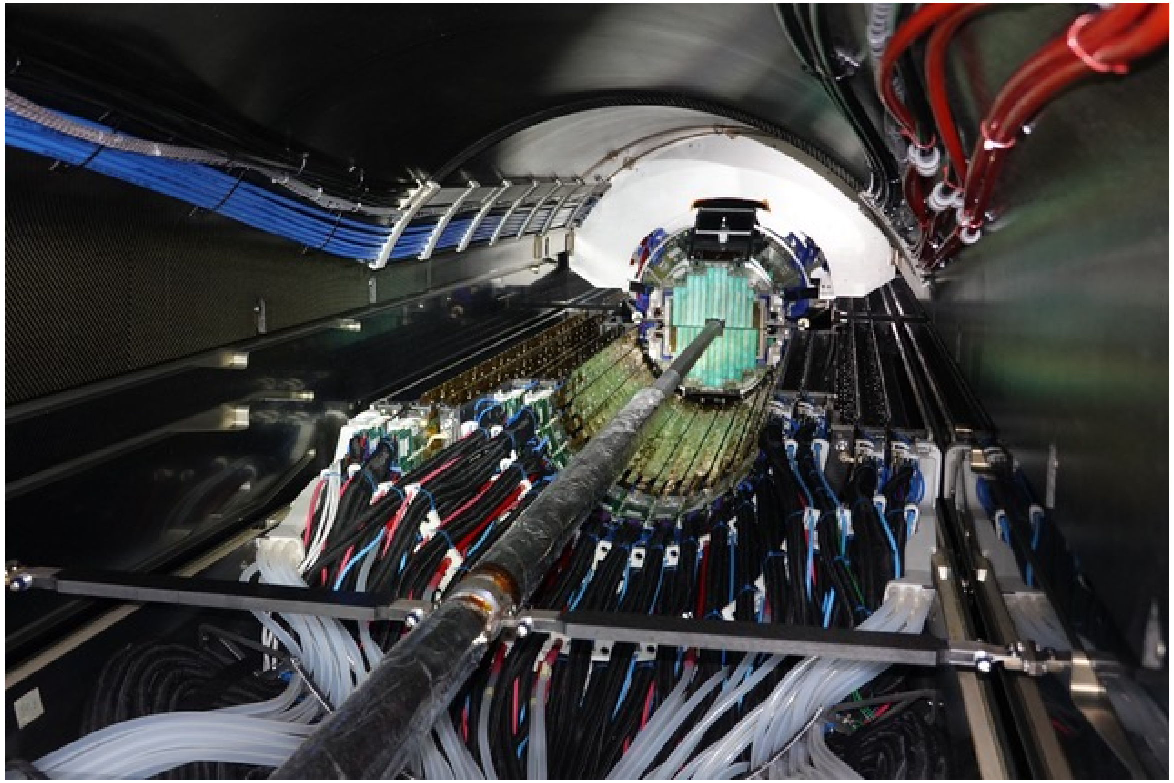
Innermost layer: at R = 18 mm
Thickness of each layer: 0.05%X_0

- Constant search for a thinner and simpler geometry…

Pictures of ITS2 installation from yesterday!



ITS2 Top Outer Barrel flying towards the ALICE magnet

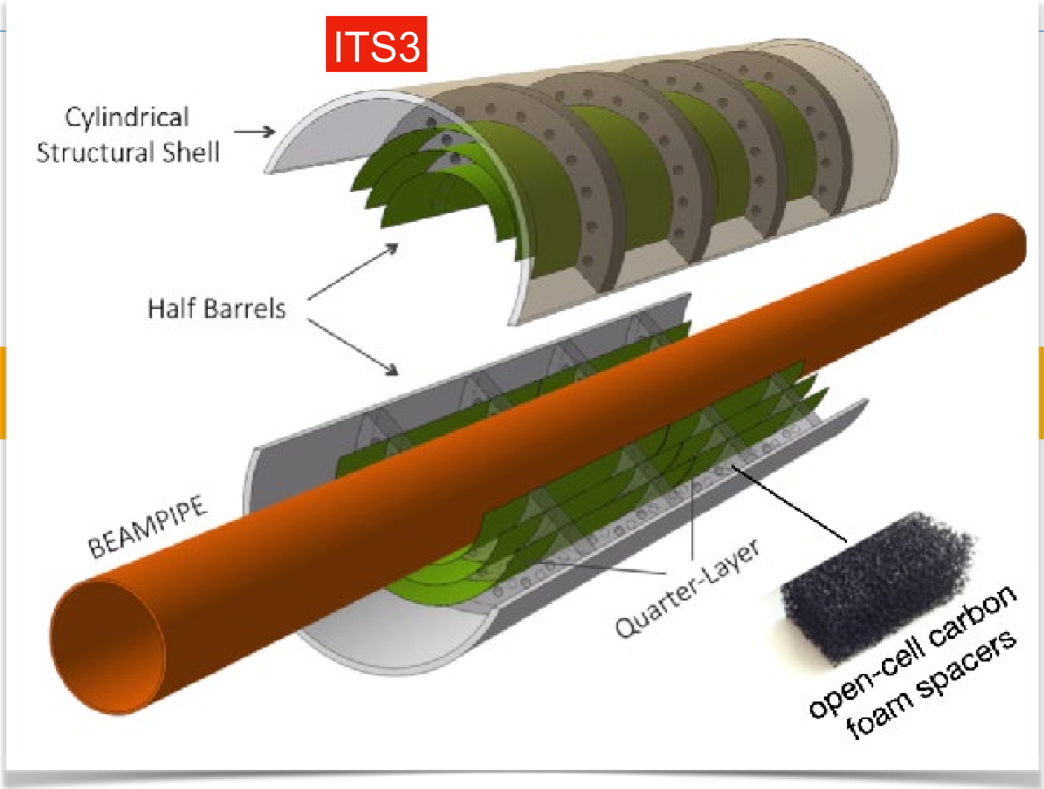


ITS2 Top Outer Barrel installed in the final location

ITS3 detector layout

replace

by



in LS3

key improvements:

- closer to beam pipe: 23→18 mm
- less material: 0.3 → ~0.03 $\%X_0$

main benefit:

- better tracking performance
- especially at low p_T

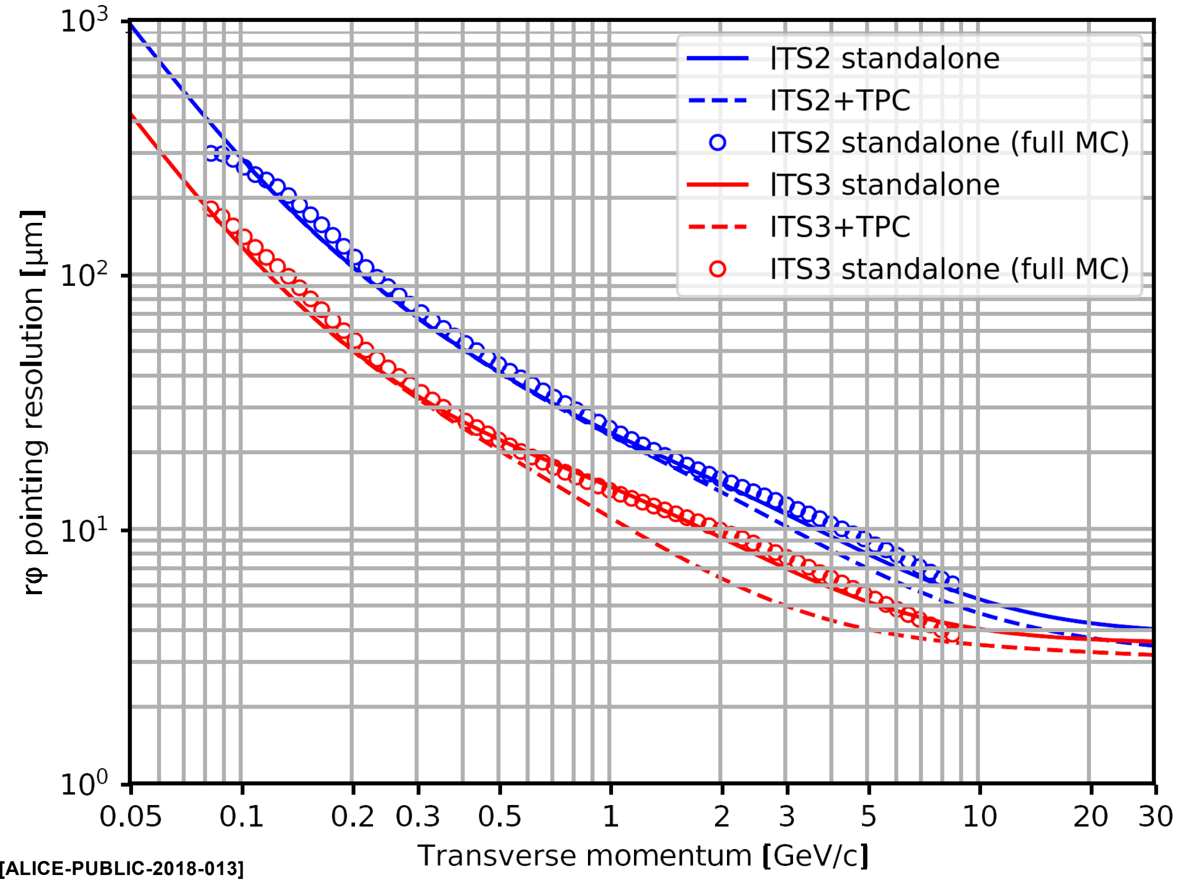
based on:

- wafer-scale (up to ~28x10 cm),
- ultra-thin (20-40 µm),
- bent (R=18, 24, 30 mm)

Si sensors (MAPS)

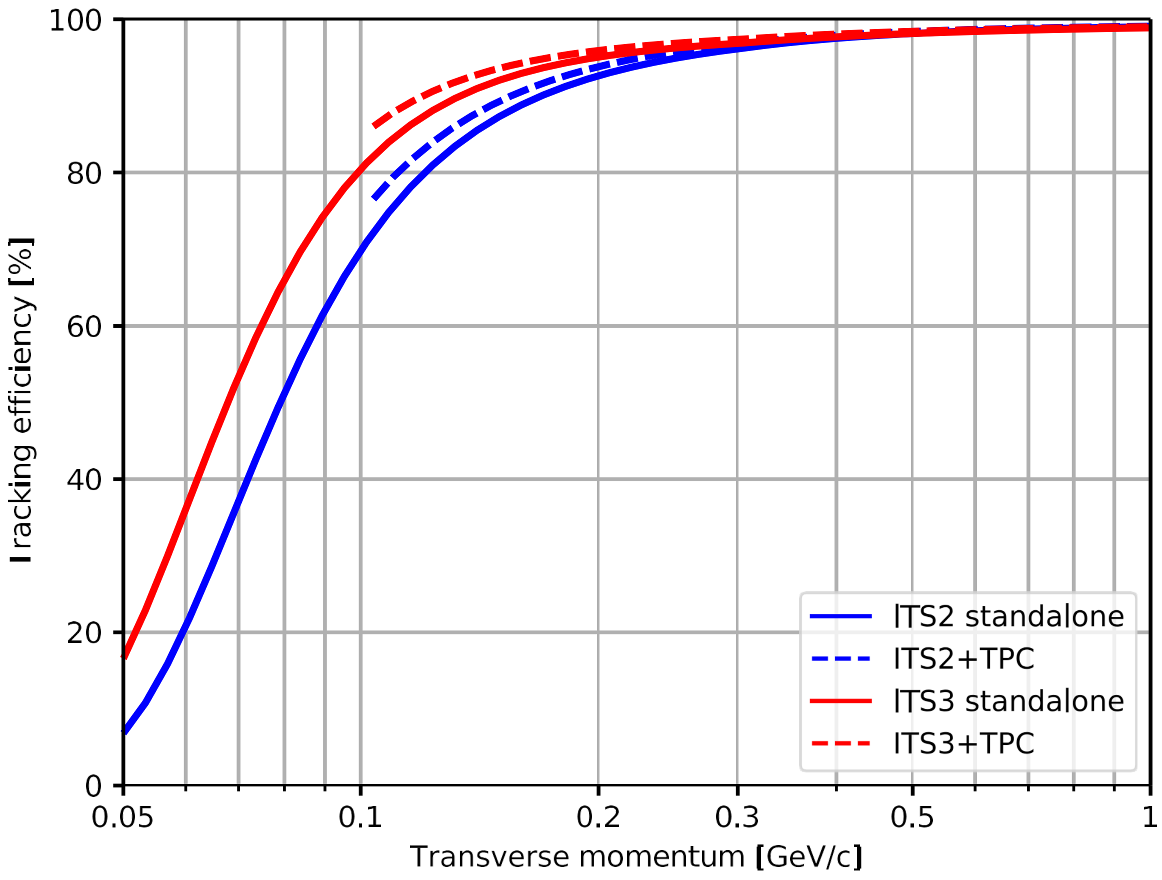
ITS3 projected performance

pointing resolution



[ALICE-PUBLIC-2018-013]

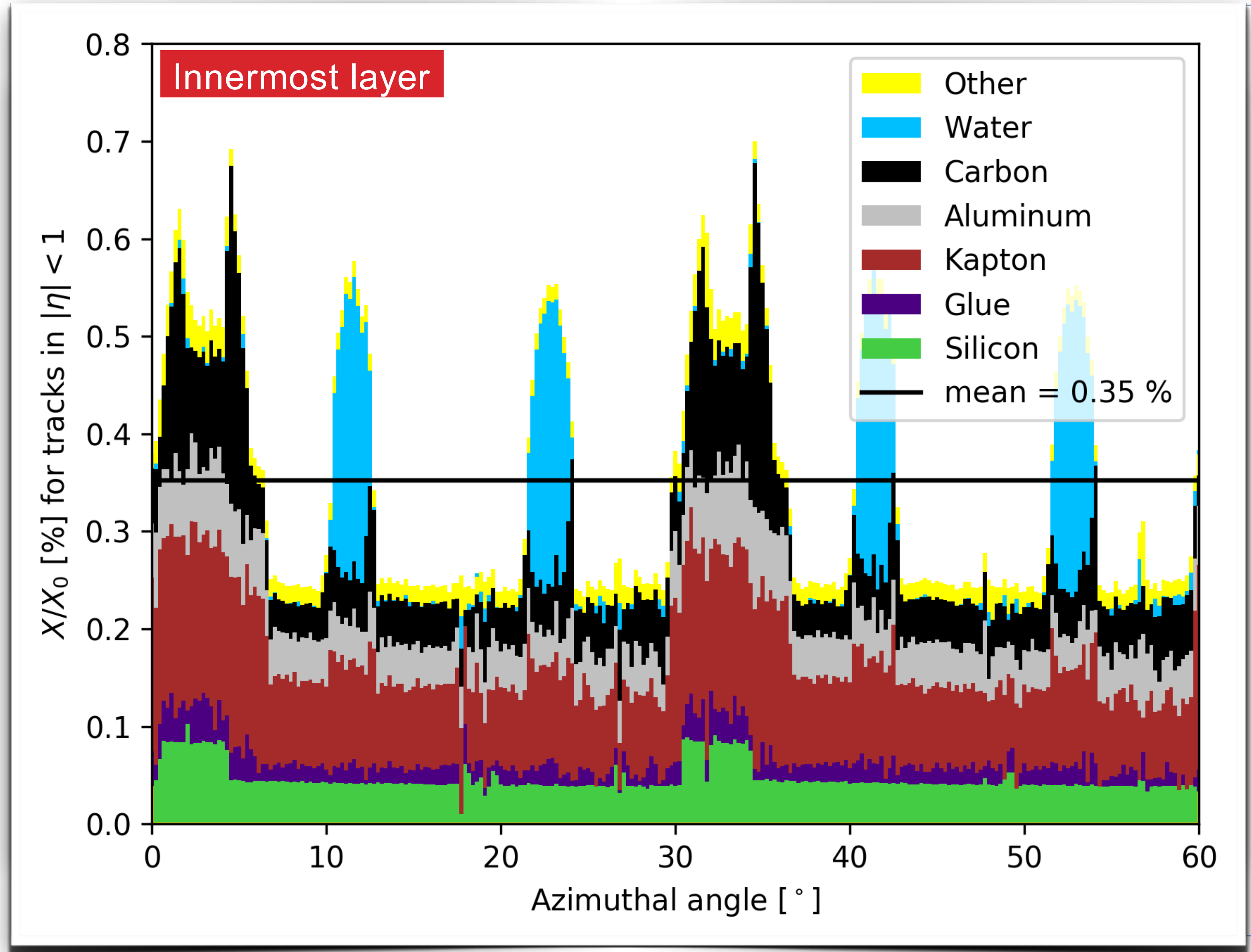
tracking efficiency



improvement of factor 2 over all momenta

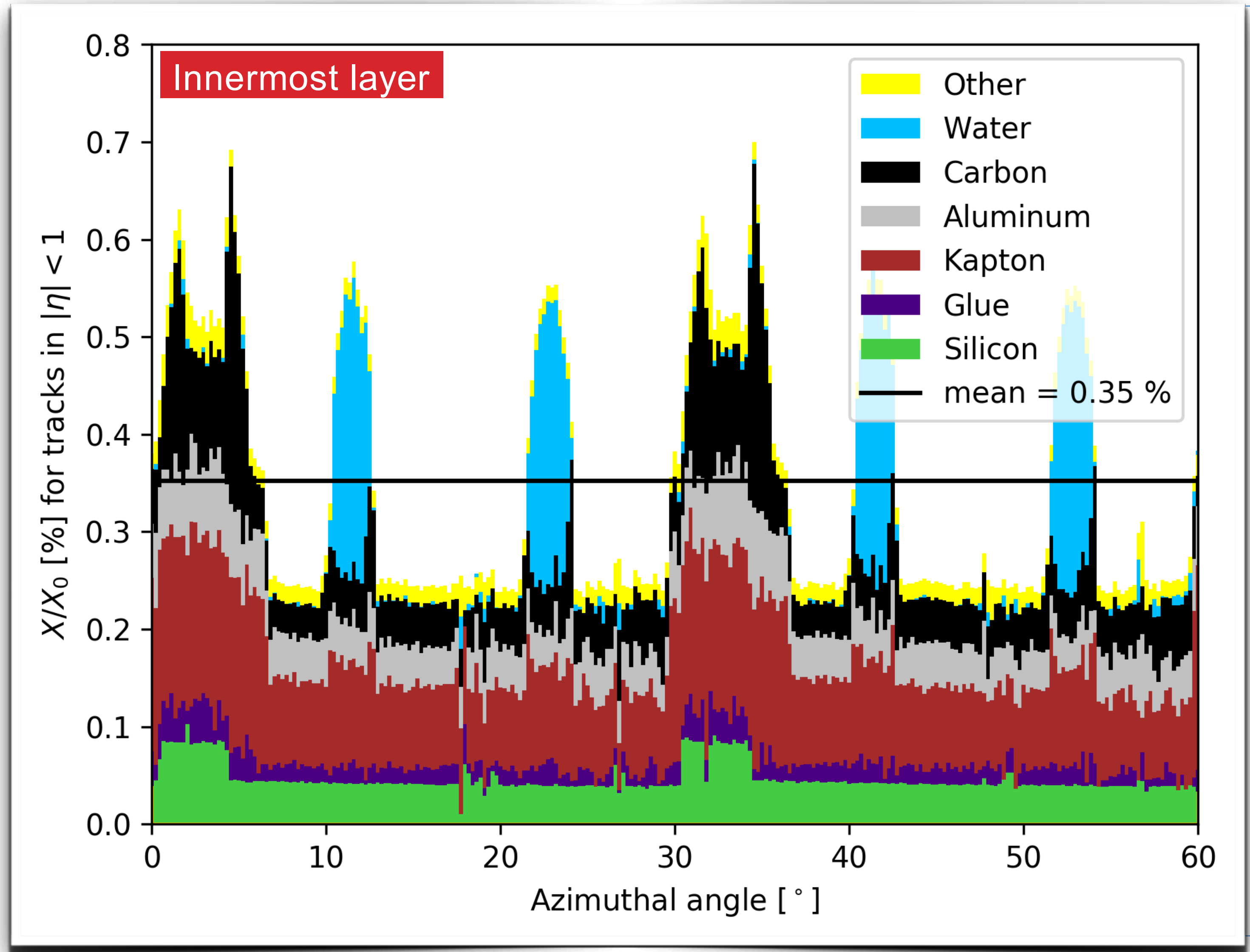
large improvement for low transverse momenta

Material budget



- Observations:
  - Si makes only 1/7-th of total material budget
  - Non-uniformity due to support, cooling & overlaps

Material budget



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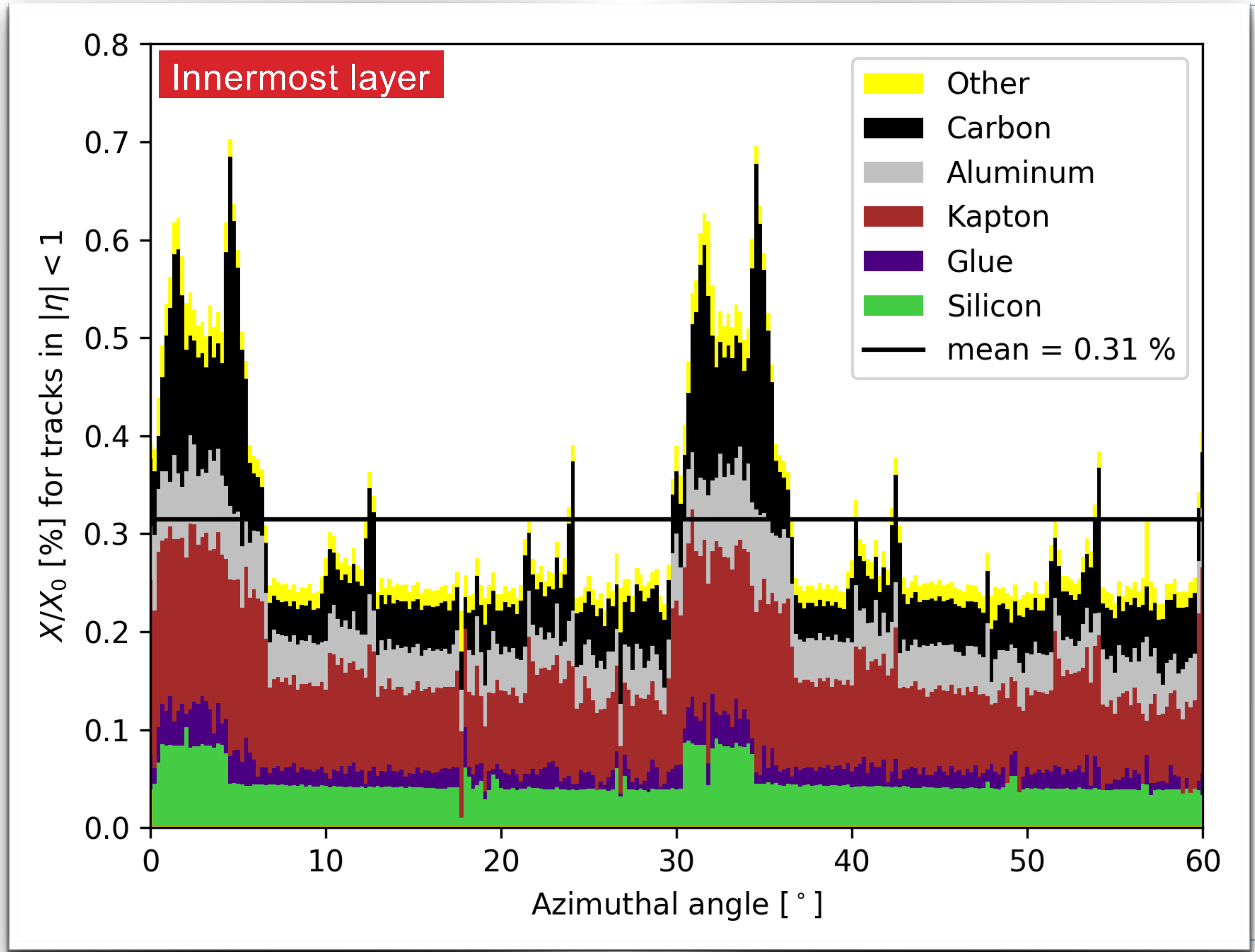
- Removal of water cooling:
  - If **power consumption < 20 mW/cm^2**

Material budget



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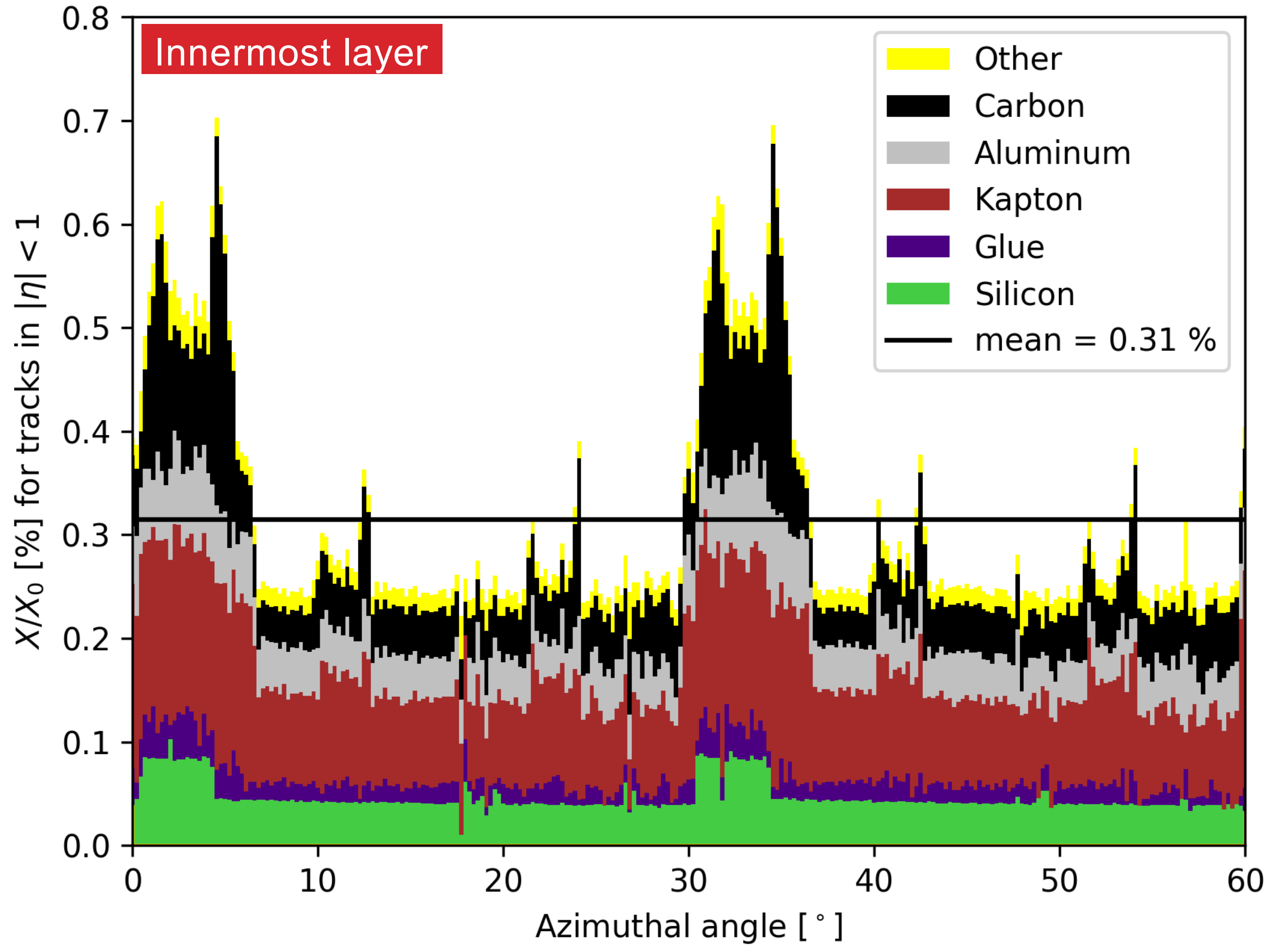

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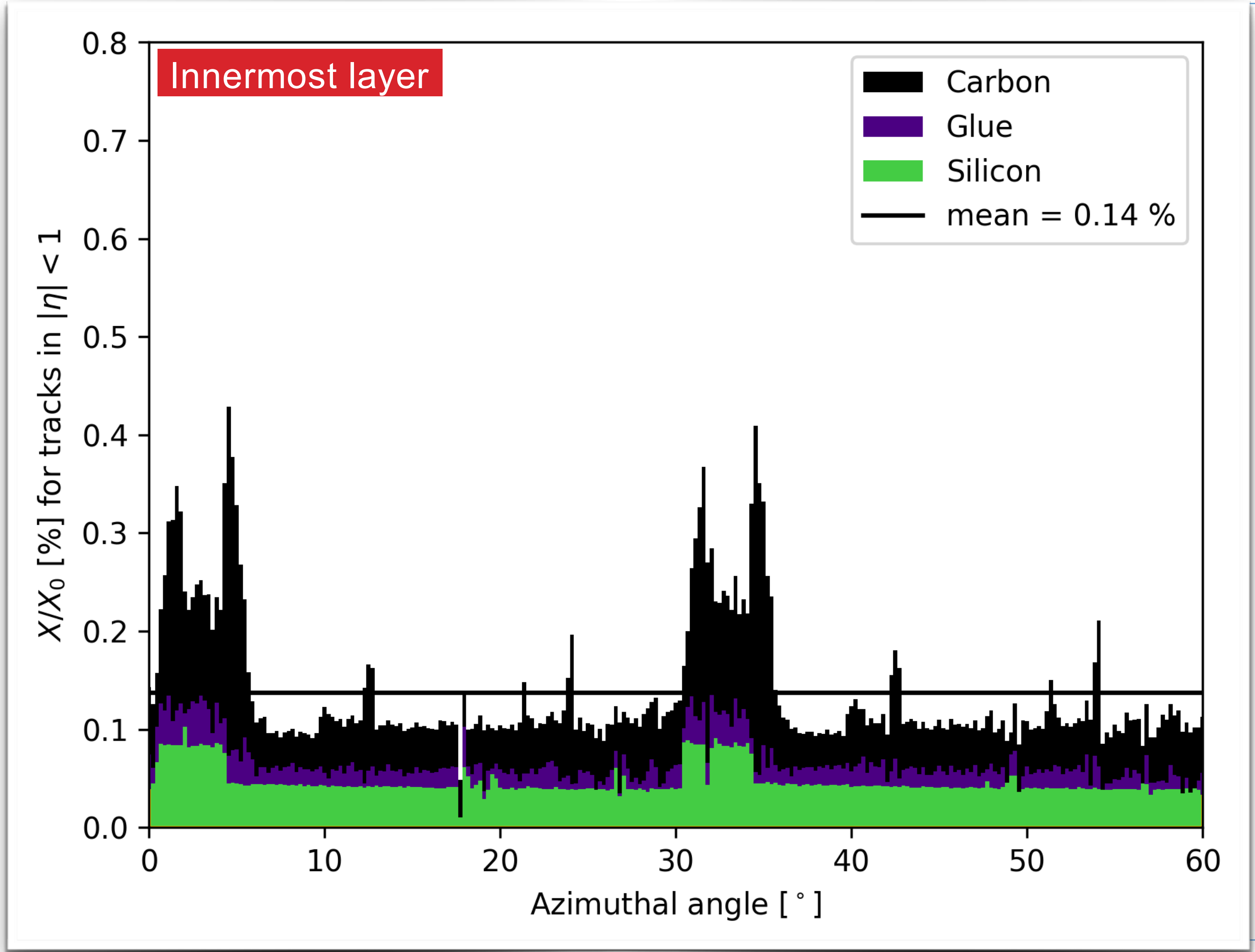

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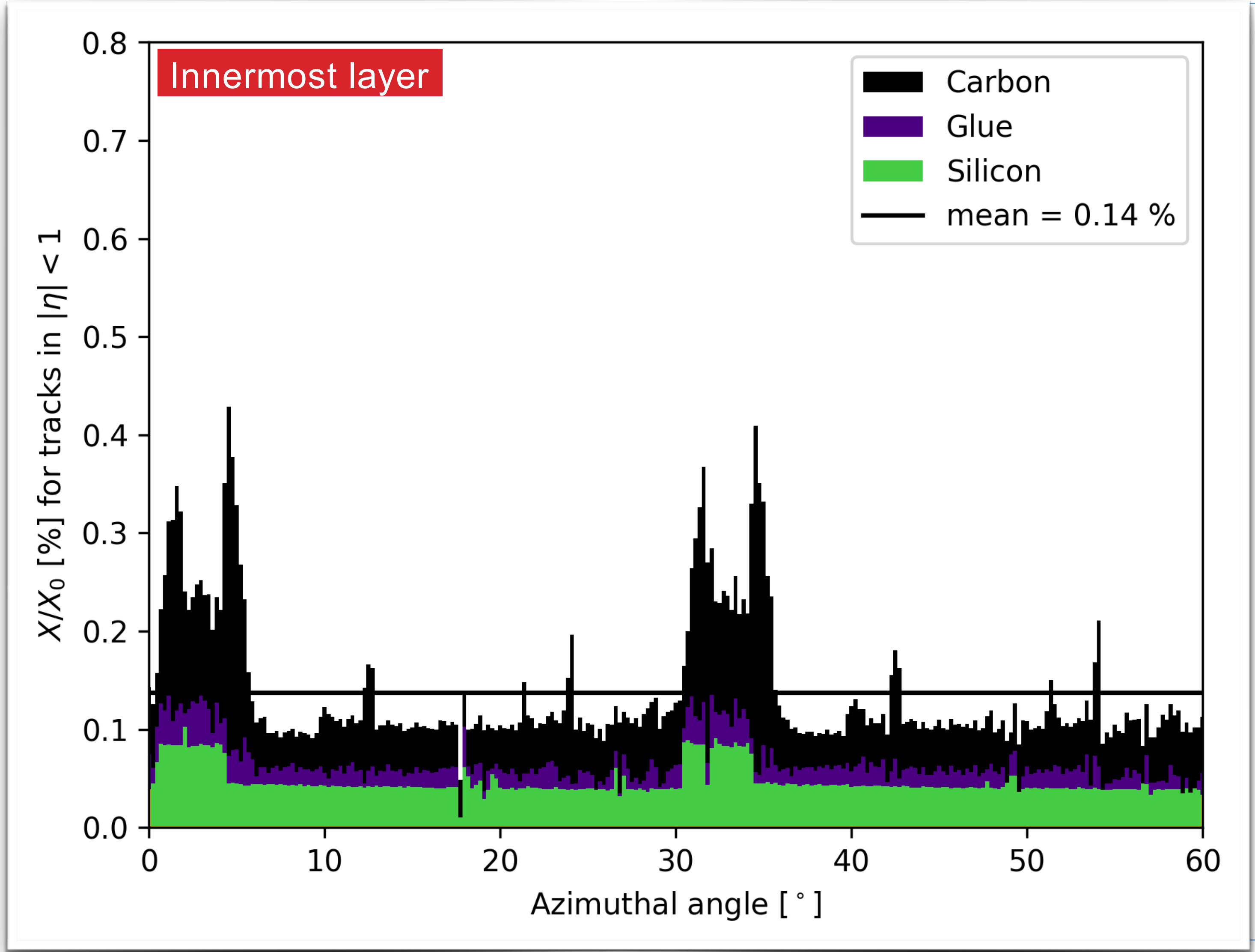

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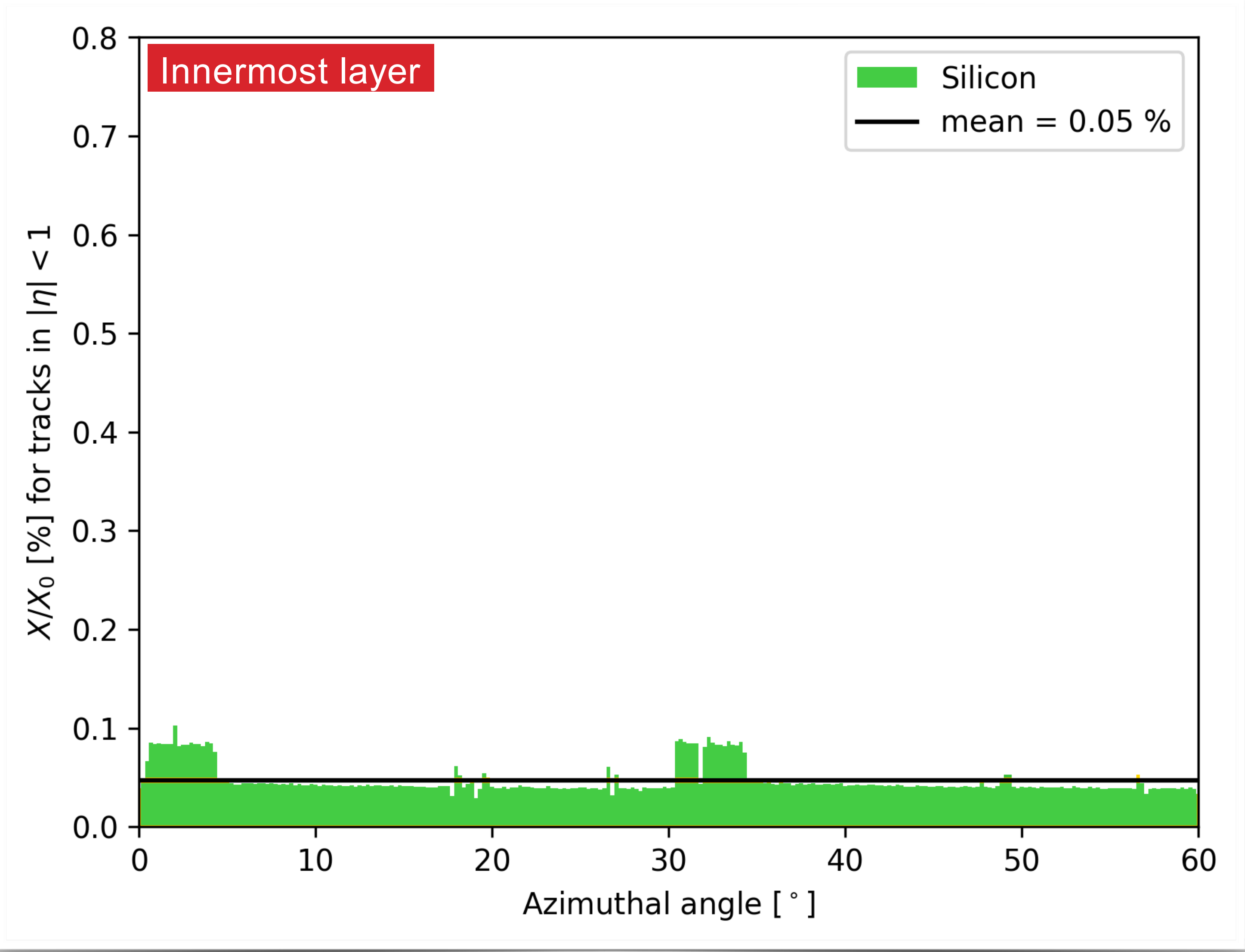
- Removal of mechanical support:
  - **Self-supporting arched structure**

Material budget



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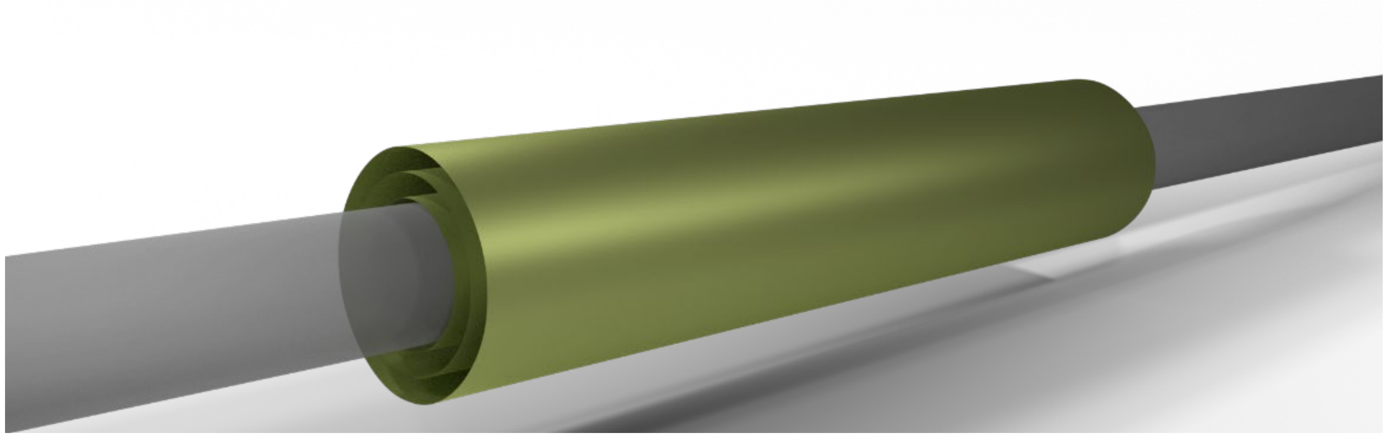
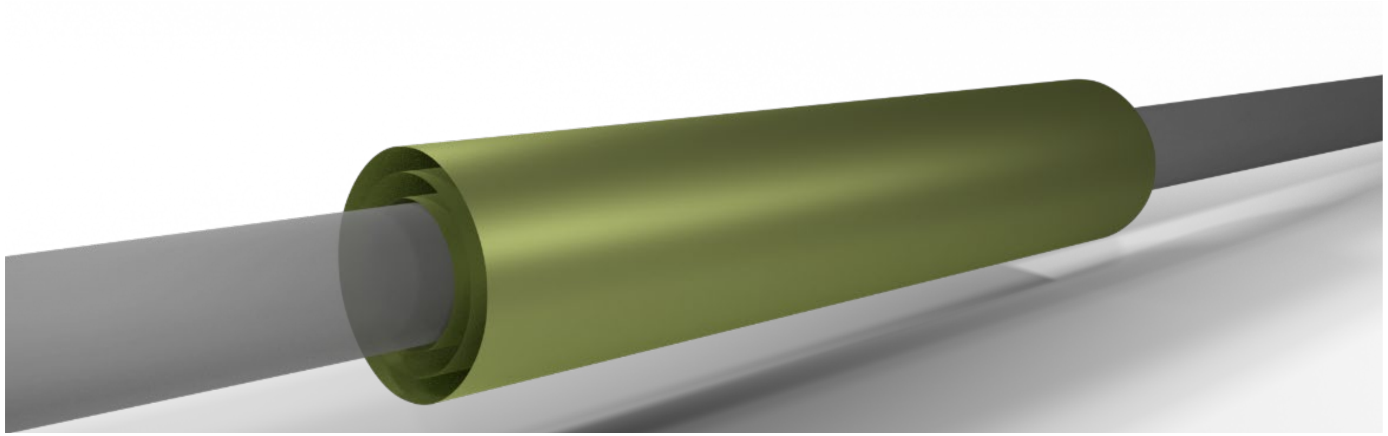
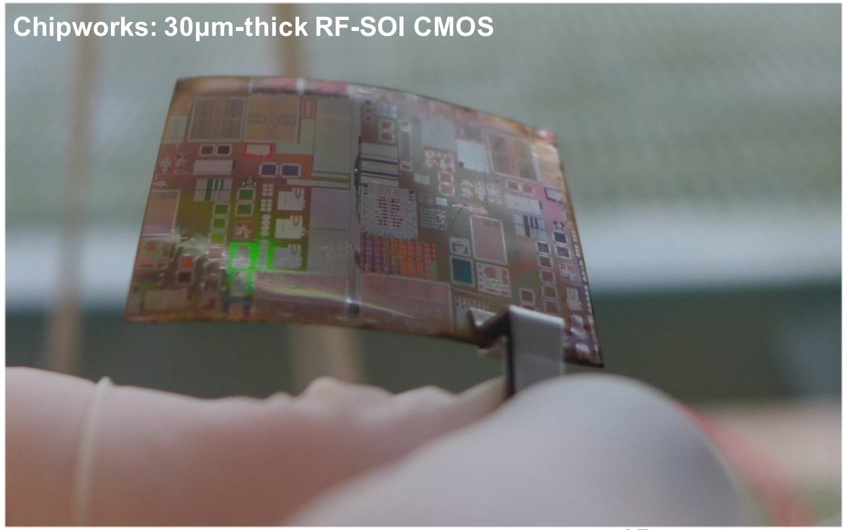
A dream: just silicon



A dream: just silicon - Curved



- Bending Si wafers + circuits is possible and has been tried!



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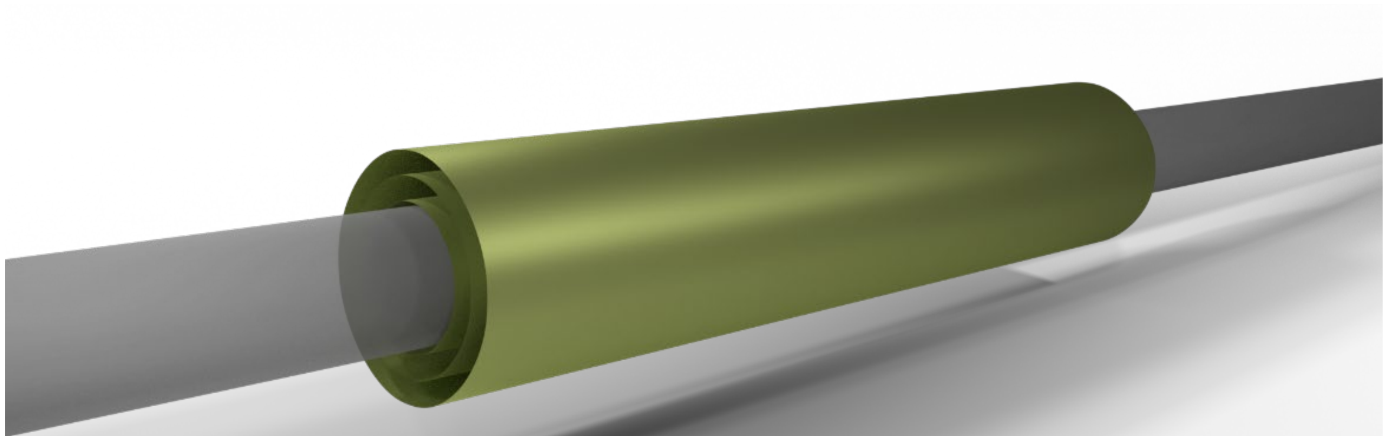


- Bending Si wafers + circuits is possible and has been tried!

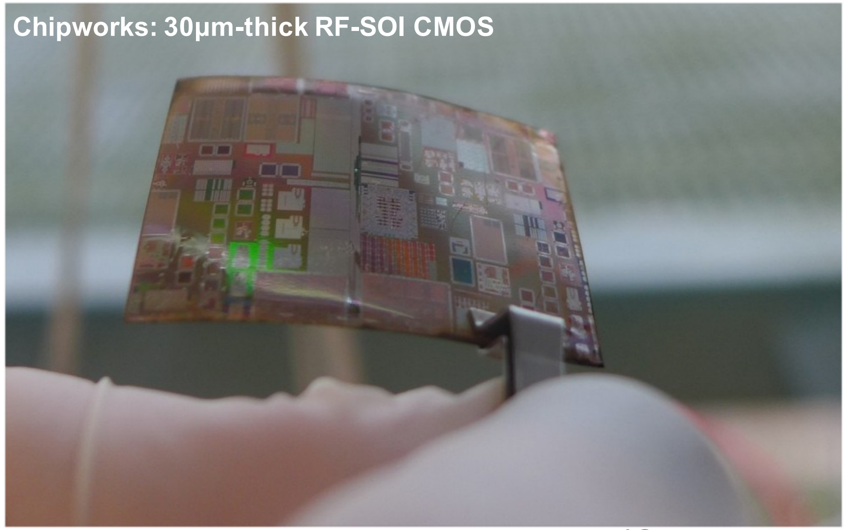
- Radii much smaller than needed have been achieved

- We need to thin it down to < 50 μm

Die type	Front/back side	Ground/polished/plasma	Bumps	Die thickness (μm)	CDS (MPa)	Weibull modulus	MDS (MPa)	r_{min} (mm)
Blank	Front	Ground	No	15–20	1263	7.42	691	2.46
Blank	Back	Ground	No	15–20	575	5.48	221	7.72
IZM28	Front	Ground	Yes	15–20	1032	9.44	636	2.70
IZM28	Back	Ground	Yes	15–20	494	2.04	52	32.7
Blank	Back	Polished	No	25–35	1044	4.17	334	7.72
IZM28	Back	Polished	Yes	25–35	482	2.98	107	24.3
Blank	Back	Plasma	Yes	18–22	2340	12.6	679	2.50
IZM28	Front	Plasma	Yes	18–22	1207	2.64	833	2.05
IZM28	Back	Plasma	Yes	18–22	2139	3.74	362	4.72

D.A. van den Ende et al., Microelectronics Reliability, vol. 54, pp. 2860-2870, 2014
http://dx.doi.org/10.1016/j.microrel.2014.07.125

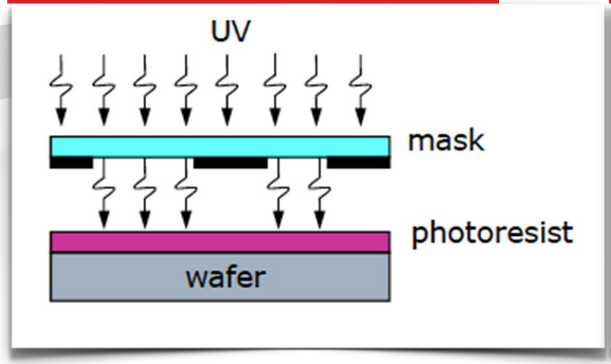

Silicon Genesis: 20 micron thick wafer


Chipworks: 30μm-thick RF-SOI CMOS

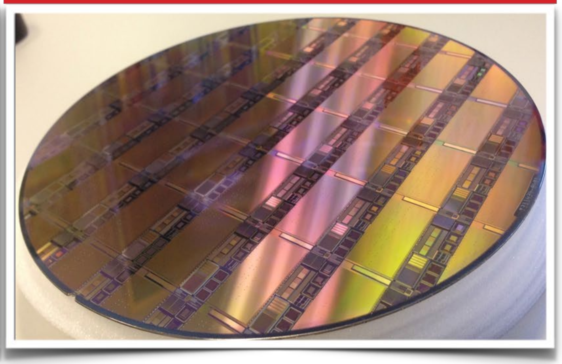
A dream: just silicon - Wafer-scale chip

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm^2
  - modules are tiled with chips connected to a flexible printed circuit board

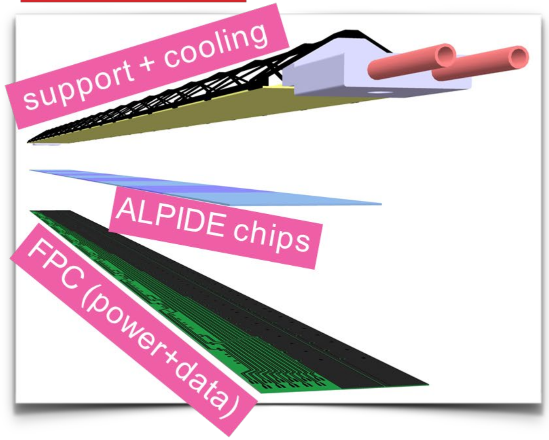
Principle of photolithography



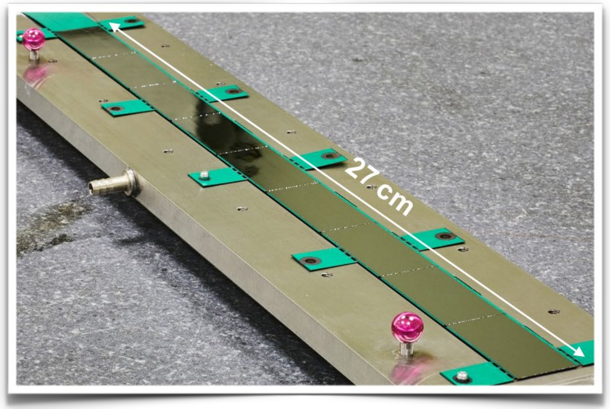
200 mm ALPIDE prototype wafer



Stave design



FPC + chips



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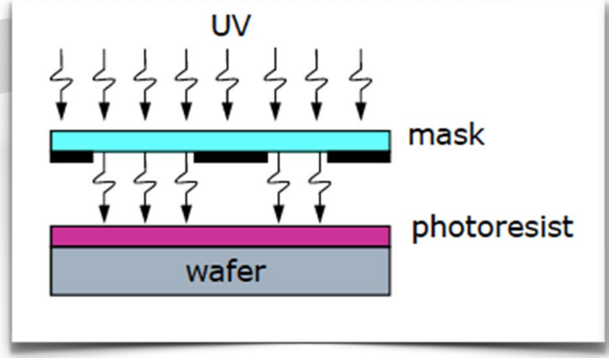
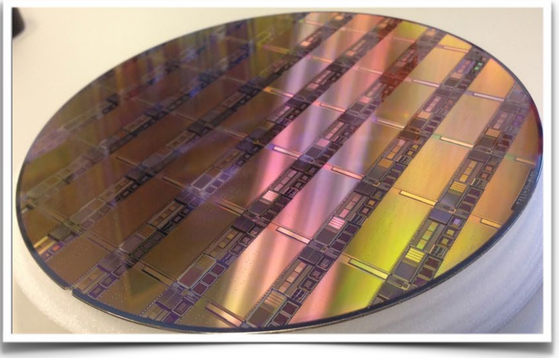
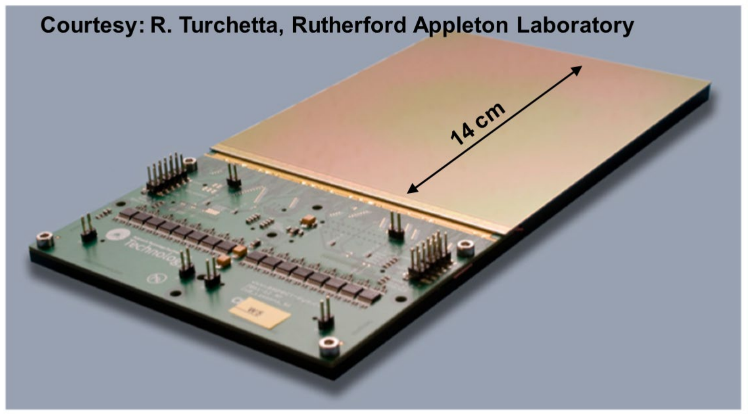


200 mm ALPIDE prototype wafer



- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - actively used in industry
  - requires dedicated chip design

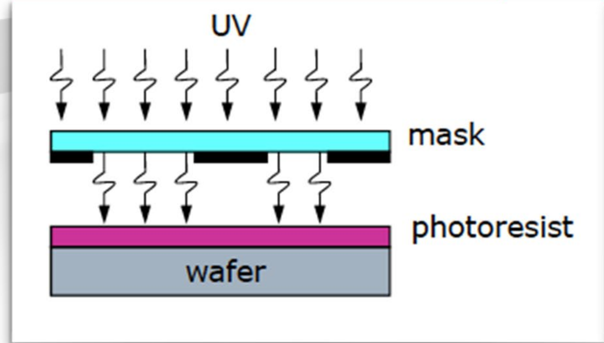
Wafer-scale sensor



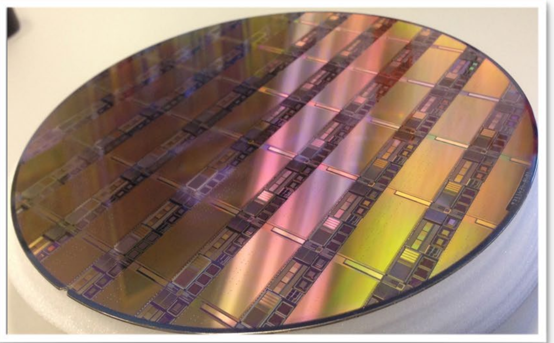
A dream: just silicon - 12” Wafer-scale chip

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm^2
  - modules are tiled with chips connected to a flexible printed circuit board

Principle of photolithography



200 mm ALPIDE prototype wafer



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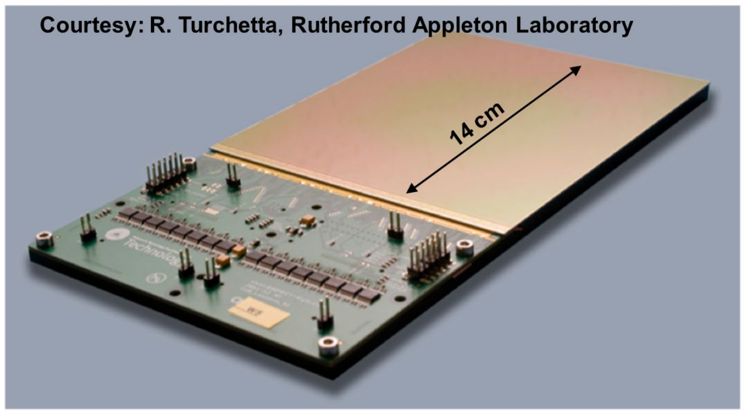
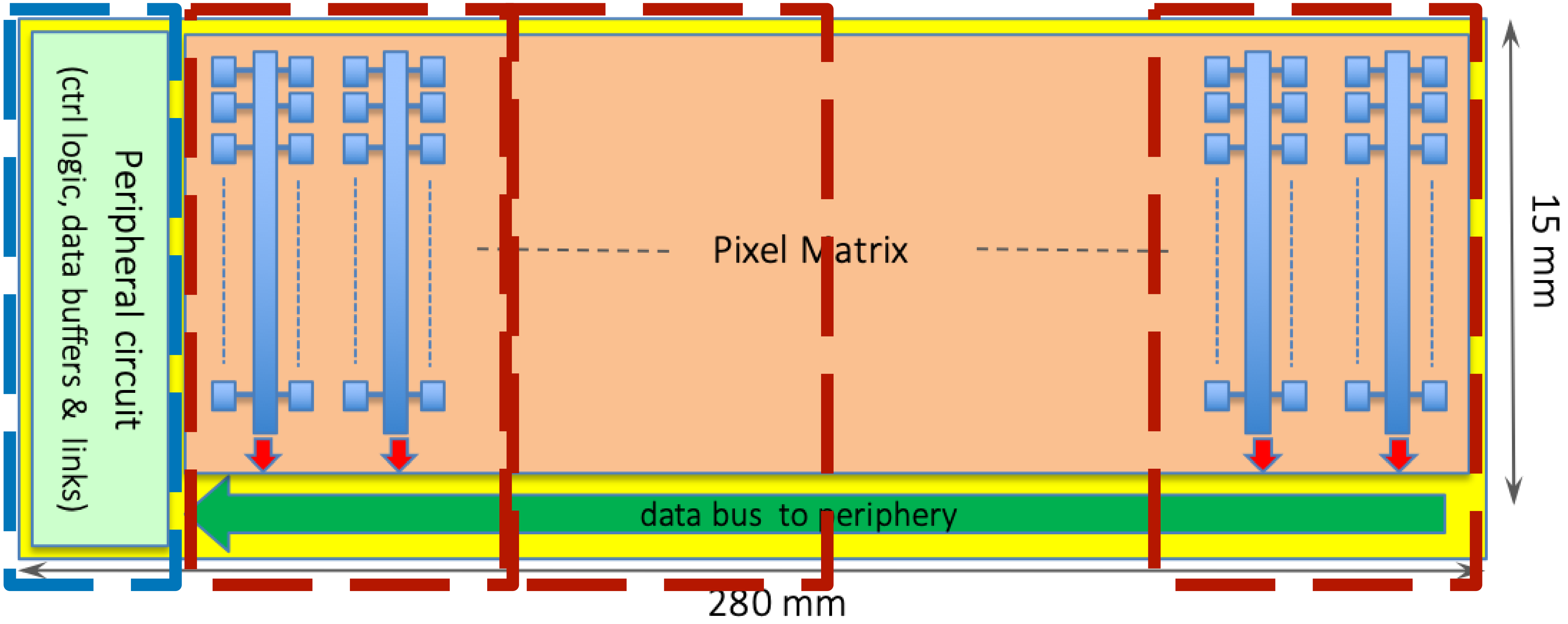
Wafer-scale sensor



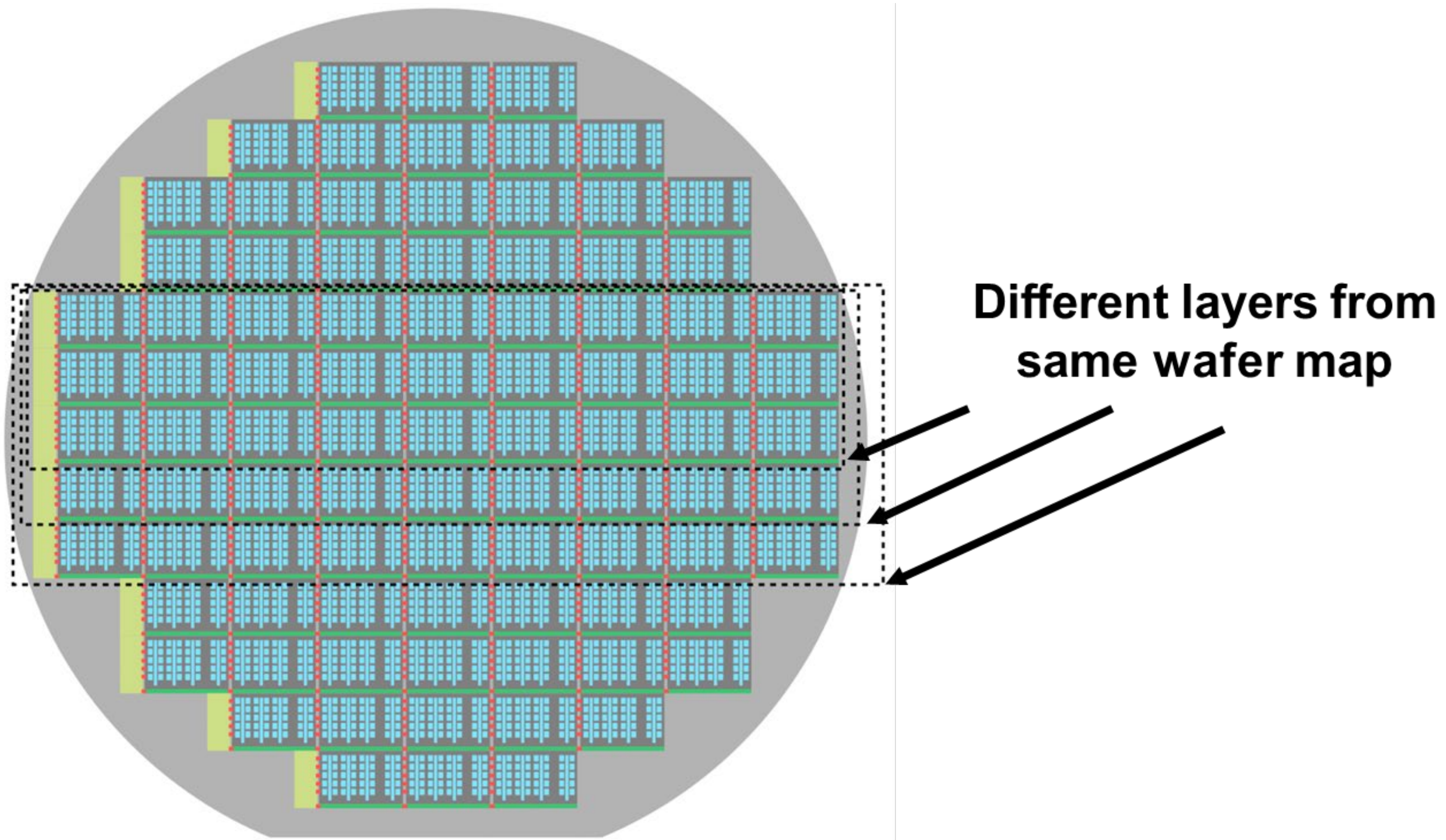
- Need to switch to TowerJazz 65 nm CMOS process ⌀= 300mm
  - ITS2/ALPIDE: TowerJazz 180 nm only available on ⌀=200mm

Wafer-scale chip: possible architecture



- Baseline: ALPIDE architecture - double column priority encoders.
- Two building blocks: periphery + pixel matrix - repeated N times in vertical direction

Wafer-scale chip: possible architecture

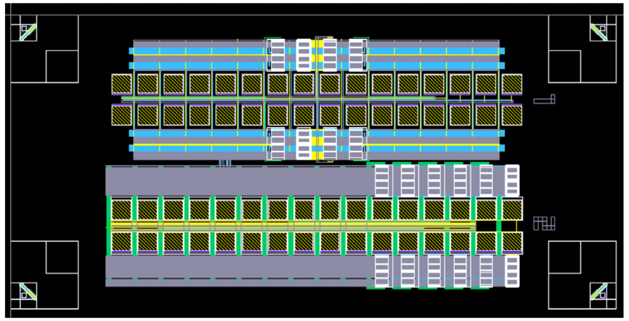


- Baseline: ALPIDE architecture - double column priority encoders.
- Two building blocks: periphery + pixel matrix - repeated N times in vertical direction

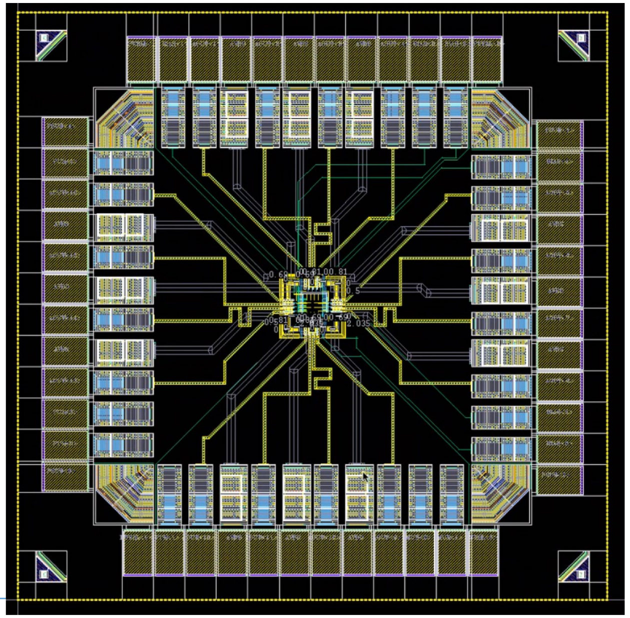
TowerJazz 65 nm process exploration

- TowerJazz 65 nm ISC technology
  - 2D stiching experience
  - 12” wafers (vs 8” mm in 180 nm)
  - Smaller feature size → smaller pixels
- First submission containing test structures
  - Transistor test structures
  - Small pixel matrices: 4x4 pixels, parallel output
  - "Large" pixel matrices: 64x32 pixels, rolling shutter
  - Bandgap, PLL, LVDS receiver prototypes
- MLR1 Submitted in Dec ‘20 – Expected back in May ‘21

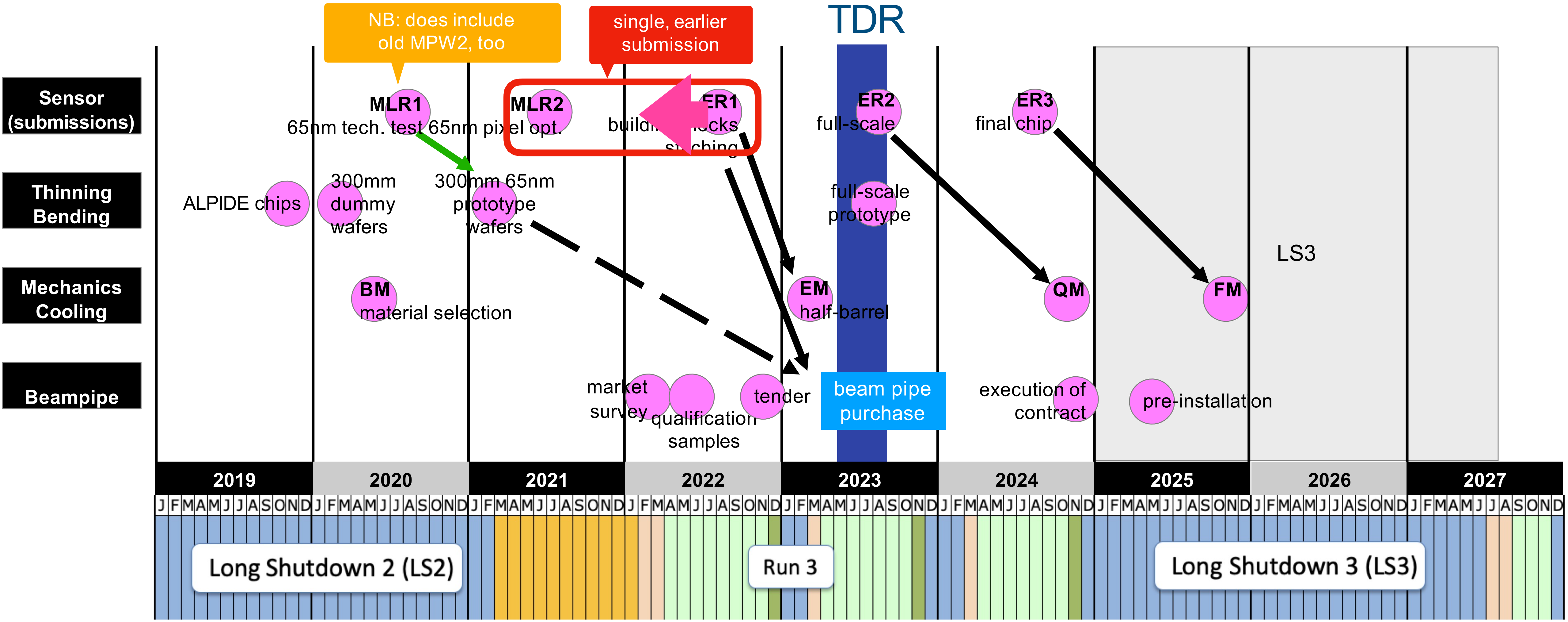
Transistor test structure



Pixel test structure

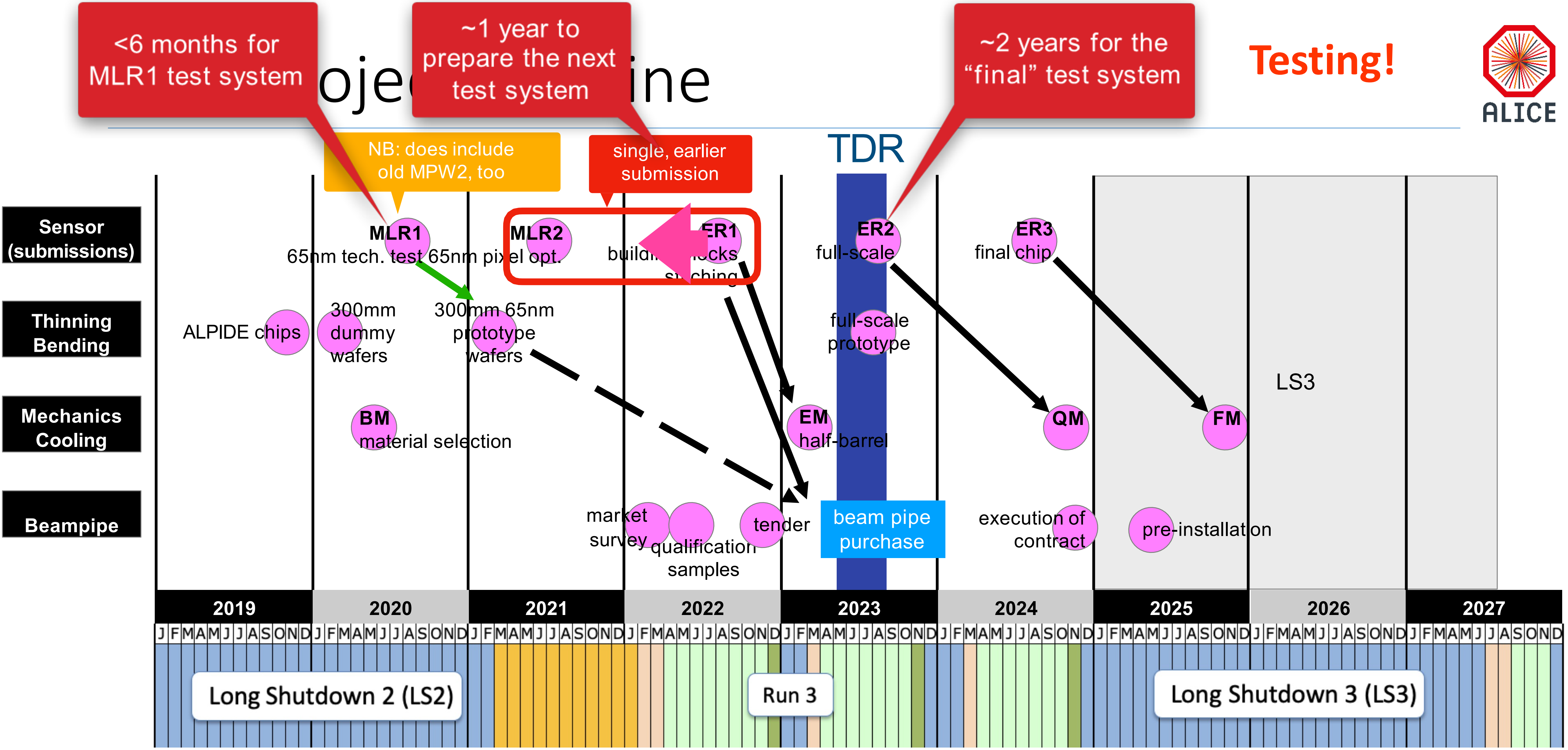


ITS3 Project timeline



MLR: multiple layer per reticle, **ER:** engineering run,

BM: breadboard module, **EM:** engineering module, **QM:** qualification module, **FM:** final module



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Testing of MLR1 pixel matrices

In 6 months and for ~1 year

- Short time to prepare the test system and short usage time
  → avoid custom solutions

- Provide feedback for ER1 quickly → distribute the characterisation workload

- **Solutions**: a “proximity board” (+ potentially “carrier card”) +
  - Existing test system, or
  - General purpose components (oscilloscopes, dev boards…)

- **To keep in mind:**
  - Testbeams, bending tests, irradiation, yield…
  - >100 chips on “carrier card”/“proximity boards” & ~20 test systems

A large variety of samples to test in a very short time!

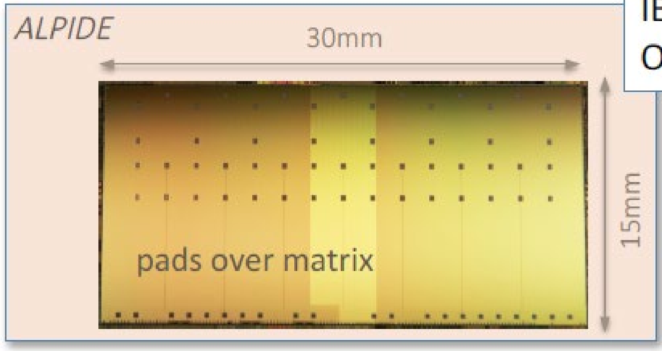
Curved silicon: does it even work?

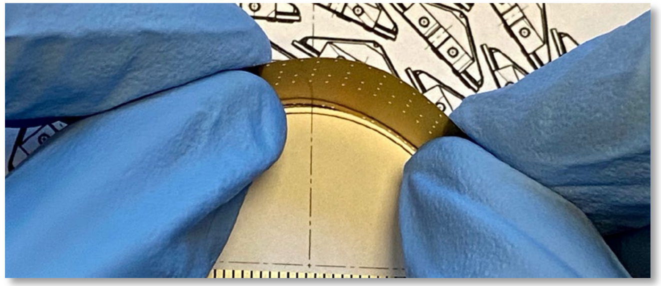
Curved silicon: does it even work?

We started from what we had available:

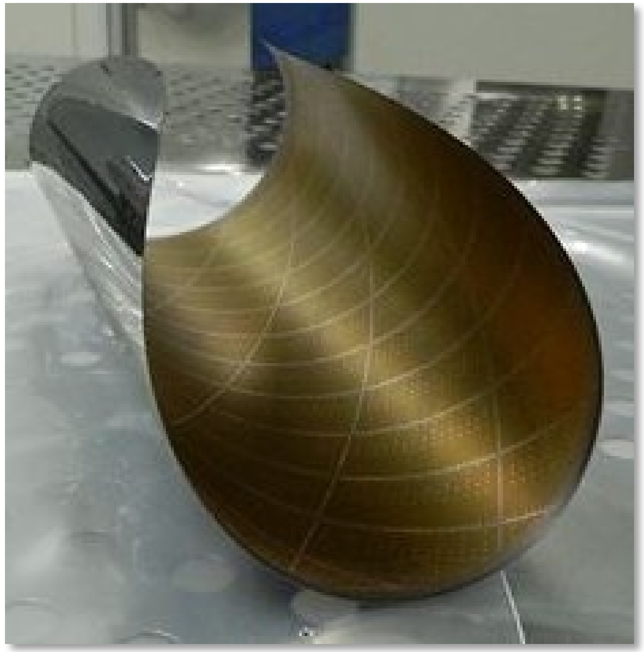
ALPIDE chips

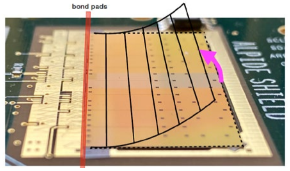
IB: 50μm thick
OB: 100μm thick





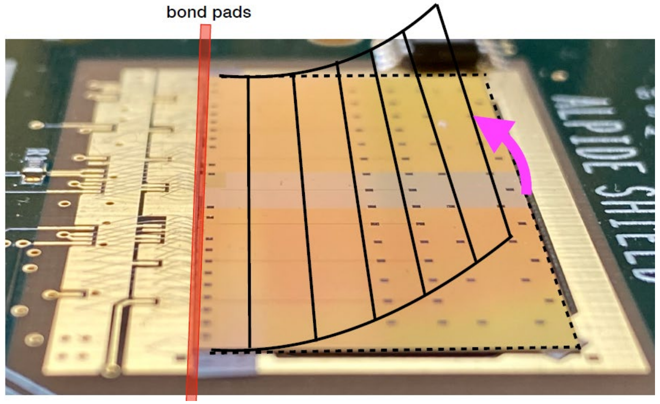
ALPIDE wafers

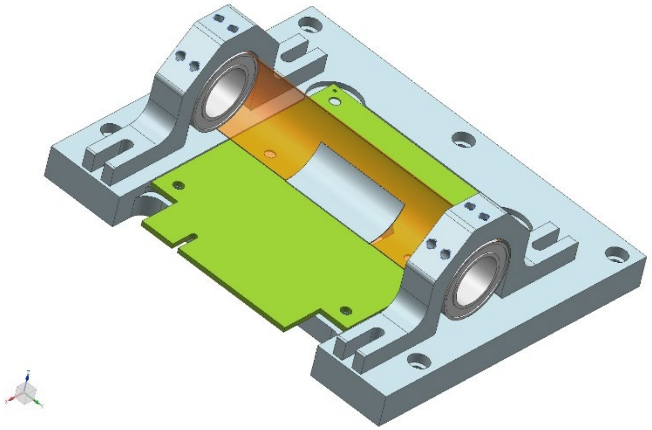


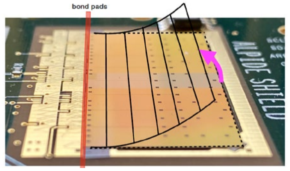


How to bend a 50 µm thick ALPIDE? - 1

- **Along the short side**
  - Bending affects pixel matrix only
  - Bonding area is glued: flat and secured
  - Variable curvature (down to 1 cm radius)







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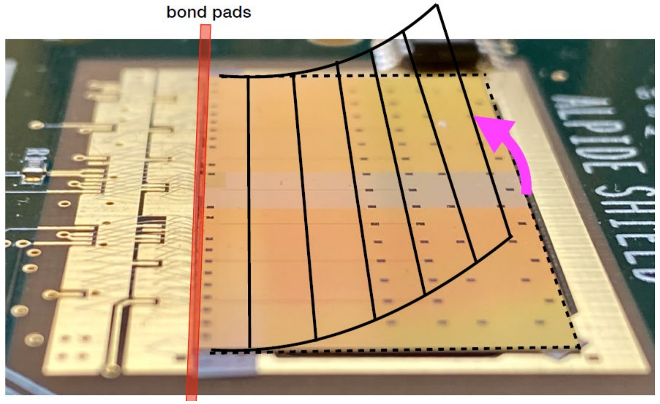
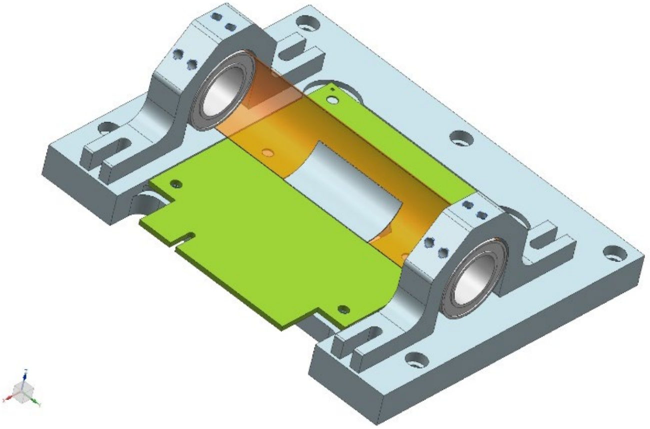
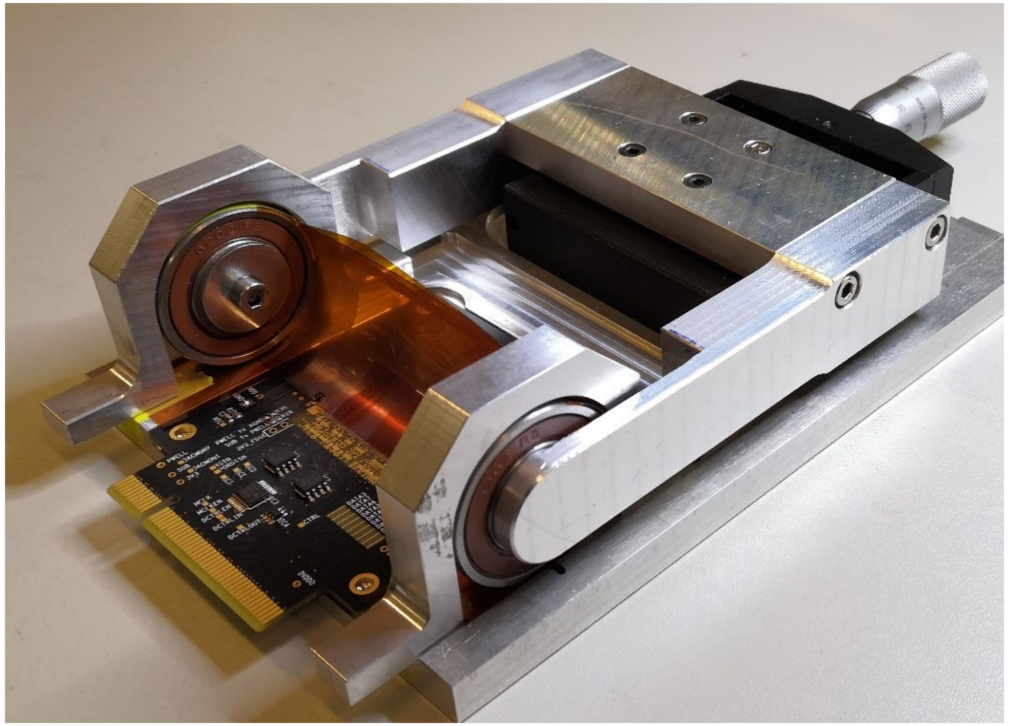
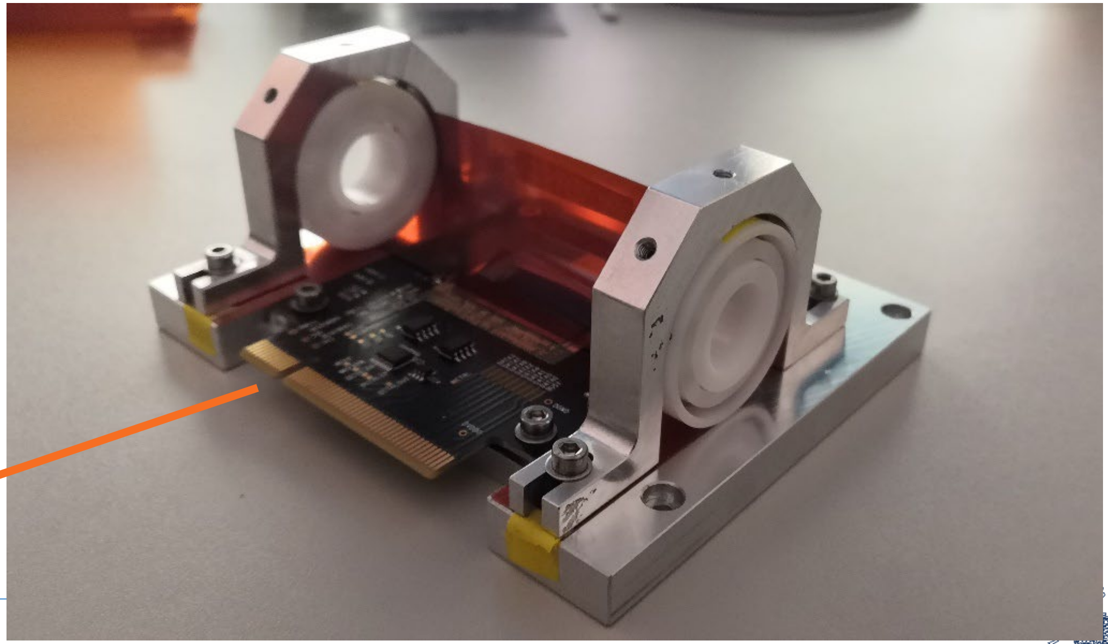


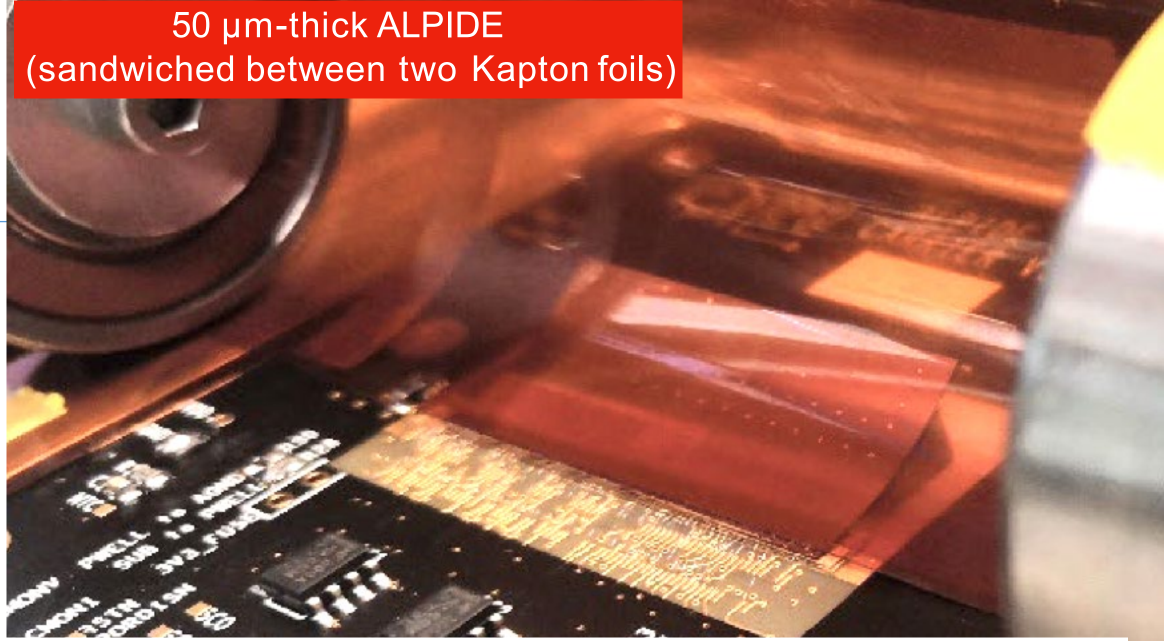




Single chip DAQ board



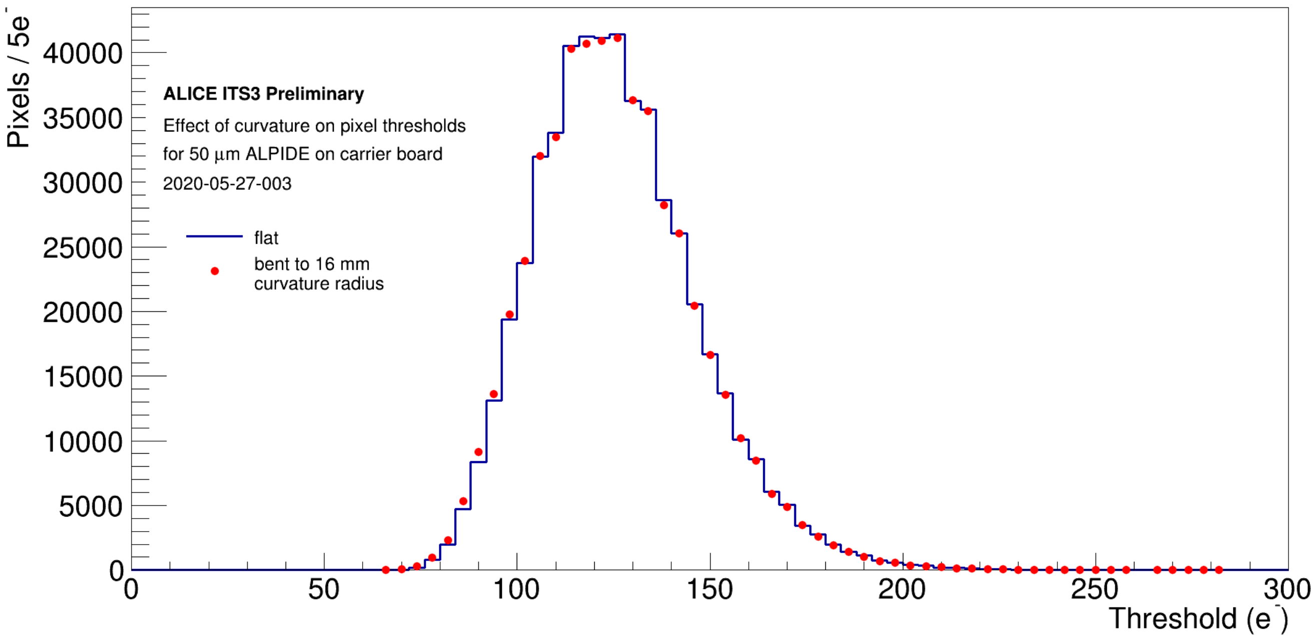
Bent chip electrical tests



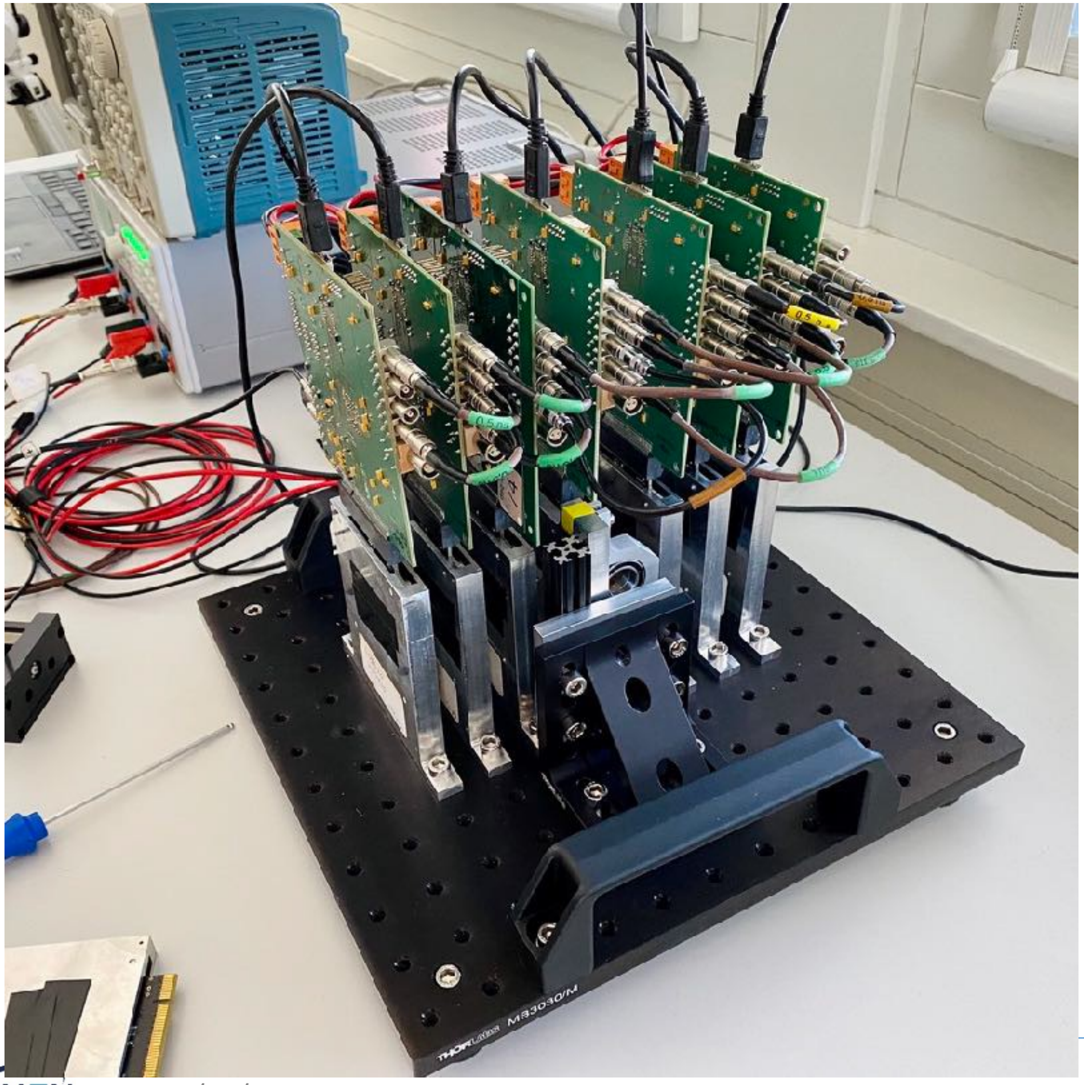
- Laboratory tests to characterize bent ALPIDEs in terms of thresholds and fake-hit rate
  - different set-ups are tried
  - experience on handling is gained

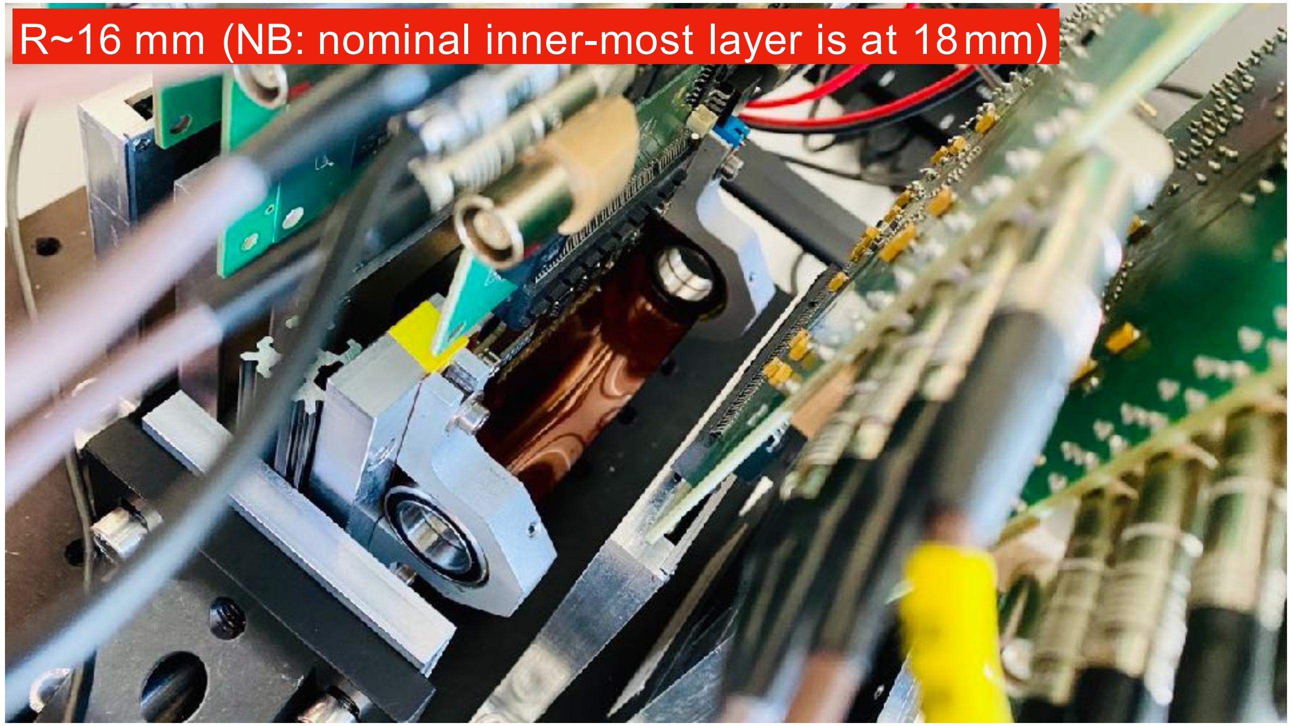
- The curvature effect is not noticeable on:
  - pixel thresholds, FHR, pixel responsiveness
  - tested down to below nominal bending radius

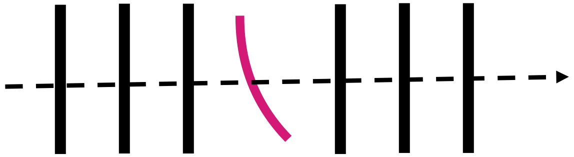
- Multiple chips successfully installed and tested in lab, 2 of them sent to DESY for testbeam



Bent chip in ALPIDE-based beam telescope





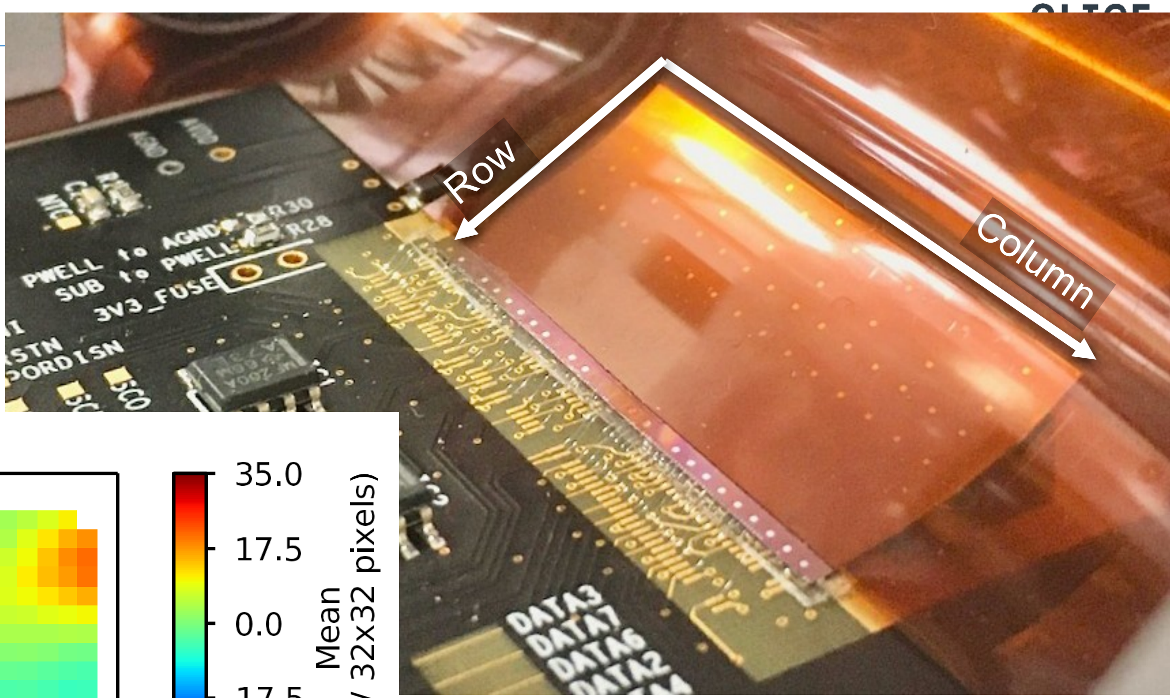


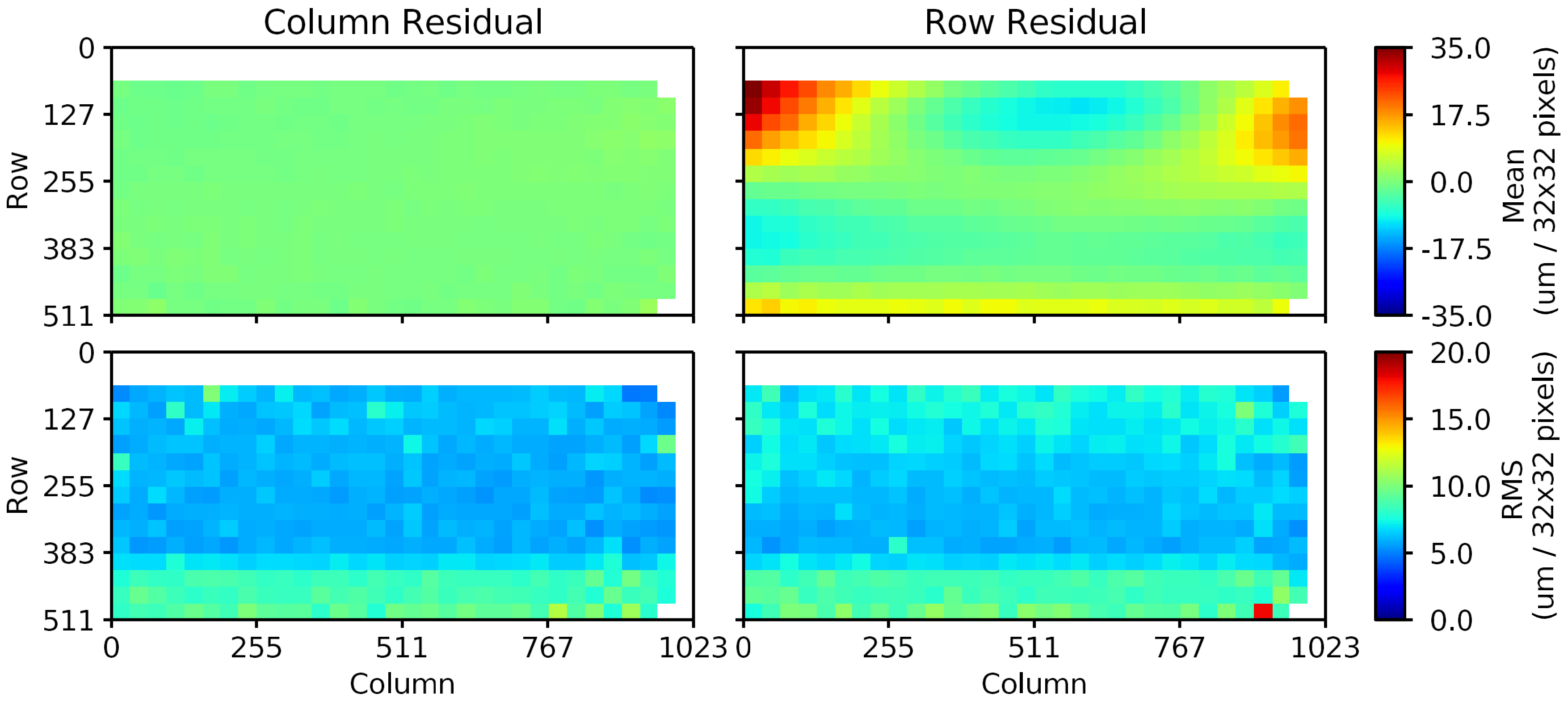
+ 2nd chip at R~18 mm

Mar '20 Testbeam analysis: residuals

Mean of the residuals:

- Column direction - invariant to rotation around column axis
- Row direction - compatible with cylindrical geometry model up to 35 μm

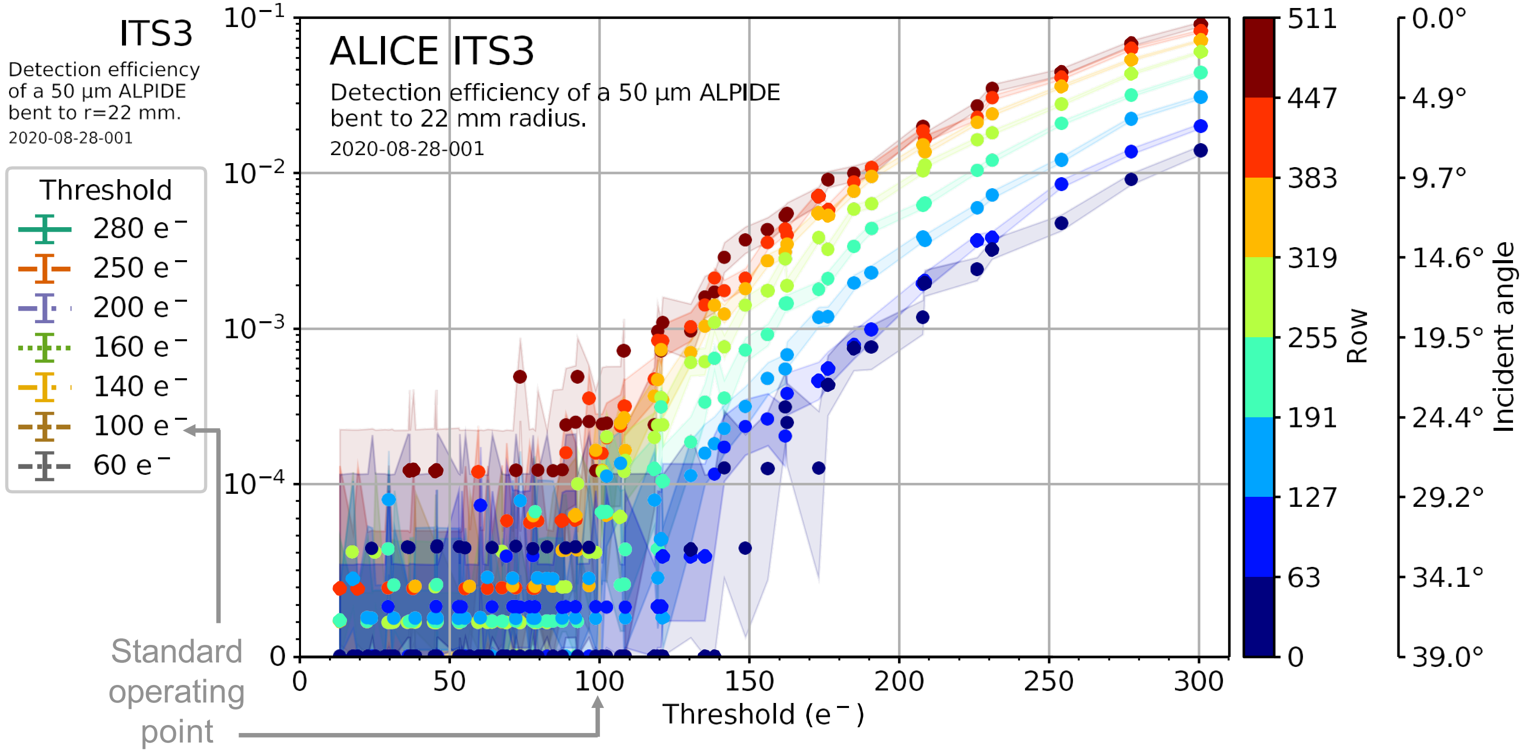




RMS of the residuals:

- Higher where chip is glued to carrier card due to scattering
- Row direction - increases with the incident angle of the beam

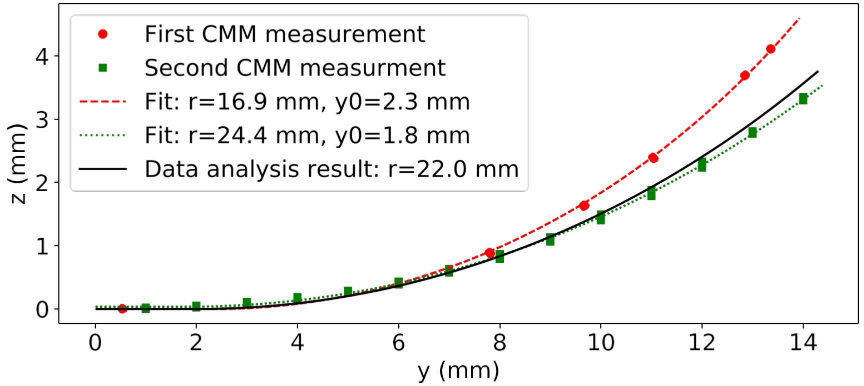
Mar '20 Testbeam analysis: detection inefficiency

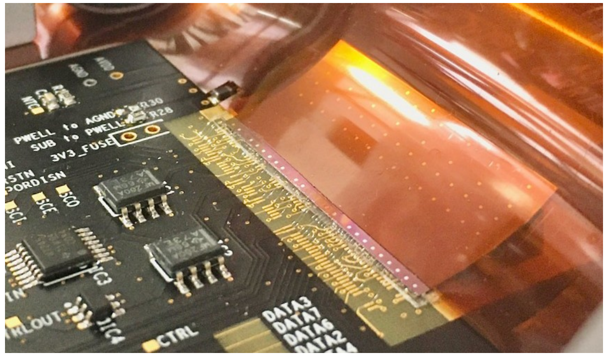


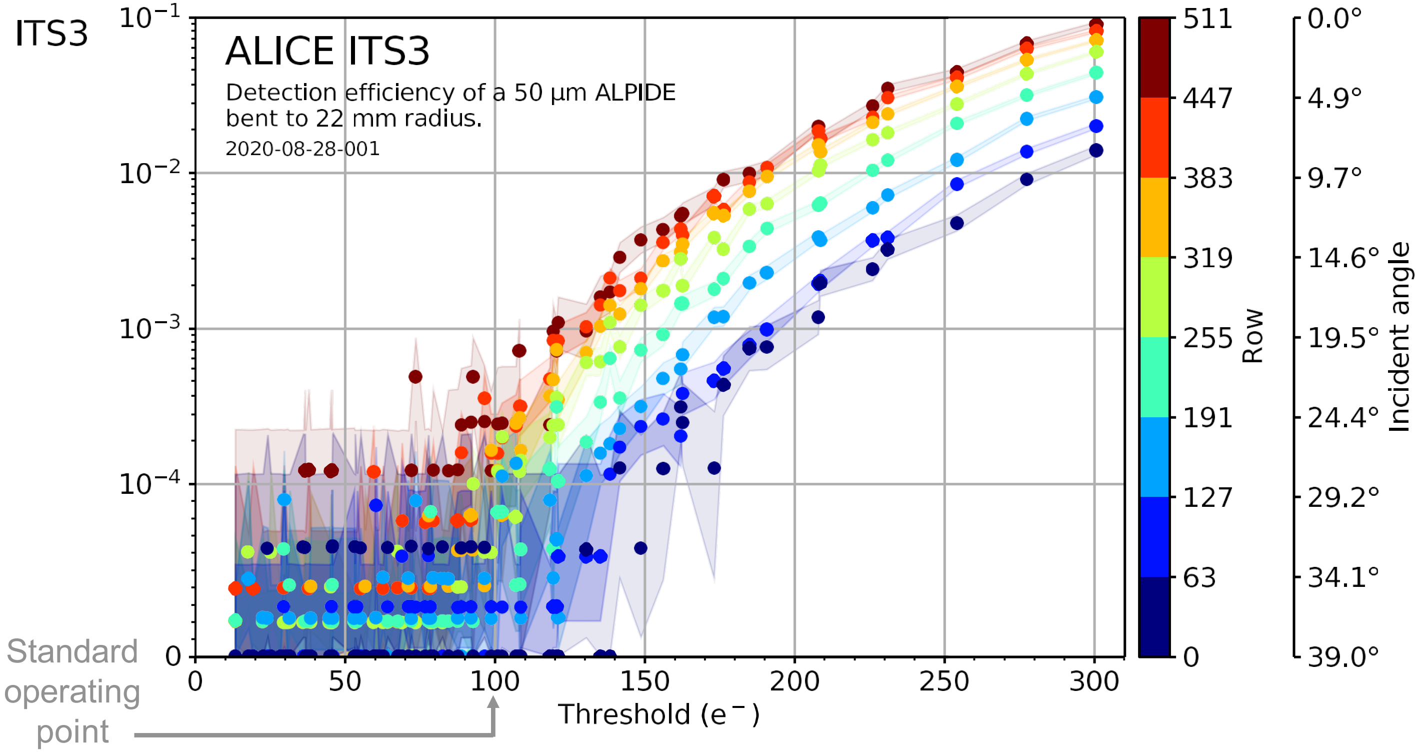
- Below a threshold of 100 e-, inefficiency is generally lower than 10^{-4}
- Above 100 e-, the inefficiency increases with decreasing beam incident angle (increasing row number)

Mar '20 Testbeam analysis: detection inefficiency

- Curvature measurements







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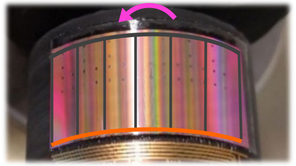
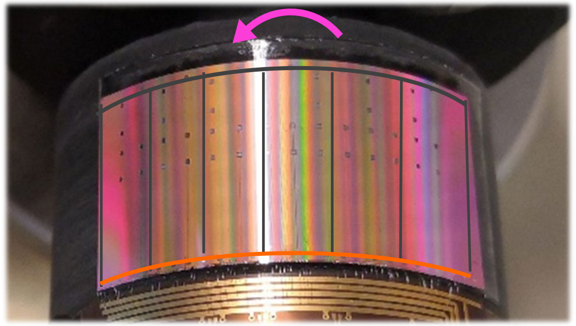
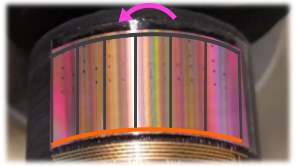


How to bend a 50 µm thick ALPIDE? - 2

- **Along the long side**
  - Affecting matrix and periphery
  - Stretches the CMOS circuitry
  - Completely glued onto support
  - Fixed curvature (1.8 cm radius)



- Needs a custom setup to interconnect the curved chip after bending



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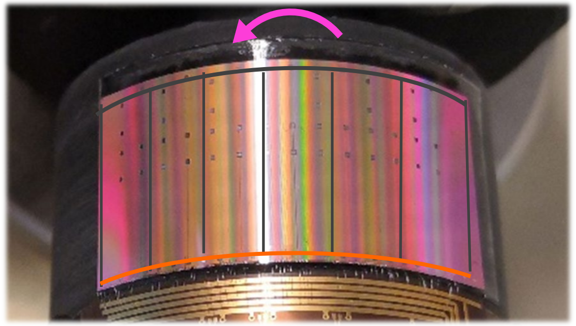
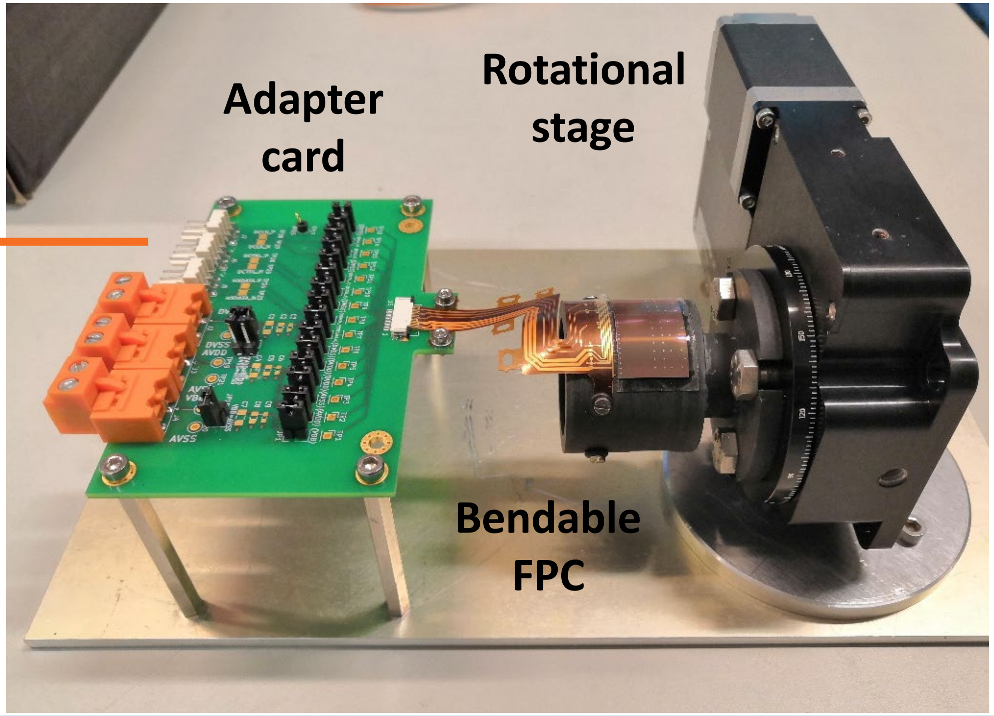
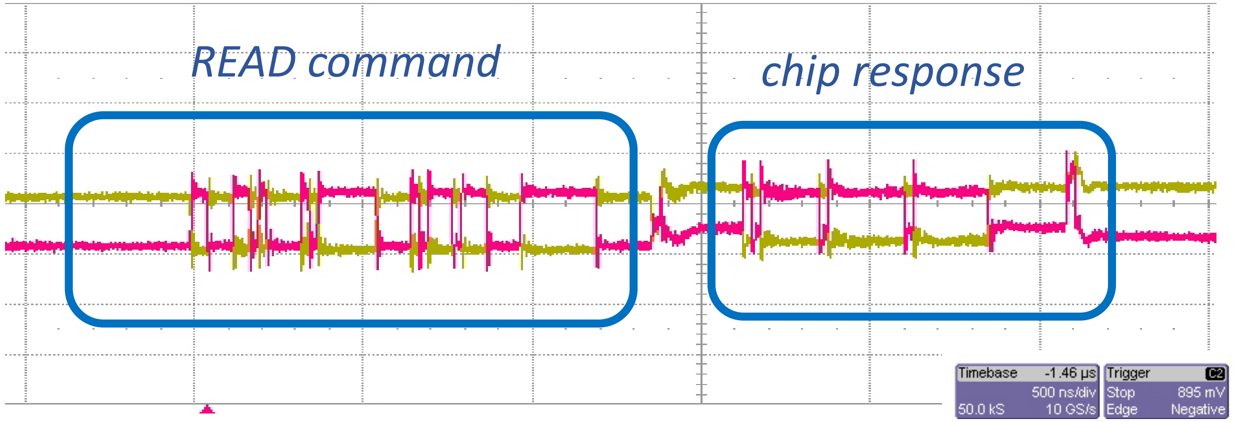


- Needs a custom setup to interconnect the curved chip after bending
- I-V and response immediately checked after interconnecting the chip: works

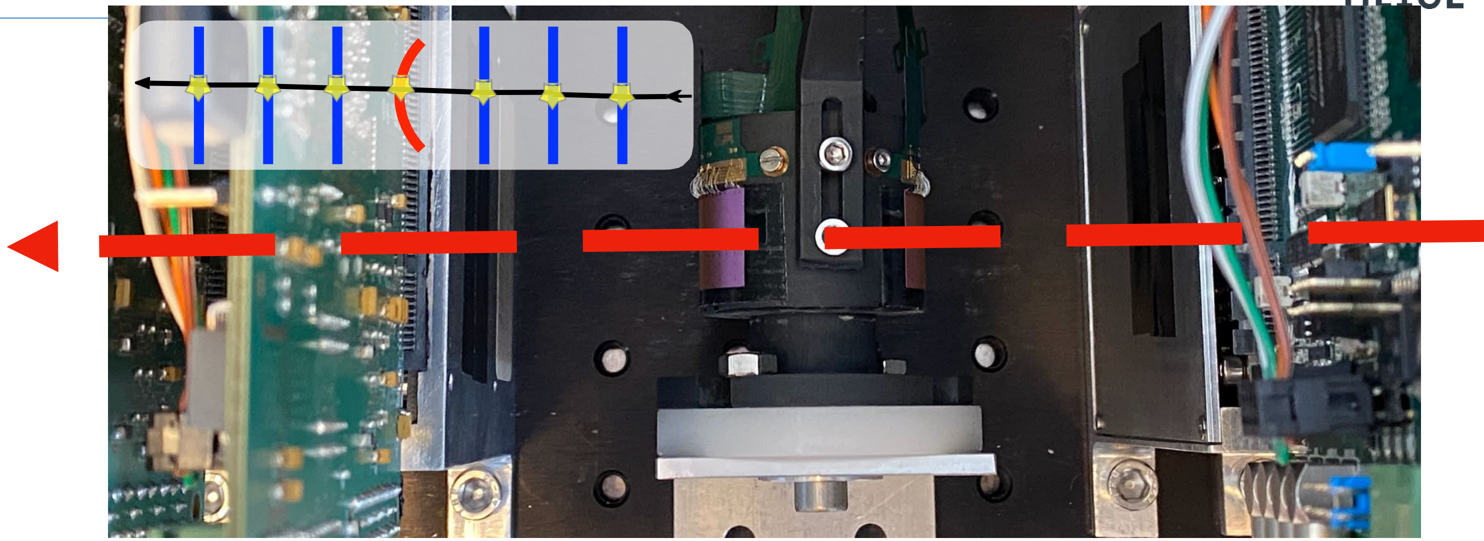




- >10 chips successfully bent and tested.
- Handling is delicate but feasible

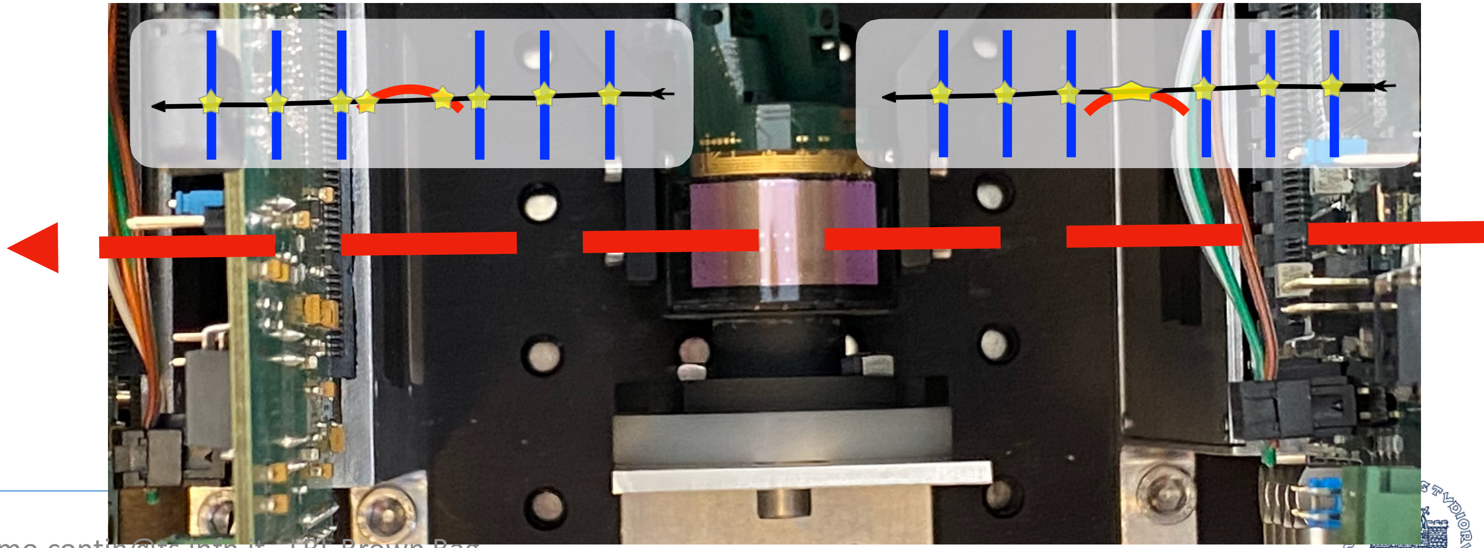
Aug ’20 Testbeam

“ordinary”



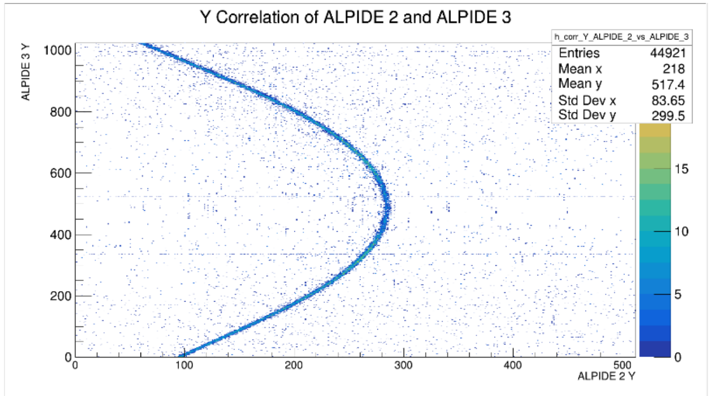
double-crossing

grazing



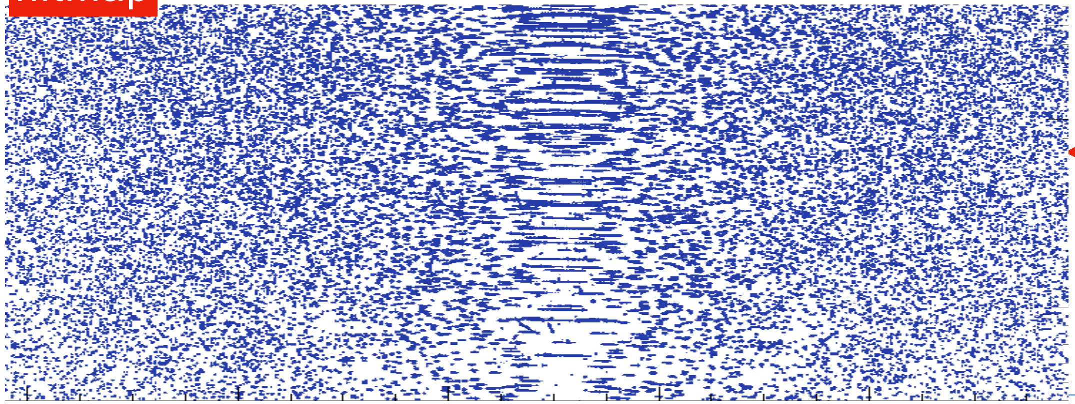
Aug ’20 Testbeam

Online monitoring
Correlation bent chip – reference plane

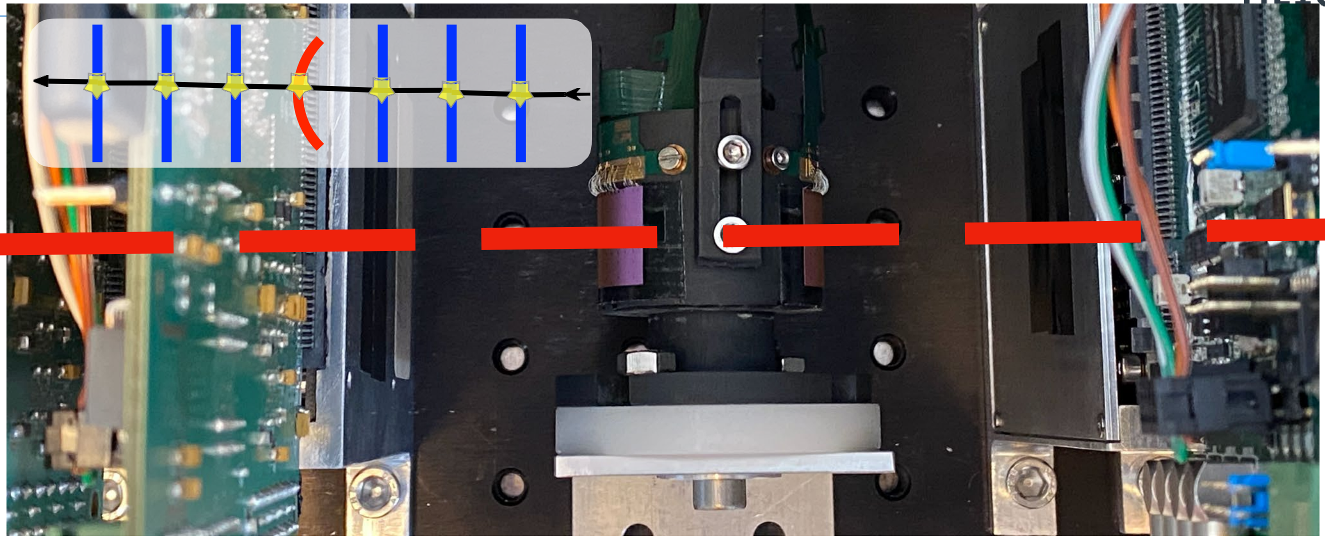


- Analysis ongoing

hitmap

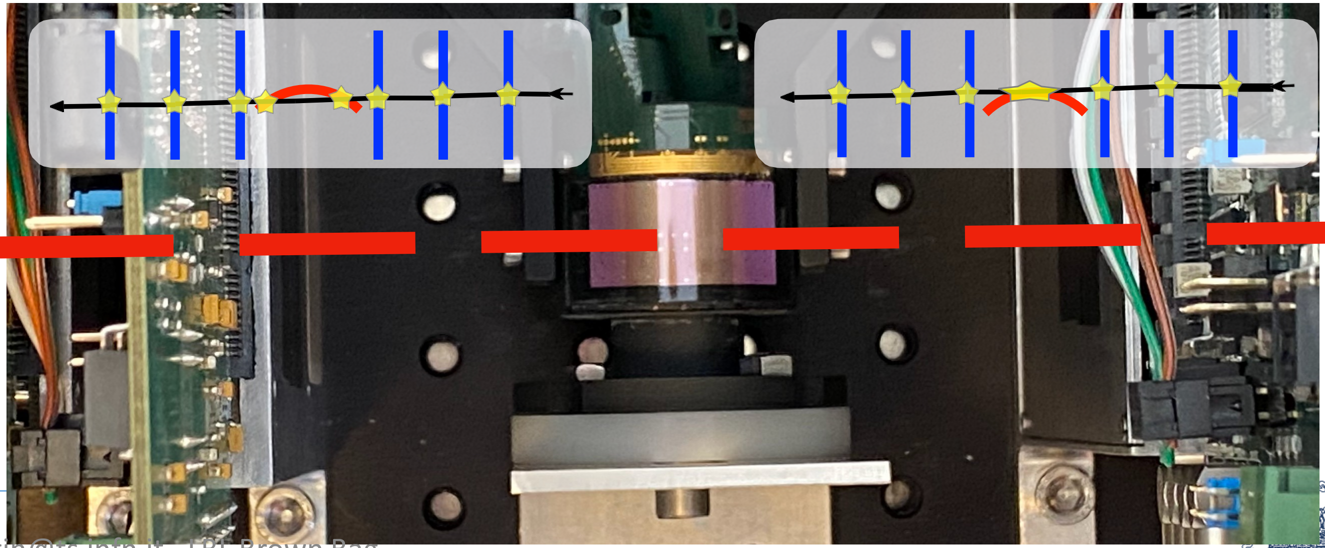


“ordinary”

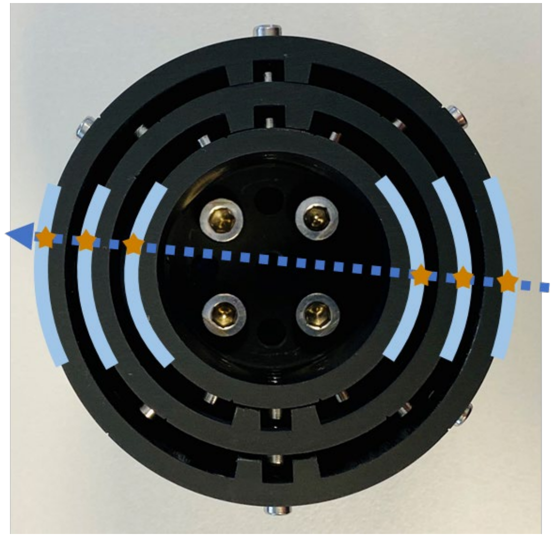


double-crossing

grazing

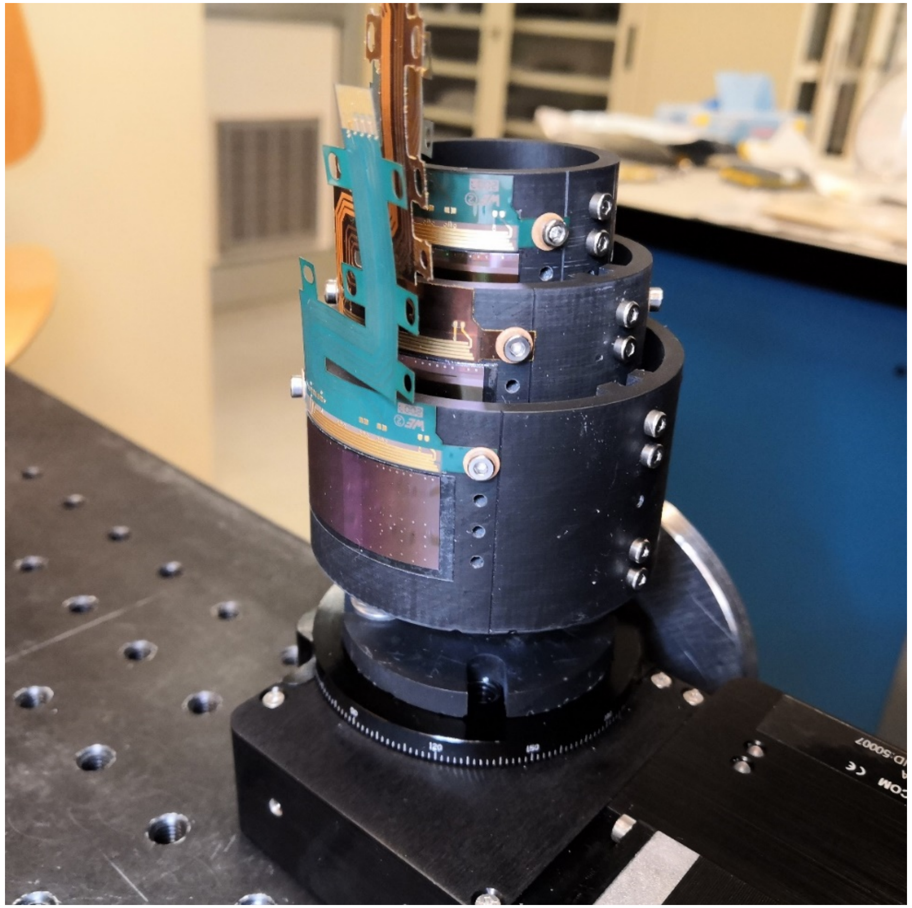


2021 Testbeam plans



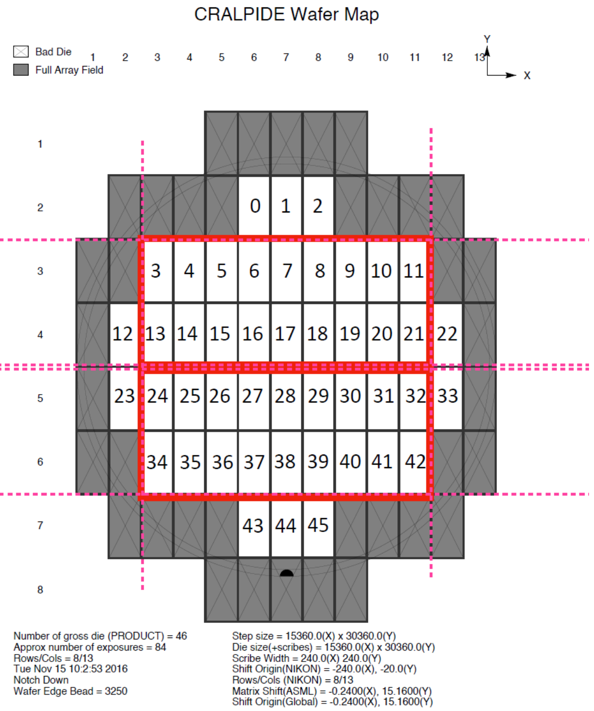
Several Testbeams planned for:

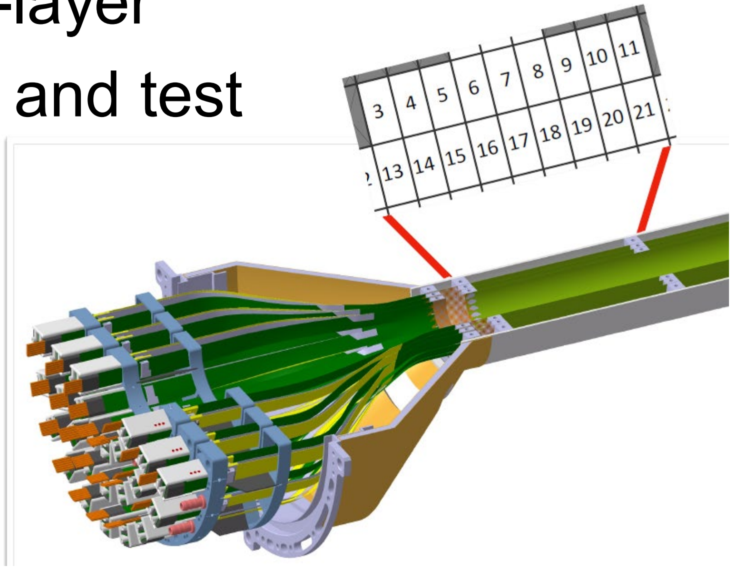
- µITS3 (6 bent chips, various radii)
- Different interconnection technologies
- New MLR1 test structures
- Large-area ALPIDE-based Superchip

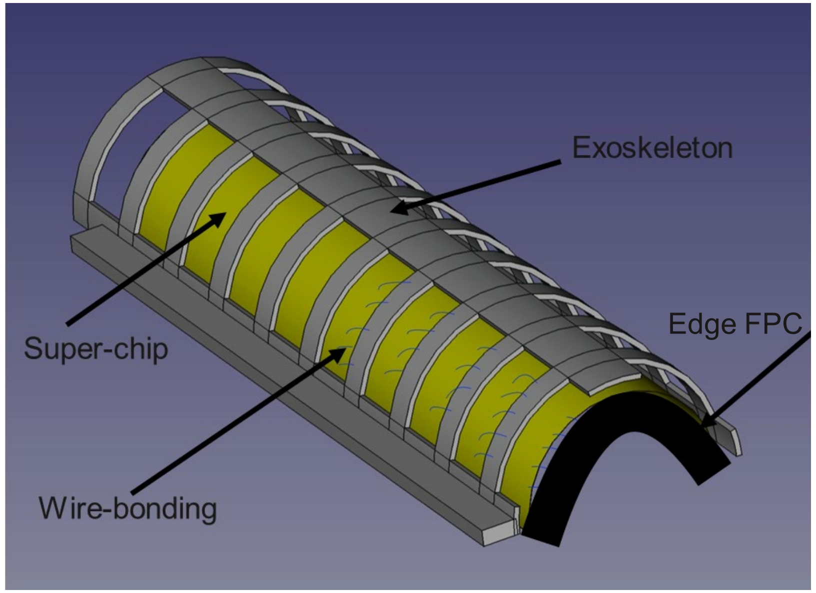


Moving to a larger size: ALPIDE Super-chip

- Idea: cut out large “super chips” from a wafer (140x60 mm^2)
- Matching the size of 1/2 ITS3 half-layer
- 9 x 2 chips to interconnect, power and test
- Thinned down to 30-40 μm







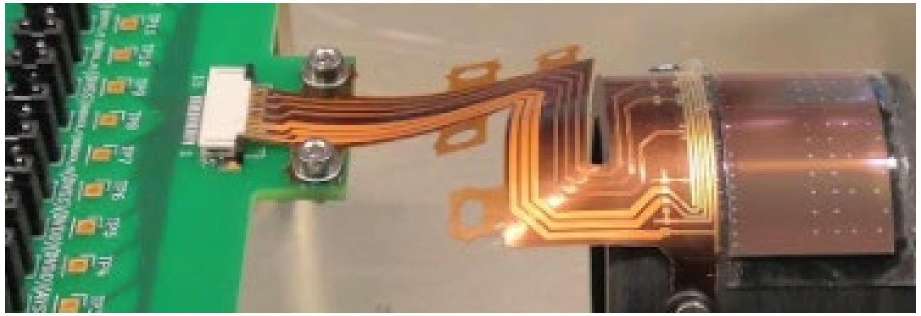
Wire-bonding based interconnections for the first 2 chips

- Toward the final chip configuration: only end-of-chip

@UniBA - PoliBA - INFN

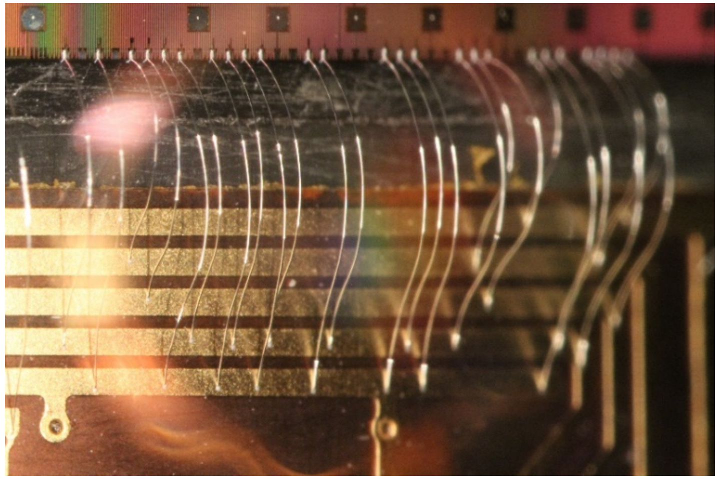
Bent silicon interconnections: wire-bonding

- **Wire-bonding** after bending



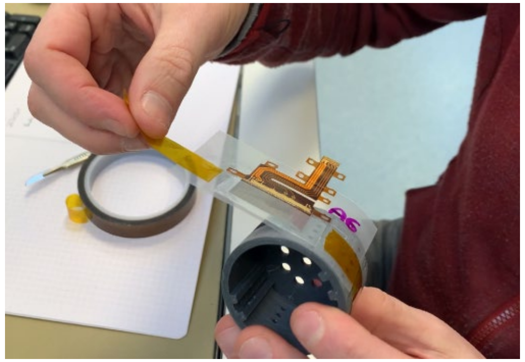
Bent ALPIDE, wire-bonded to bendable FPC, connected to interface card

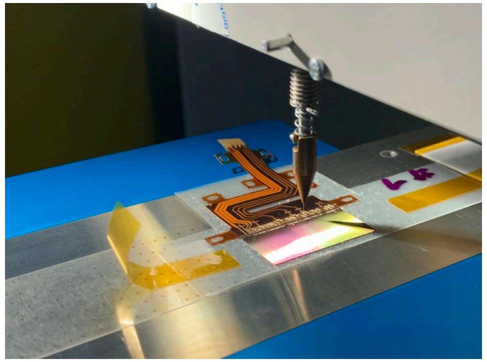
Bent ALPIDE, wire-bonded



- **Bending after wire-bonding** (reversible)
  - Useful for validating the mechanical stability
  - Bent around a cylinder and reverted flat
  - Satisfactory pull-test after multiple bending
  - Chip still alive and communicating

@IPHC

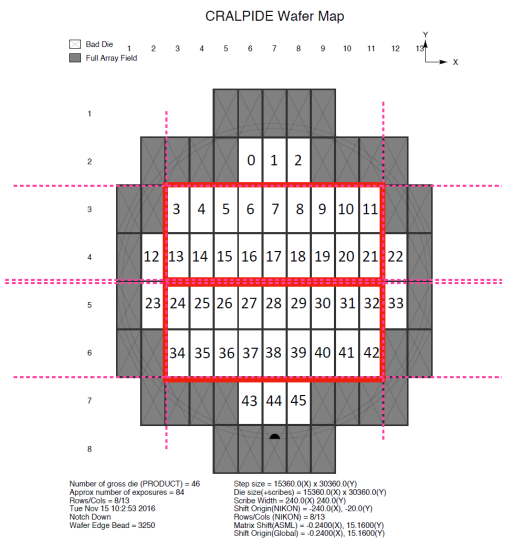


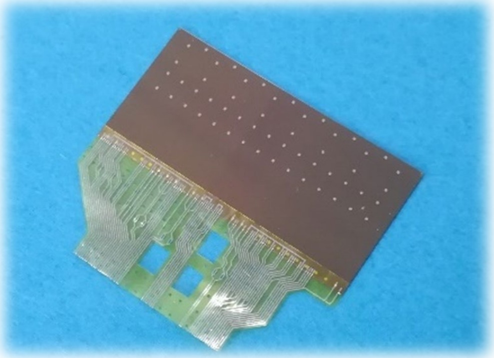


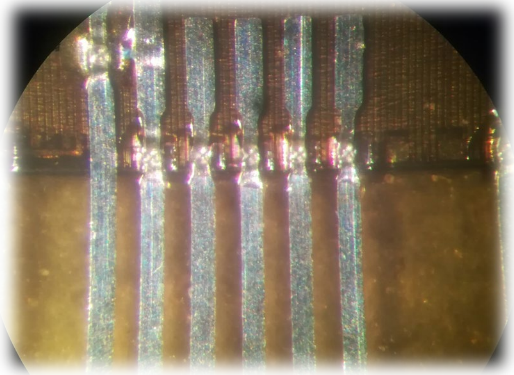
Bent silicon interconnections: SpTAB

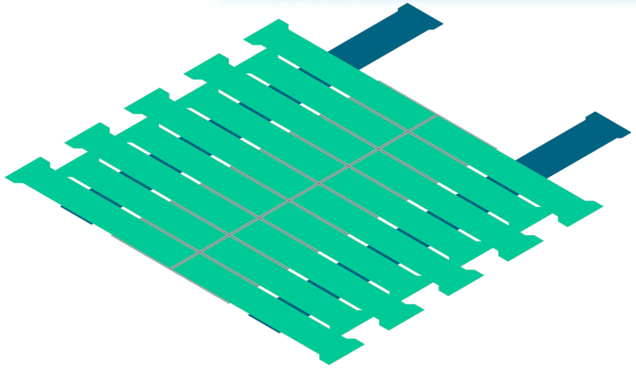
- **Bending after SpTAB bonding**
  - Easily allows for bending in different directions
  - Doesn't need mechanical support

ALPIDE, SpTAB bonded to microcable





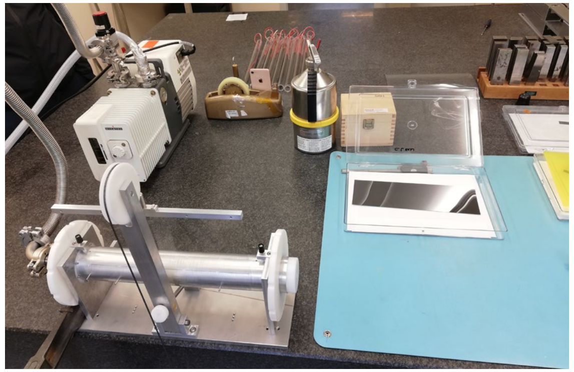


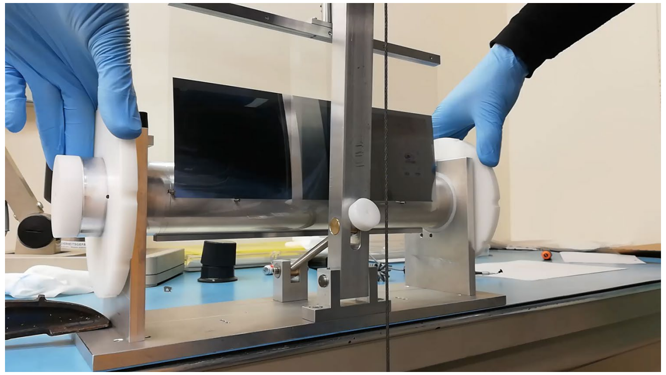


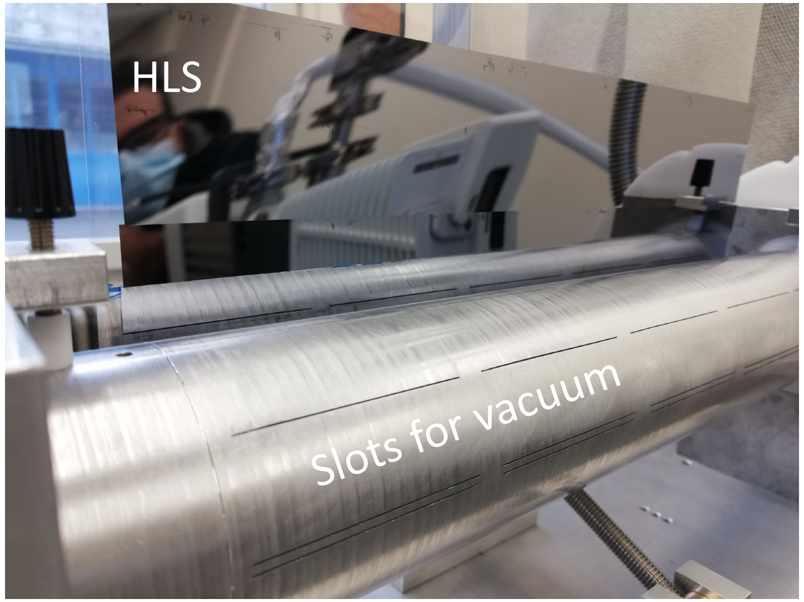
- ALPIDE Super-chip SpTAB bonding is under development

@LTU-Bergen-USN

Towards the Engineering Module





- Half Layer Sensor wrapped around the vacuum chuck
- Held in position by vacuum + mylar layer
  - At the moment the vacuum is not enough to hold 50um large chip

EM: Engineering Model 1

- Feasibility studies: carbon foam wedges placed and glued on silicon and on exoskeleton

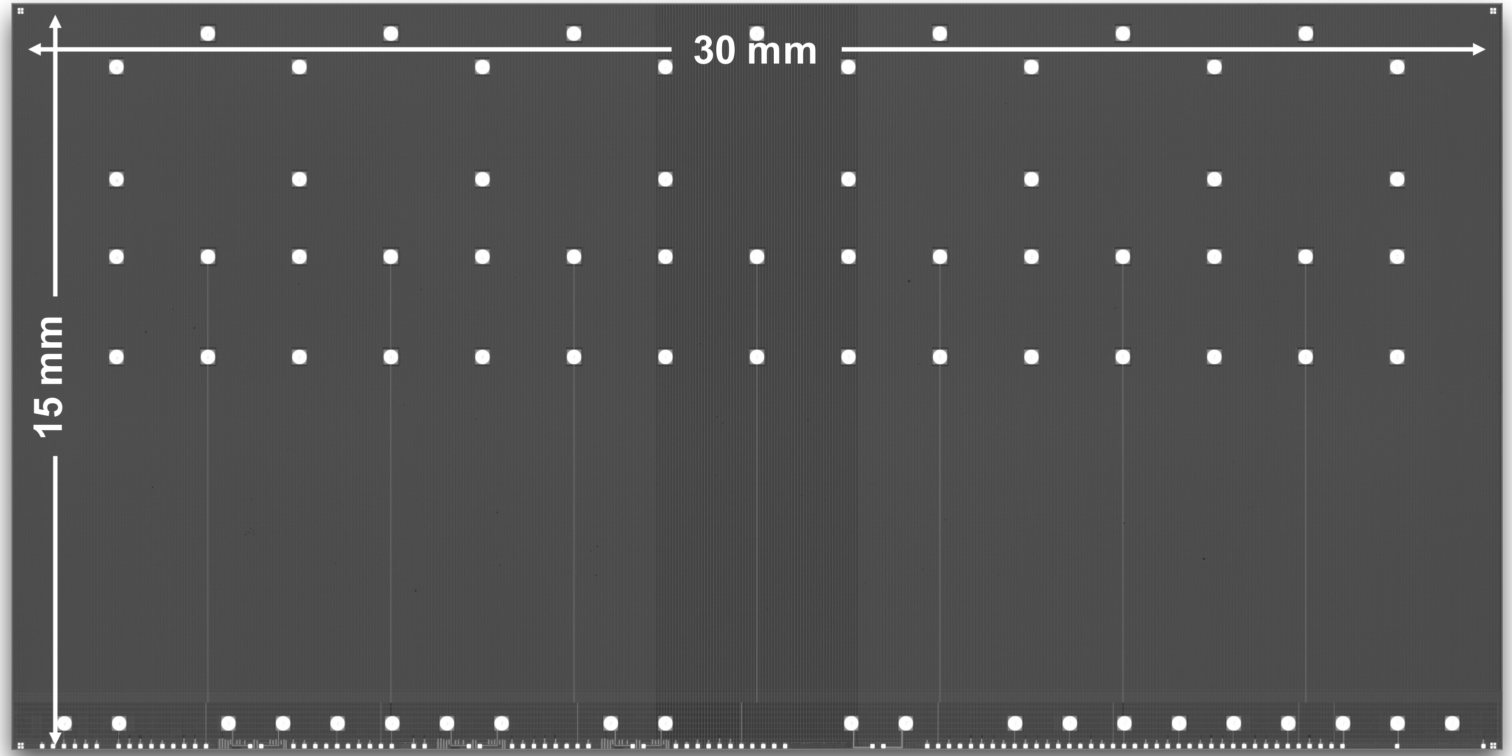
Dummy Silicon Half Layer Sensor
280mmx93.2mmx40 µm

Carbon foam wedge: ERG Duocel
[0.06 kg/dm^3]
Carbon fleece
[8g/m^2]

Araldite 2011

Cooling

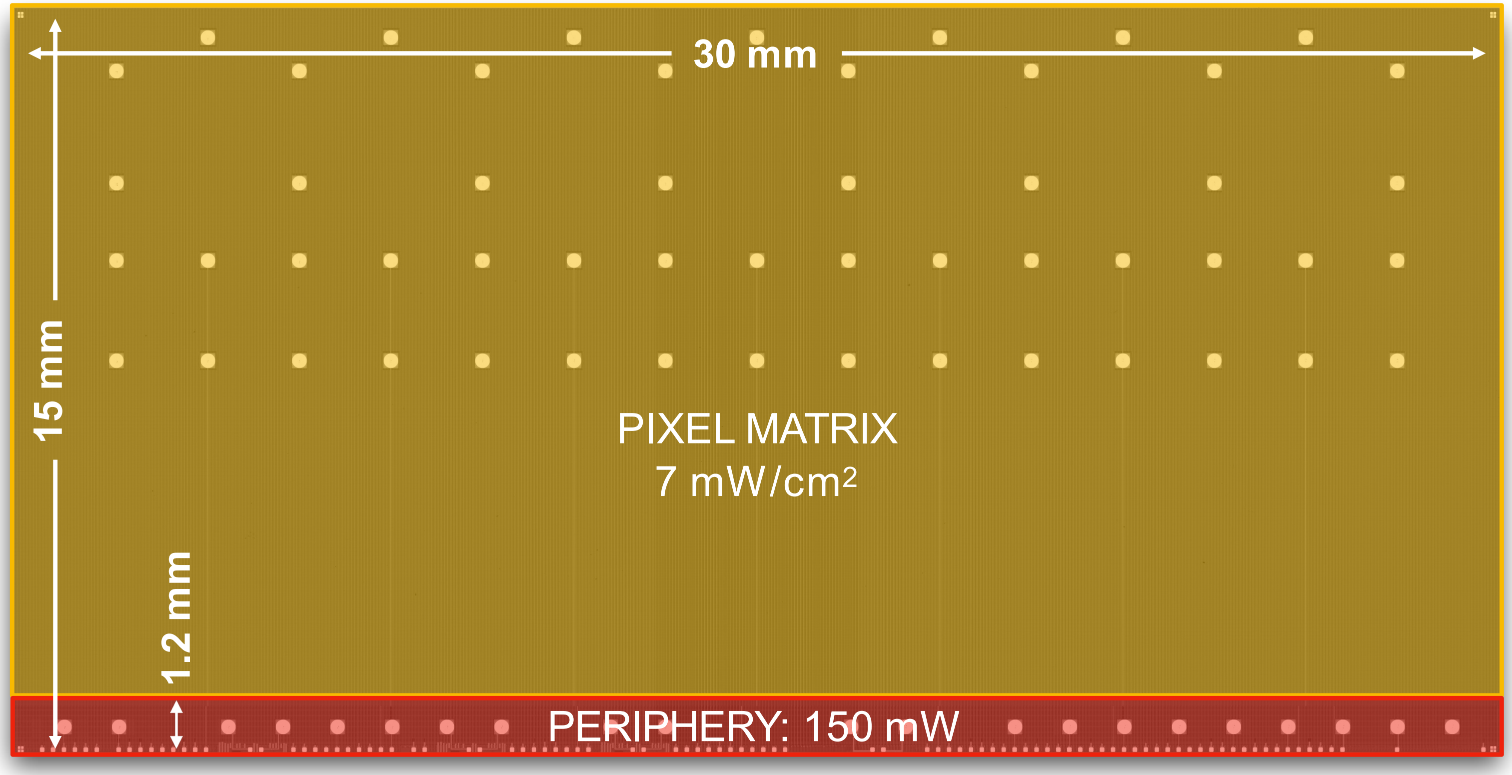
ALPIDE - the MAPS for the ITS2



- Air cooling possible as from ~20 mW/cm²
- ALPIDE already close: ~40 mW/cm²

Cooling

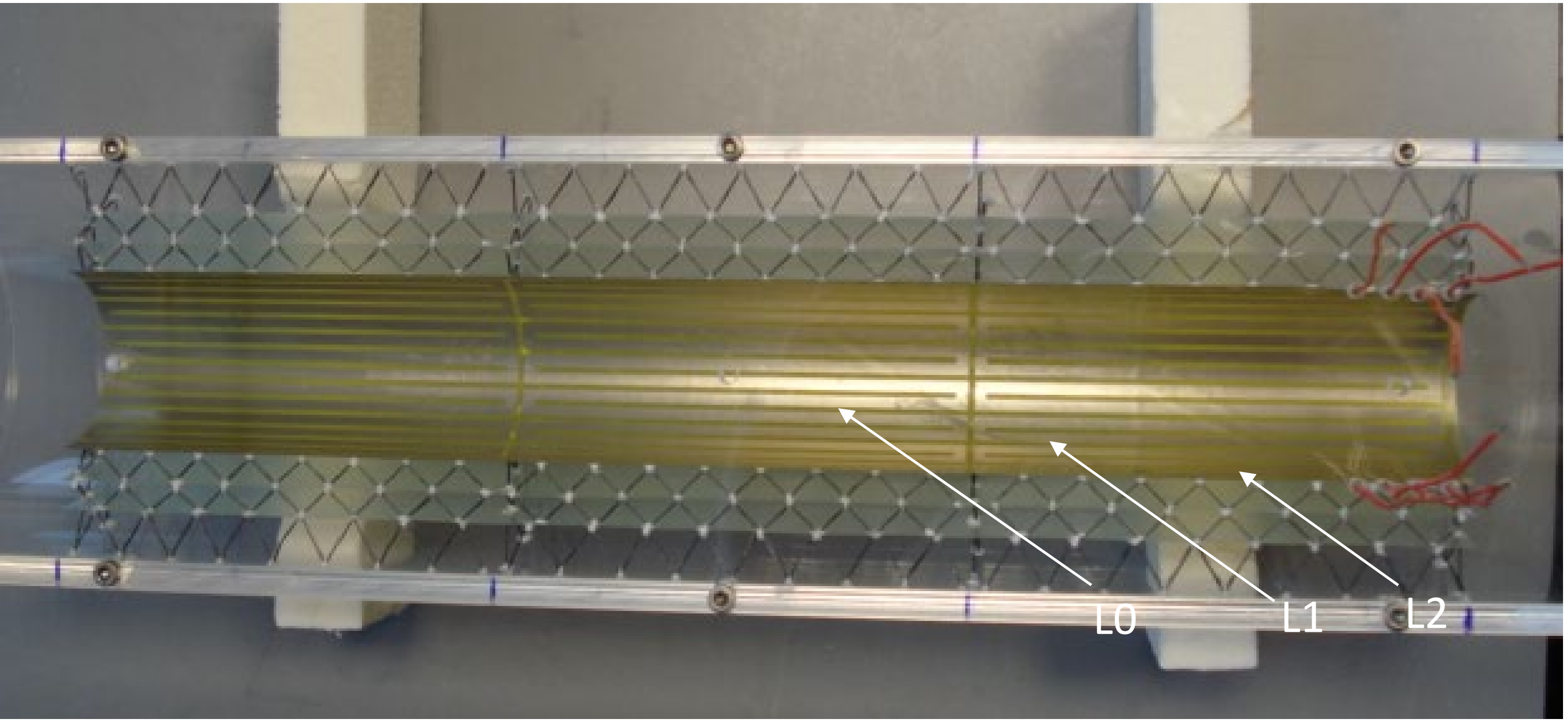
ALPIDE - the MAPS for the ITS2

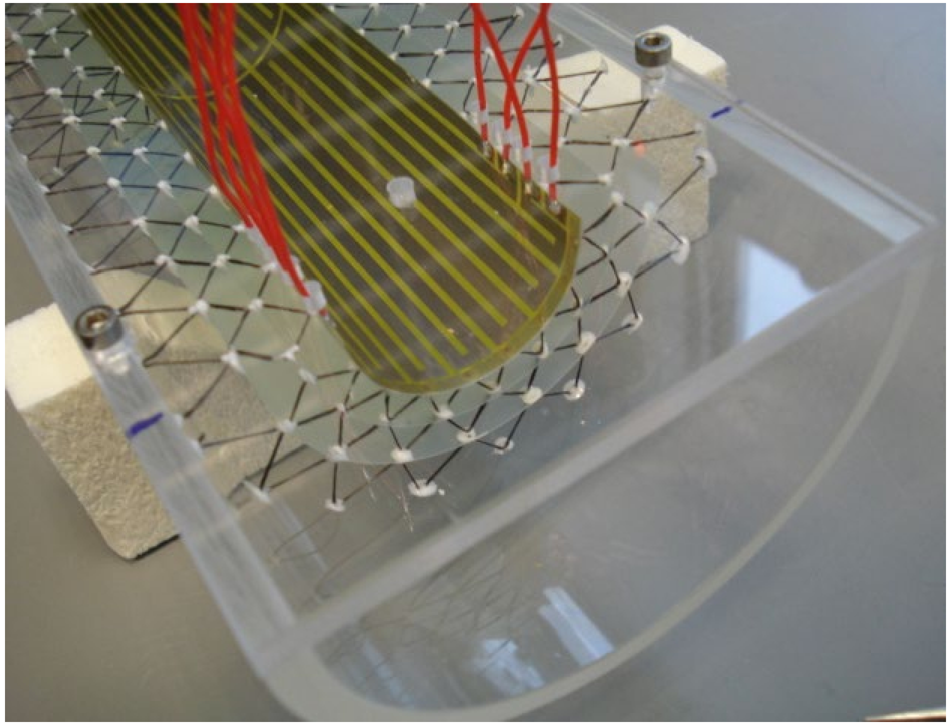


- Air cooling possible from ~20 mW/cm^2
- ALPIDE already close: ~40 mW/cm^2
- actually largely sufficient if periphery outside fiducial volume

Breadboard Model: dummy HLS with glued heaters

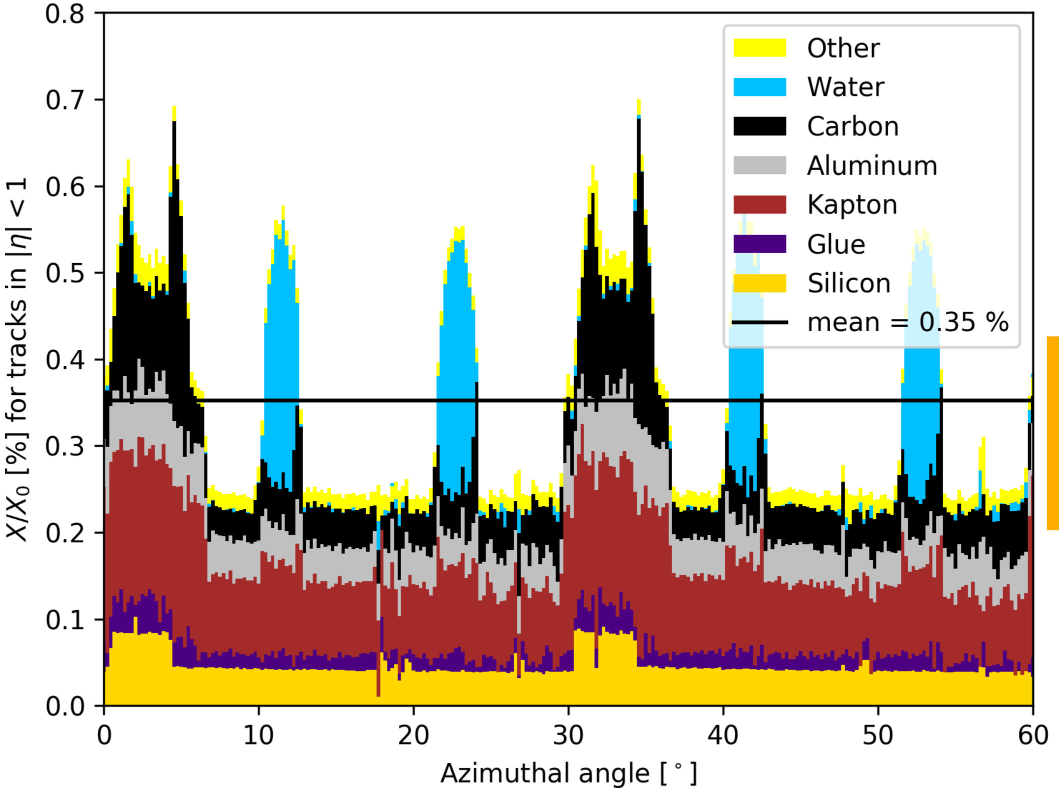
- Dissipated heat simulated by Foil heaters for thermal test





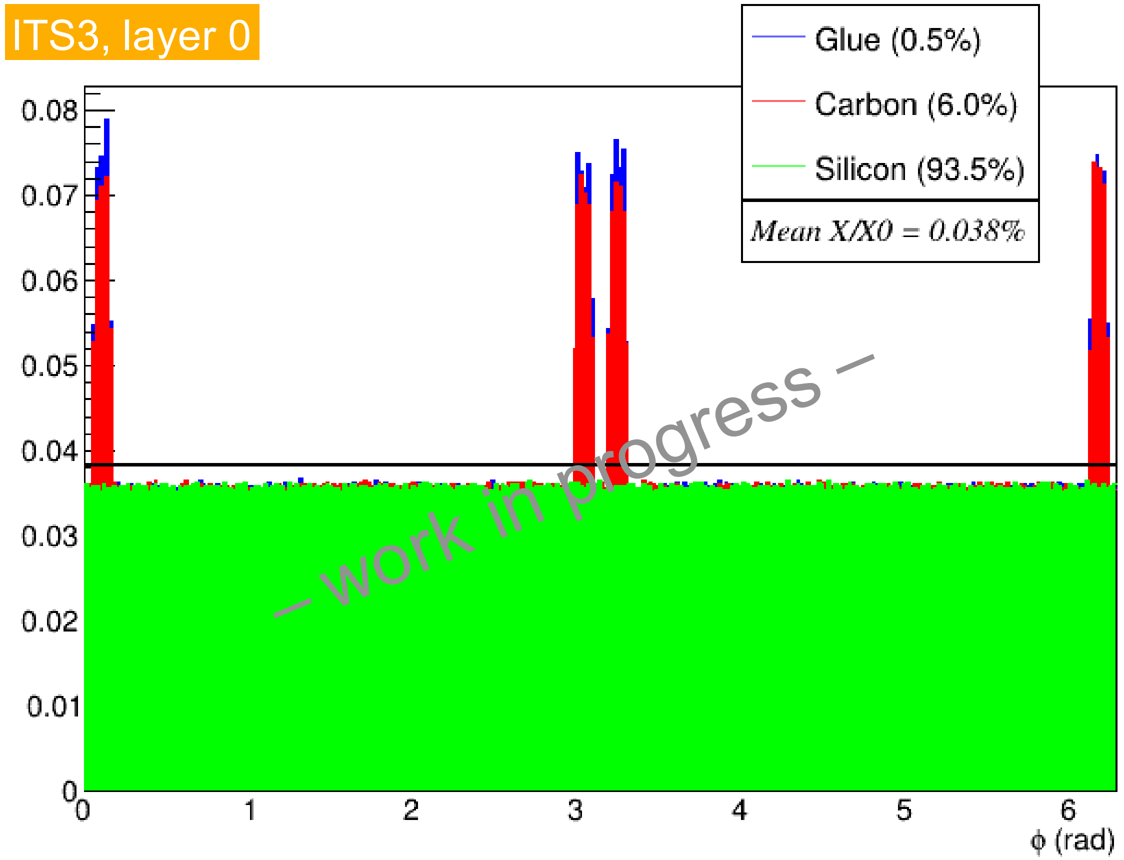
Where do we stand with material budget?

ITS2, layer 0



× 1/10

ITS3, layer 0



This is very reassuring and now also input to our MC!

Outline

- A free-standing detector based on curved silicon
  - The idea behind ALICE ITS3
  - Bent silicon performance
  - R&D highlights

- Timing with silicon
  - LGAD, SPAD/SiPM, FD-MAPS
  - Characterization campaign towards a 20 ps resolution

Includes material and help from: M. Suljic (CERN), M. Mager (CERN), G. Giacomini (BNL), L. Pancheri (UniTN - INFN), F. Carnesecchi (UniBO – INFN), R. Preghenella (UniBO – INFN), C. Gargiulo (CERN), and many others …

Fast timing silicon detectors in Trieste
(and in the ALICE community)

R&D activities in Trieste started from concurring motivations:

- **Scientific interest** within the local group for this new silicon application
- Availability of new **AC-LGAD prototype** samples (from BNL)
- **Experimental push** from the ``ALICE community and beyond``
- **Growing interest** in other fields (medical applications, industry, …)

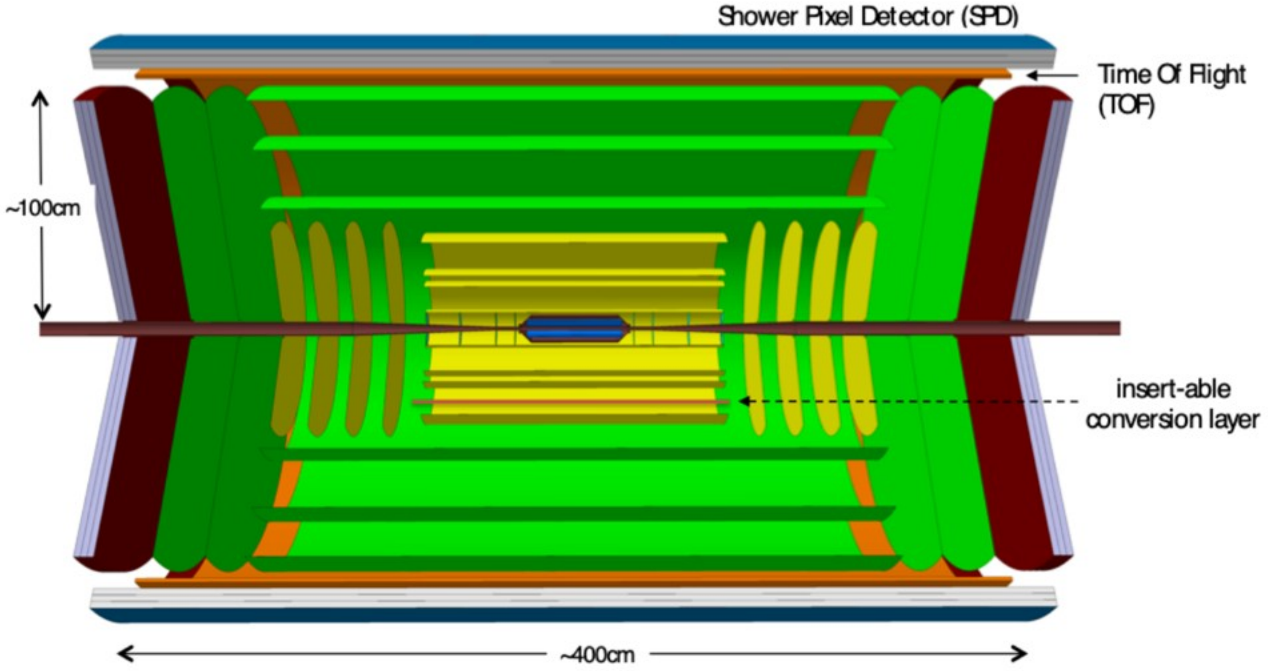
Goal: build up experience on timing sensor characterization

- Early definition of activity plan – open to suggestions for path forward

ALICE3 Experiment for Post-LS4 LHC

"All"-silicon apparatus

- Central/forward tracking
  - ~10 layers based on MAPS
- Particle identification
  - Time-of-flight layers in the central barrel based on **silicon timing sensors**
  - Pre-shower detector based on dense material and MAPS

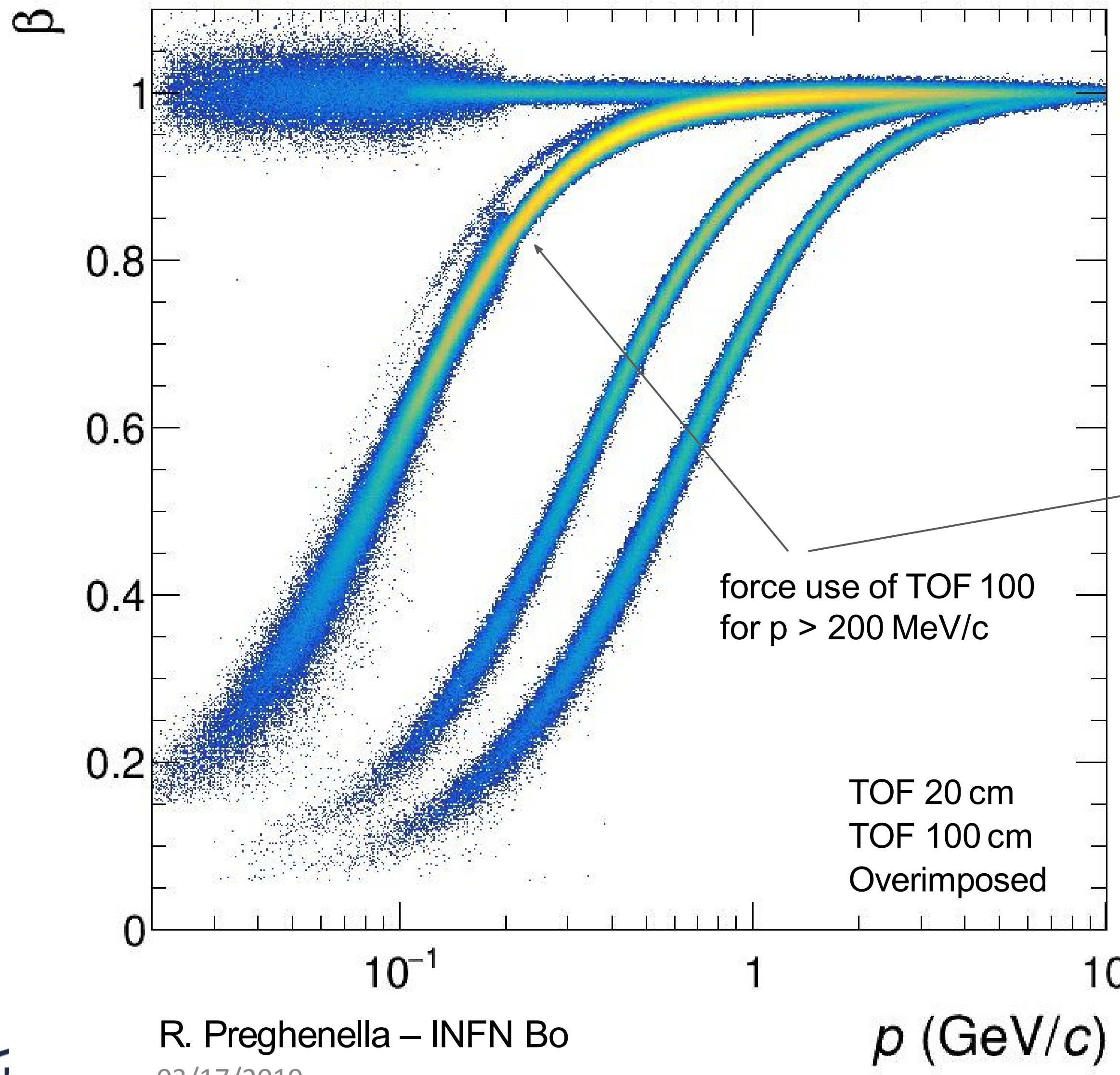


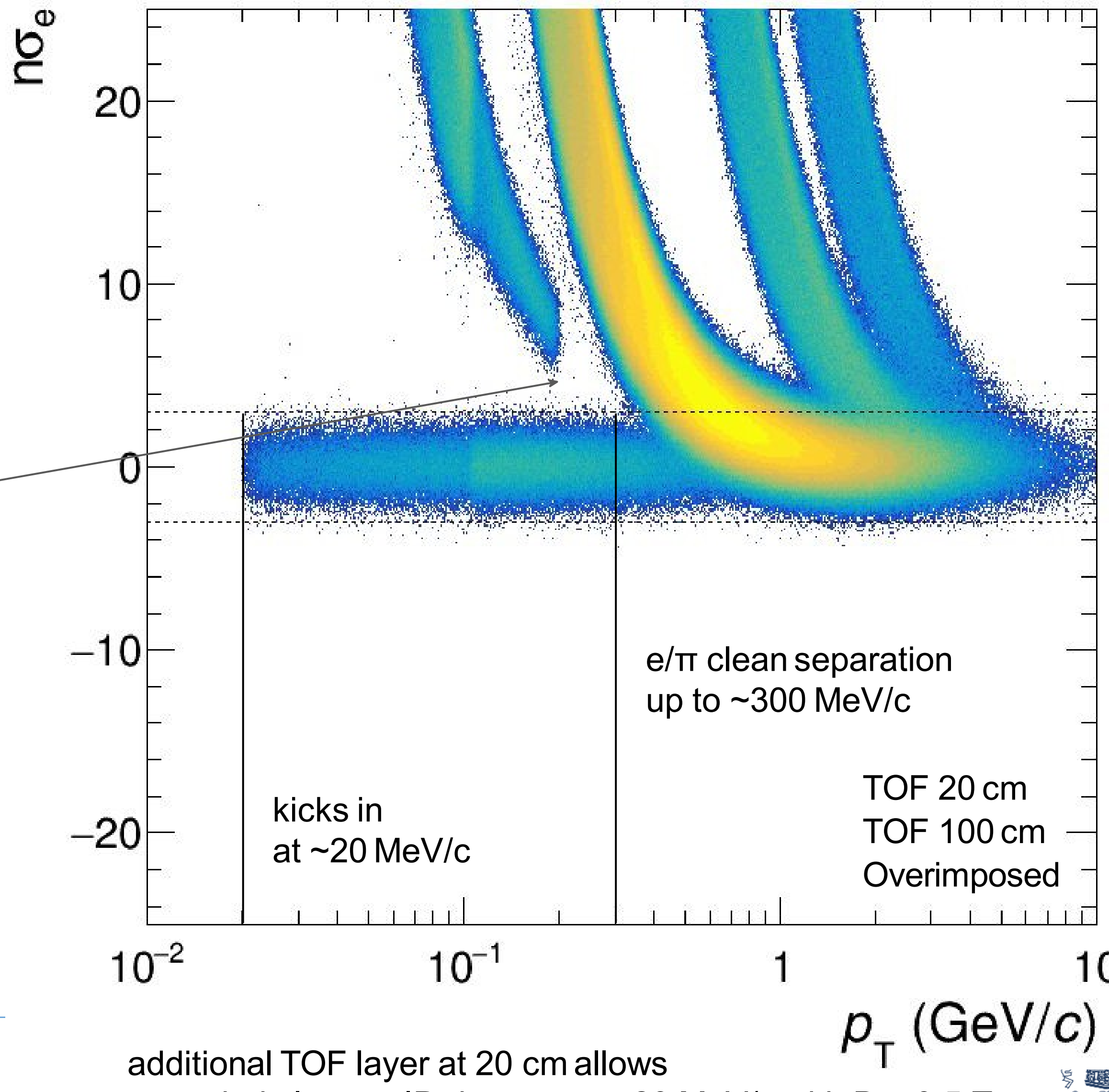
Specifications for TOF layers:

- outer layer, currently at ~1.0 m
- inner layer, currently at ~20 cm
- radii to be tuned for continuous PID performance (e/π)
- **20 ps resolution**

TOF performance simulations

Pythia8, inelastic pp, 14 TeV
primary particles
$|\eta| < 1.44$
B = 0.5 T

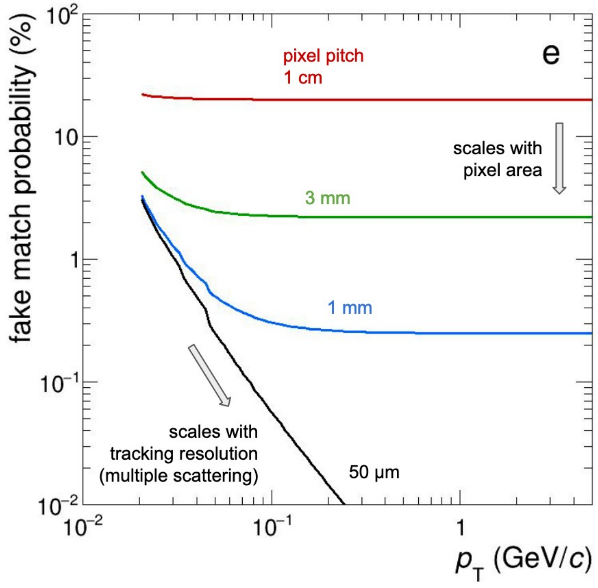


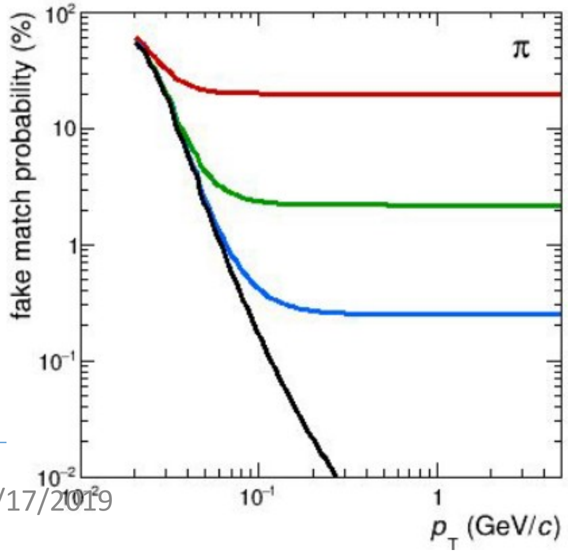


additional TOF layer at 20 cm allows
extended electron ID down to p_T ~ 20 MeV/c with B = 0.5 T

TOF layer cell size Vs fake match probability

TOF layer at R = 22 cm
after tracking layer at R = 20 cm





From simulation studies:

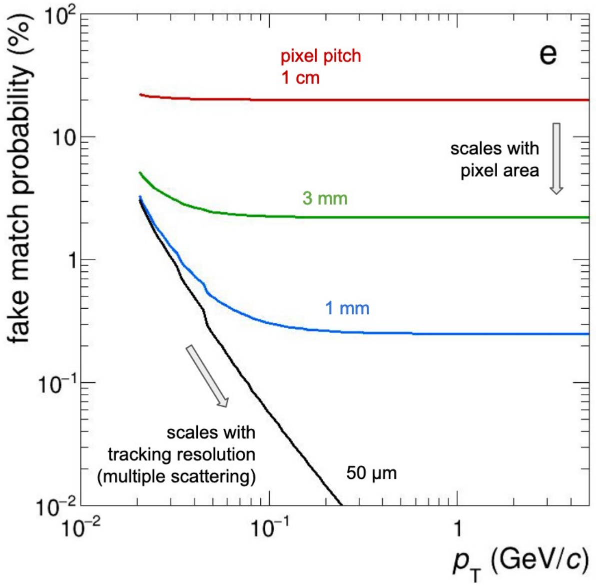
Inner TOF layer (22 cm)

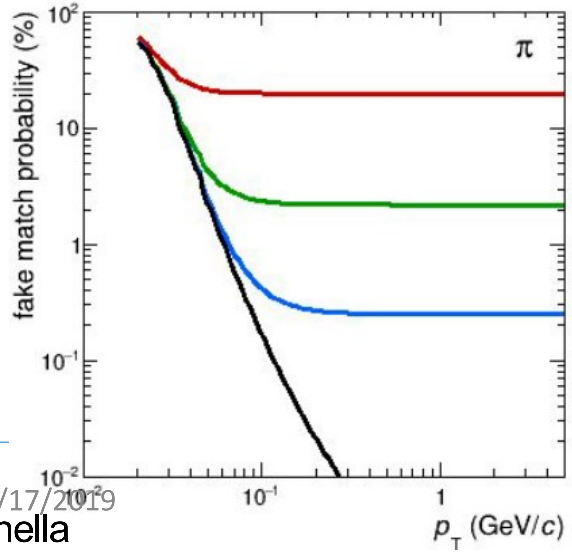
- 1 cm pixel pitch is too big
- 1 mm pixel pitch fake match probability < 1%

R. Preghenella – INFN Bo

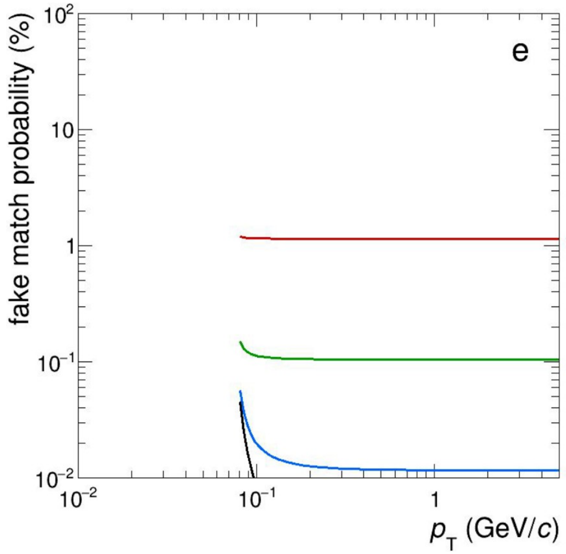
TOF layer cell size Vs fake match probability

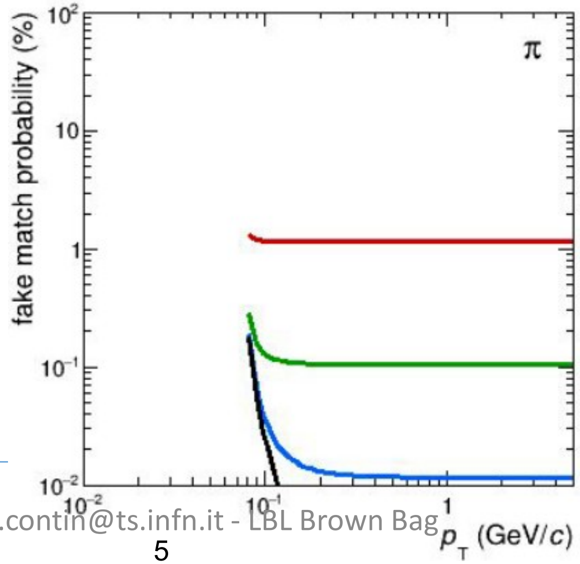
TOF layer at R = 22 cm
after tracking layer at R = 20 cm





TOF layer at R = 102 cm
after tracking layer at R = 100 cm





From simulation studies:

Inner TOF layer (22 cm)

- 1 cm pixel pitch is too big
- 1 mm pixel pitch fake match probability < 1%

Outer TOF layer (102 cm)

- pixel pitches smaller than 1 mm are not needed, negligible contribution from tracking resolution

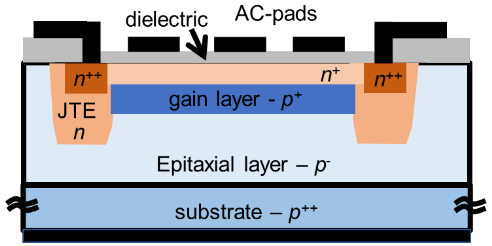
R. Preghenella – INFN Bo

Large menu of silicon timing technologies

Setting up a characterization campaign to answer some questions:

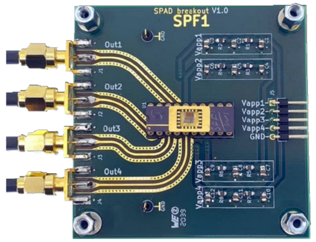
(AC-)LGAD

- Can it provide an acceptable segmentation?



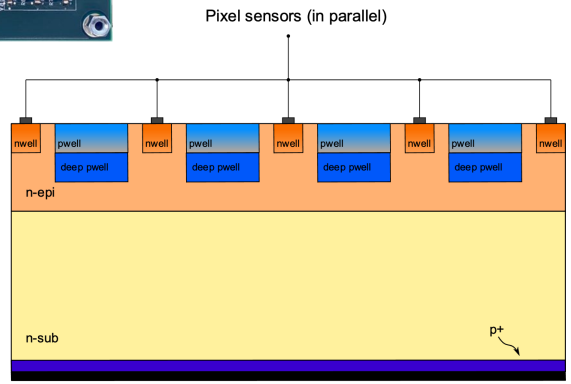
SPAD/SiPM

- How does it perform with particles?

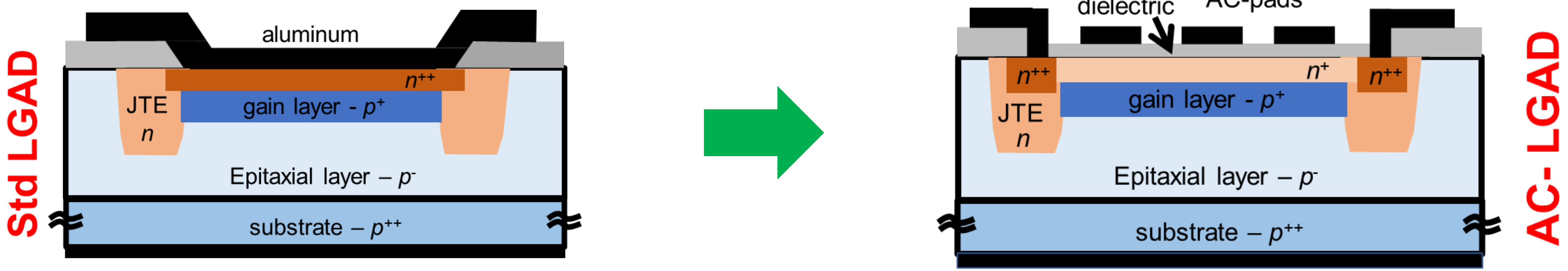


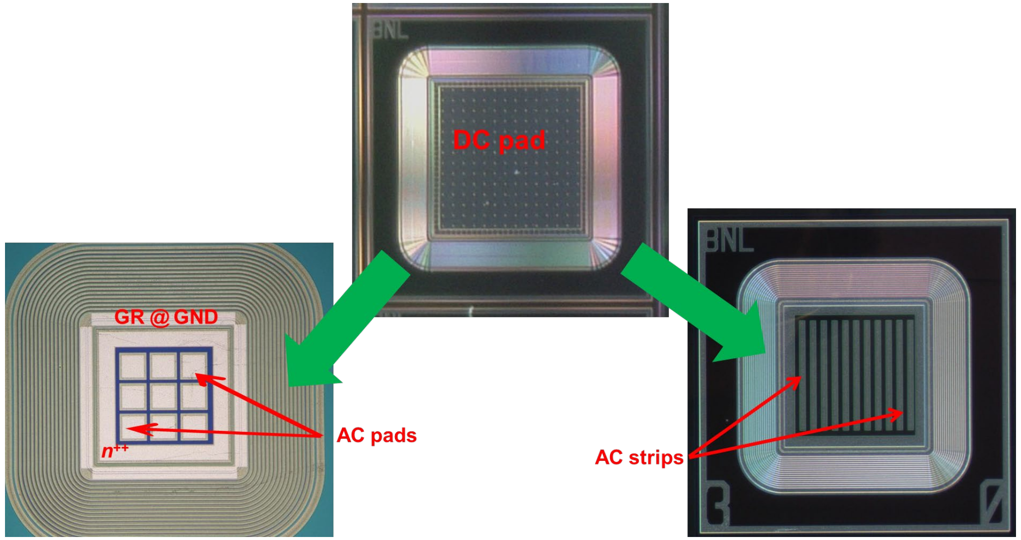
FD-MAPS

- Could we use it for 4D-tracking?



BNL AC-LGAD





Potentially achieve:

- 100% Fill Factor
- High spatial resolution with 200 um pitch
- Fast timing information at a per-pixel level

G. Giacomini @BNL Instrumentation Div.

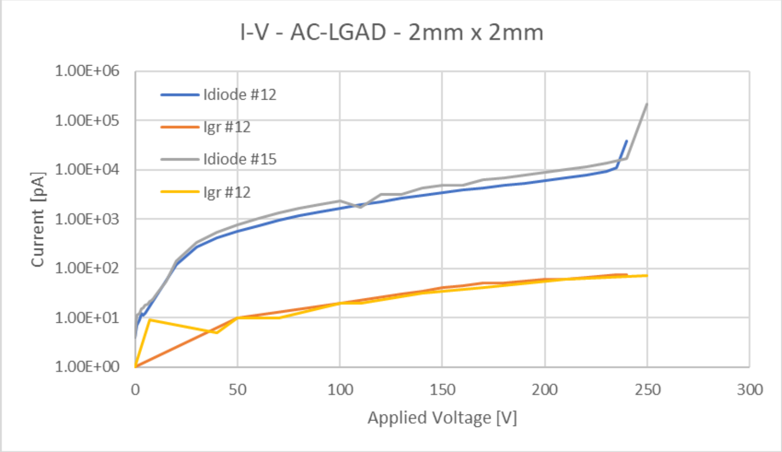
(AC-)LGAD measurements campaign

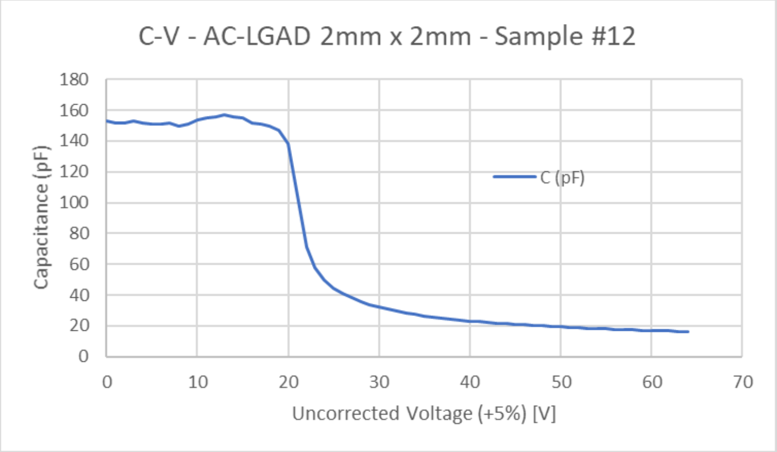
- Static characterization

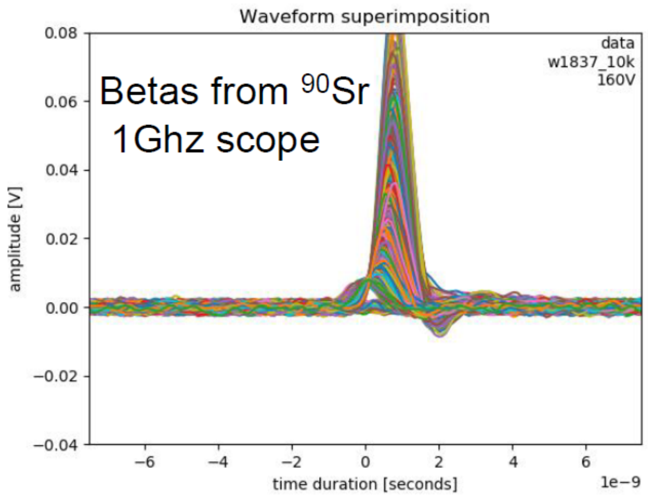
- Fast amplification + waveform an.
  - β irradiation
  - Optical pulsing
  - Laser scan

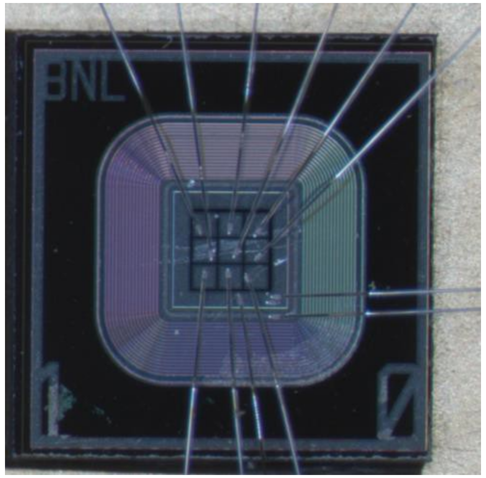
- Compare flavors
  - Diode
  - LGAD
  - AC-LGAD

- Multi-channel board
  - AC-LGAD performance





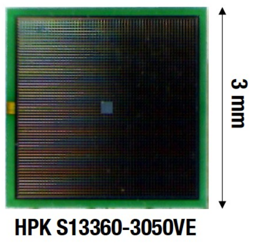




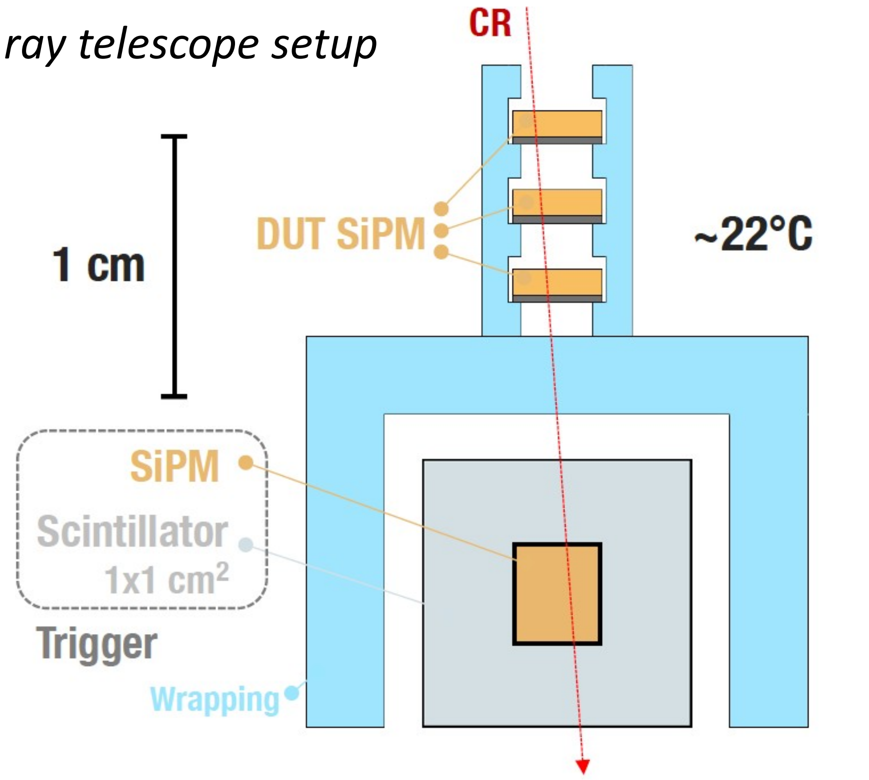
Off-the-shelf SiPM with cosmic rays

- Hamamatsu SiPM @Bologna

HPK S13360-3050VE	
Area	3x3 mm^2
Number of pixels	3584
Gain (at 56 V)	1.7 10^6
Pixel pitch	50x50 μm^2
Fill Factor	74%



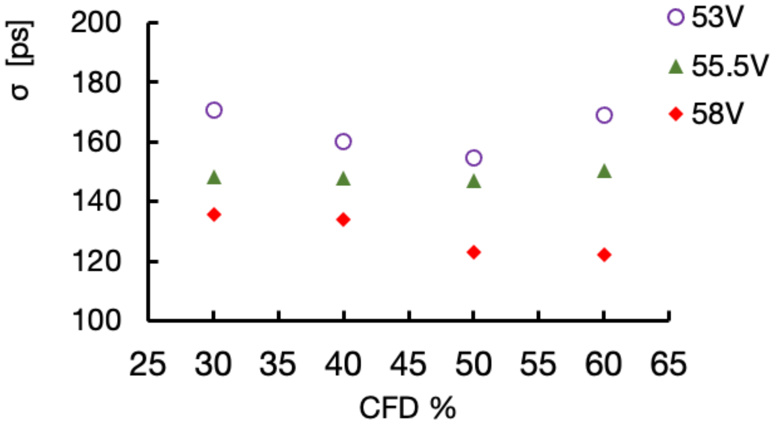
Cosmic ray telescope setup



Preliminary results:

$\sigma_{measured}$ ~ 120 ps @58V

Working on electronics noise evaluation and "cross-talk" effects



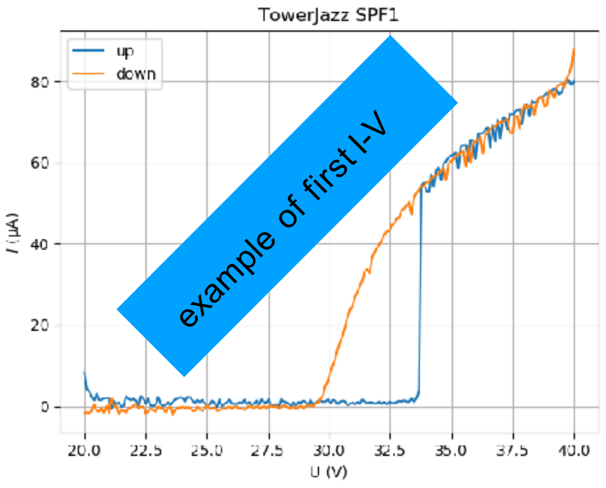
Front-end electronic: cividec (~100 amplification)
Readout: oscilloscope

$$\sigma_{measured} = \sigma_{intrinsic} \otimes \text{electronics noise jitter}\left(\frac{V_{noise}}{dV/dt_{@threshold}}\right) \otimes \text{aquisition jitter}$$

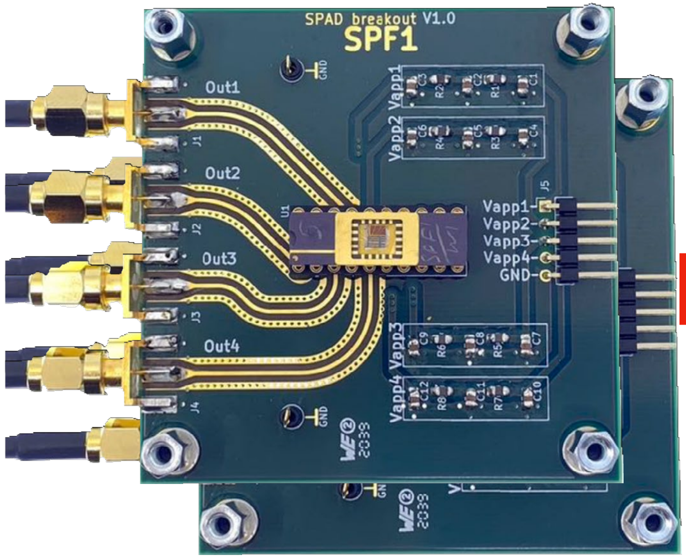
F. Camesecchi – INFN Bo

SPAD prototypes with particle beams

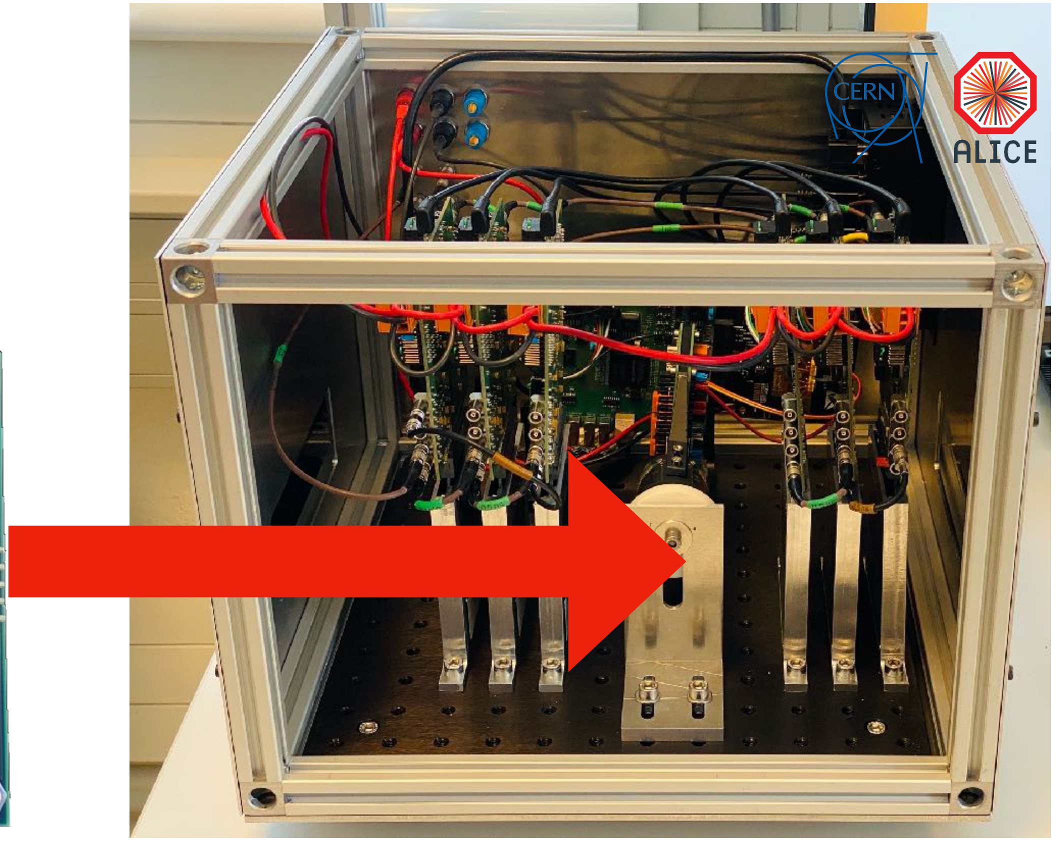
- TowerJazz SPAD prototypes @CERN
- Included in custom made interface boards
- Ready to join the next ITS3 Testbeams
  - Electrons at DESY
  - Pions at CERN PS + SPS



M. Mager – CERN



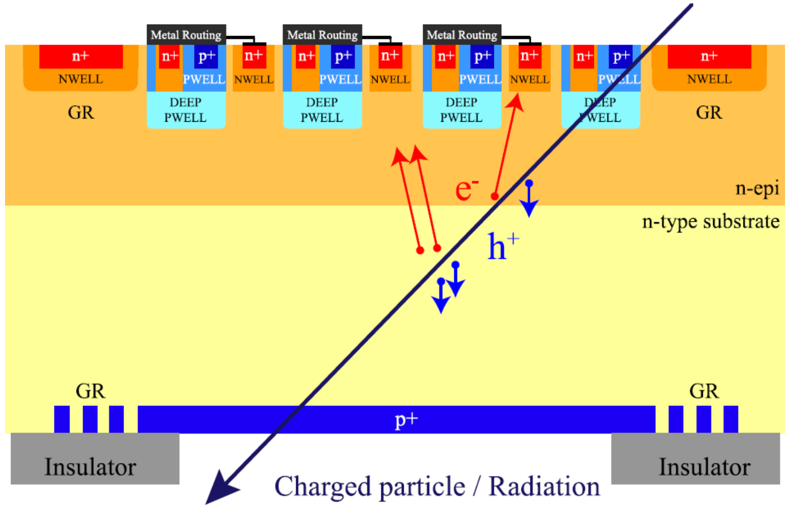
Alpide-based telescope

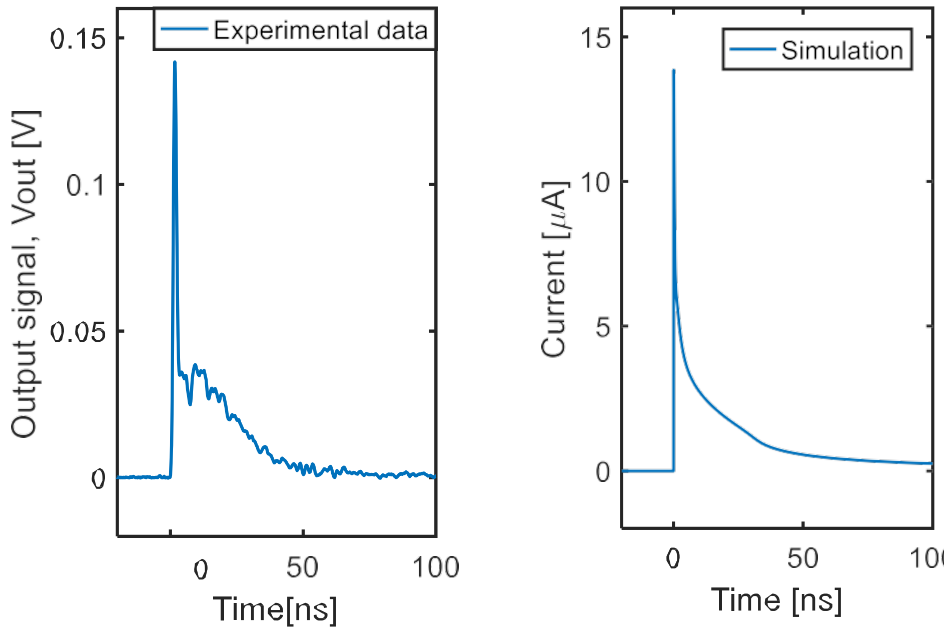


Fully depleted MAPS

ARCADIA monolithic sensors @Trento

- Fully depleted substrate: charge collection by drift
- **Process validated** on 100 – 300μm thick substrates, 25 and 50μm pitch
- **New test structures** with **10μm pitch on 50μm substrate** optimized for timing have been designed. Expected delivery: April/May 2021





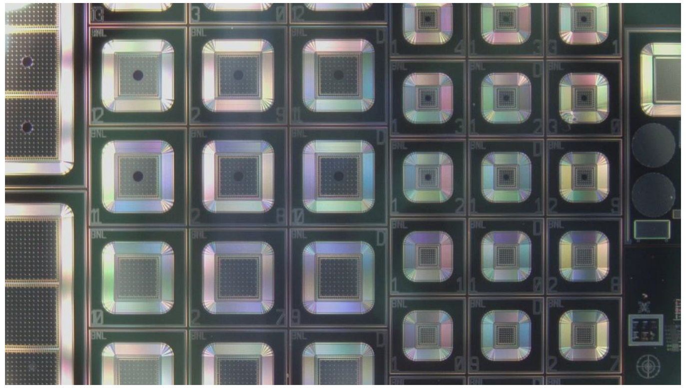
- Signal with IR pulsed laser (1060nm, < 100ps PW) on pixel test structures with 50μm pitch on 300μm substrate
- Measurements with sources and beam to be extended the new test structures

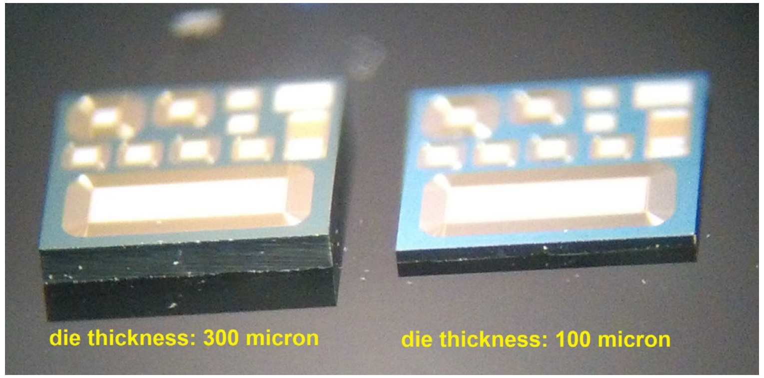
L. Pancheri, INFN Trento & UniTN
(IEEE Tran. Electron Dev., Vol. 67, No. 6, 2020)

Sensor availability for the testing campaign

Sensors currently available:

- **SiPMs** from **HPK**: S12572-050P, S13360-3050VE
- **LGADs** from **HPK**, **FBK** and **BNL** (and reference standard diodes): **50 µm, 1x1 mm^2 , 1x3 mm^2, 2x2 mm^2, 3x3 mm^2**
- **AC-LGADs** from **BNL: 50 µm, 2x2 mm^2**
- **Pixel sensor** test structures (from the SEED project) with **100µm and 300µm thickness, 25µm pitch**





Foreseen for March:

- **SiPM, SPADs** from **FBK: various sizes (15-30 µm)** and shapes

Later (early Summer):

- **Pixel sensor** test structures (from the ARCADIA project) with **50µm thickness, 10µm pitch**

Conclusions

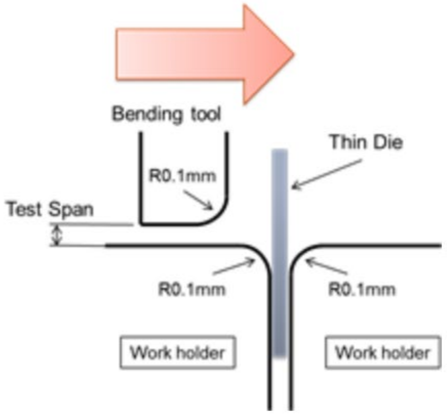
- A year of R&D for the ALICE ITS3 produced exciting results
- A truly-cylindrical detector based of curved silicon seems possible
- The ITS3 is a baseline for future detectors such as the EIC Experiments and ALICE3 @LHC

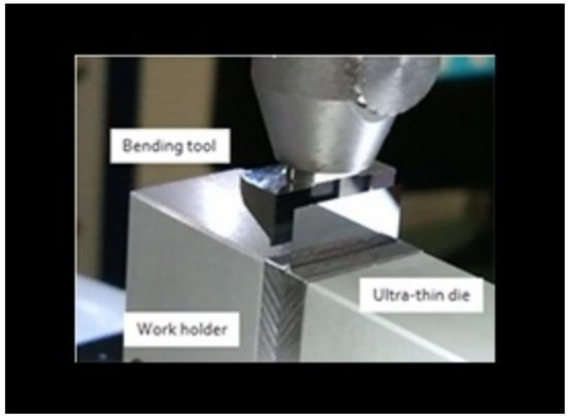
- It is also a good moment to push the R&D on timing silicon sensors and try to include these technologies in such experiments

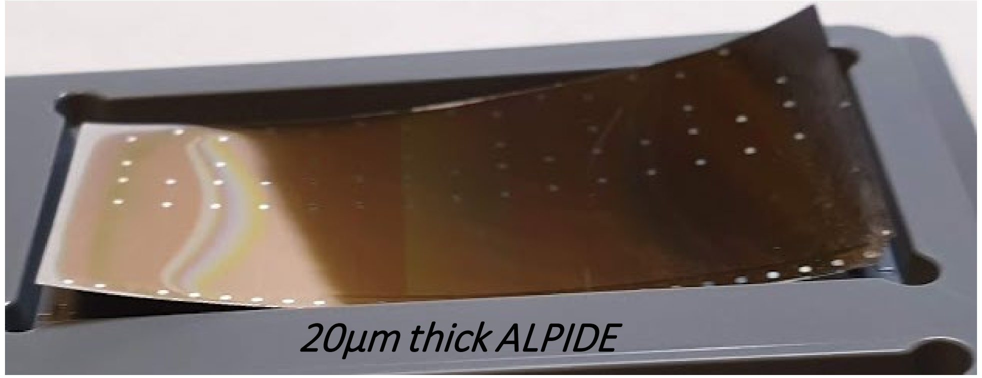
Thank you for your attention…

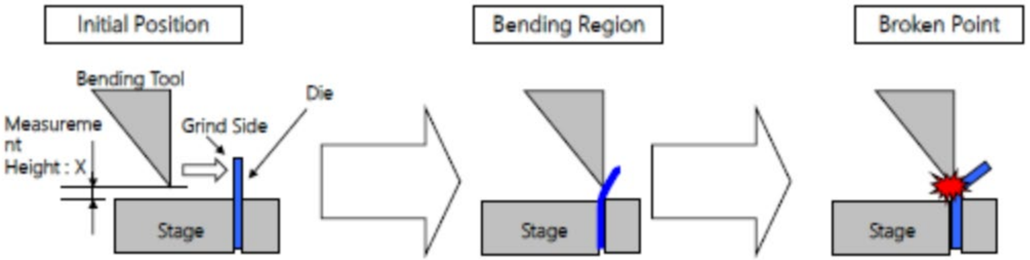
Thinning and bending of single ALPIDEs

- Silicon Deep Reactive Ion Etching (DRIE) of ALPIDE
  - Thinned down to 20-30-50-56 μm
  - Cantilever bending test to breakage
    - 3&4 points test hard to apply on thin small area chips

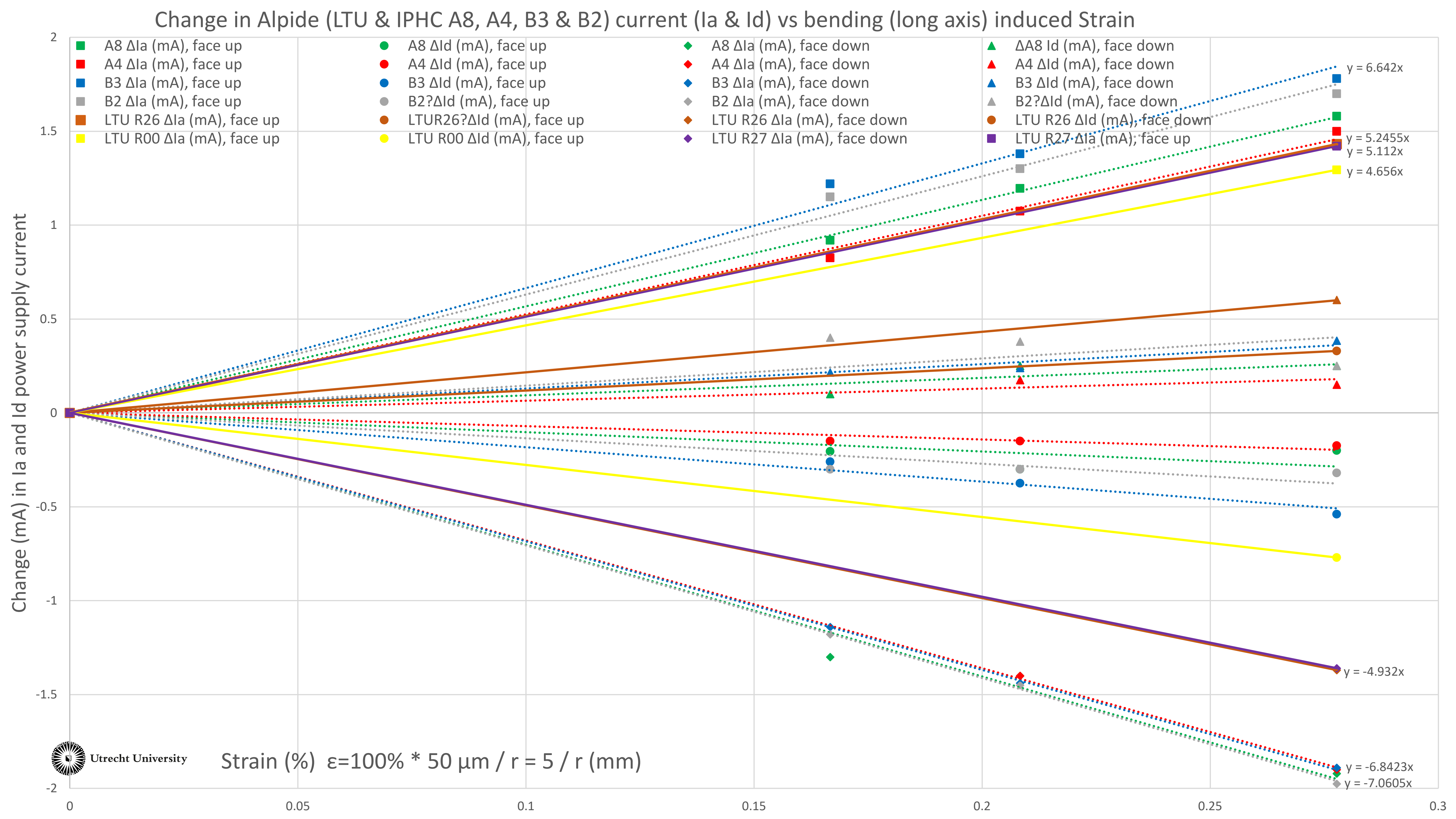








Thickness	Force at break [cN]		
20um	14.8	11.45	16.92
30um	35.95	29.25	35.07
50um	56.04	65.03	124.24
56um	110.5	129.35	


Change in Alpide (LTU & IPHC A8, A4, B3 & B2) current (Ia & Id) vs bending (long axis) induced Strain
A8 ΔIa (mA), face up
A4 ΔIa (mA), face up
B3 ΔIa (mA), face up
B2 ΔIa (mA), face up
LTU R26 ΔIa (mA), face up
LTU R00 ΔIa (mA), face up
A8 ΔId (mA), face up
A4 ΔId (mA), face up
B3 ΔId (mA), face up
B2?ΔId (mA), face up
LTUR26?ΔId (mA), face up
LTU R00 ΔId (mA), face up
A8 ΔIa (mA), face down
A4 ΔIa (mA), face down
B3 ΔIa (mA), face down
B2 ΔIa (mA), face down
LTU R26 ΔIa (mA), face down
LTU R27 ΔIa (mA), face down
ΔA8 Id (mA), face down
A4 ΔId (mA), face down
B3 ΔId (mA), face down
B2?ΔId (mA), face down
LTU R26 ΔId (mA), face down
LTU R27 ΔIa (mA), face up
y = 6.642x
y = 5.2455x
y = 5.112x
y = 4.656x
y = -4.932x
y = -6.8423x
y = -7.0605x
Change (mA) in Ia and Id power supply current
Strain (%) ε=100% * 50 µm / r = 5 / r (mm)
Utrecht University
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
0
0.05
0.1
0.15
0.2
0.25
0.3