Bergen module production site qualification stage #1

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Special thanks to Alessandro Lapertosa

Presented by Simon Huiberts

ATLAS EXPERIMENT

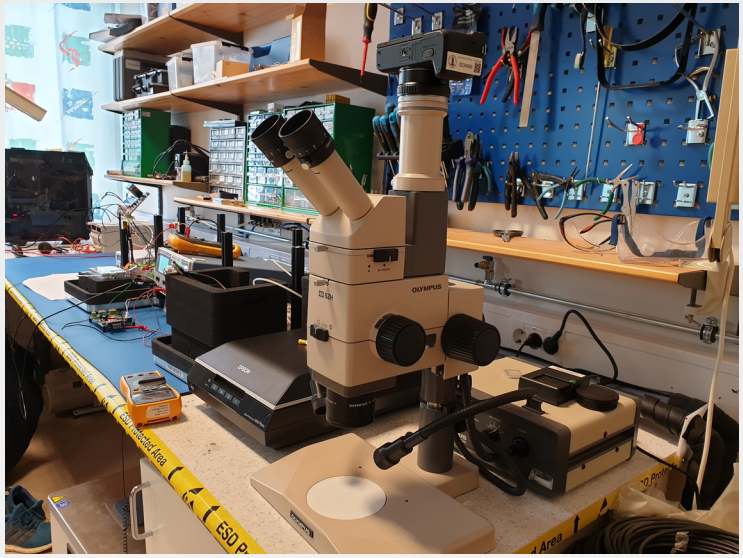
UNIVERSITY OF BERGEN

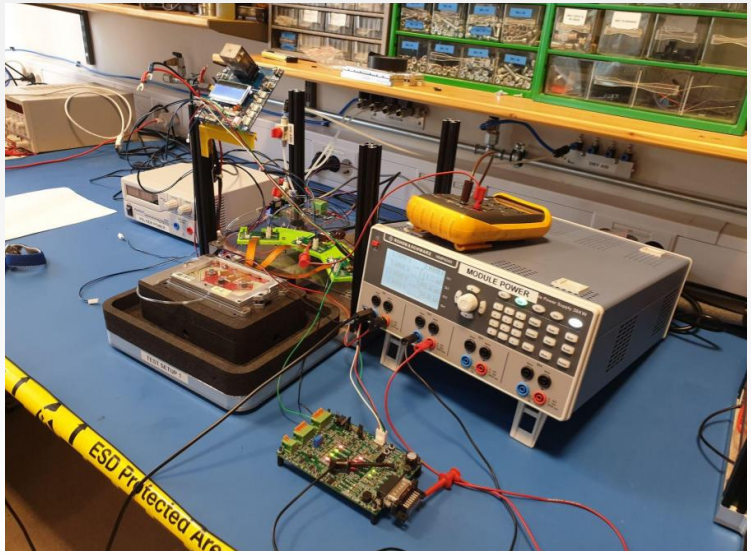
Requirements

- **Stage 1 focuses on setup and electrical testing**
- **Check and document any damages on the module**
- On a triplet module receival preform the following tasks:
  - Check the packaging for damage
  - Register shipment in PDB
  - Visual inspection (module carrier, triplet: flex and wirebonds)
  - VI-curve to find the operational power
  - Check the VIN and trim VDDD/VDDA
  - Preform the tuning procedure on triplet
  - Upload data to local DB
- Also monitor the temperature when operating the triplet
  - Active or passive cooling to keep the module below 55 ℃

Setup overview

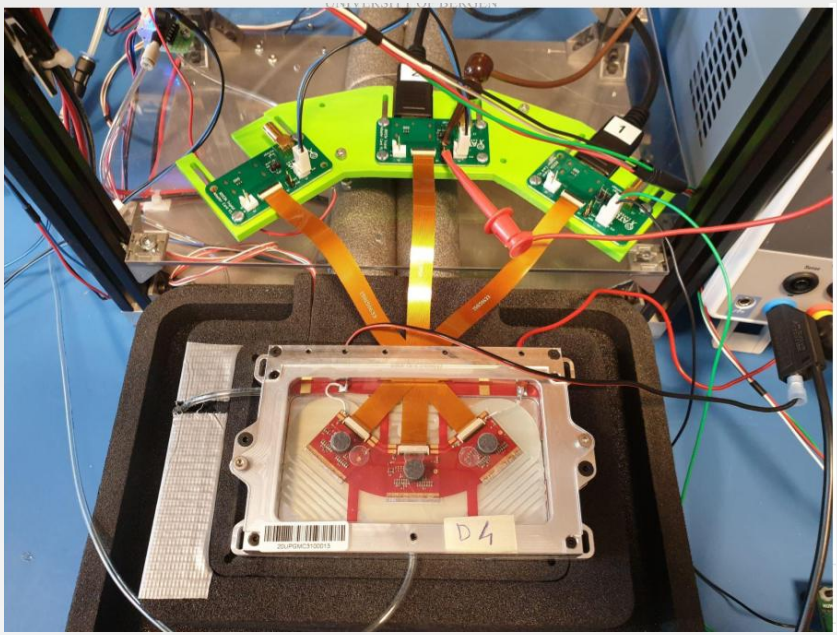
- Triplet cooling unit (Link to documentation)
- Julabo DD1000F refrigerated circulator (cooler/chiller)
- PG28L Purge Gas Generator for supply of dry air 28 L/min
- Visual inception with EPSON Perfection 0600 photo scanner and Olympus microscope with Canon EOS MK II camera
  - Detailed images taken manually with software for stitching
- HMP4040 LW power supply
- Vacuum generator
- Peltier Controller and Test Monitor (PCTM)
  - HW interlock
  - Transmits the temperature measurements from the NTC accessible trough the data cables
- DAQ PC: Intel computer with latest version of YARR

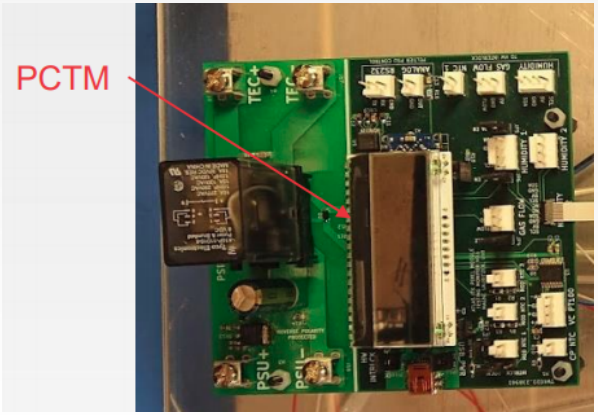


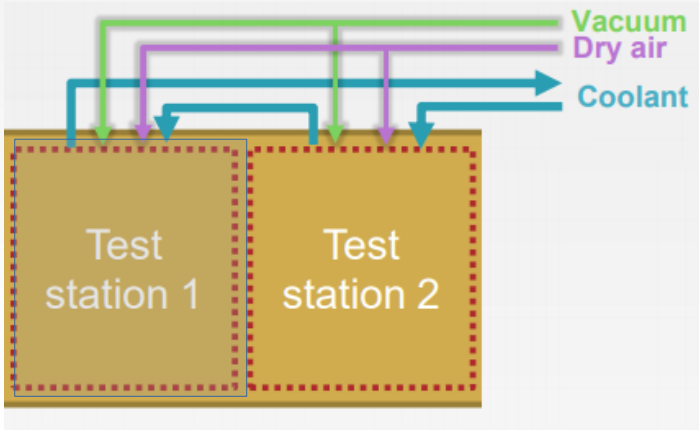


Setup during testing

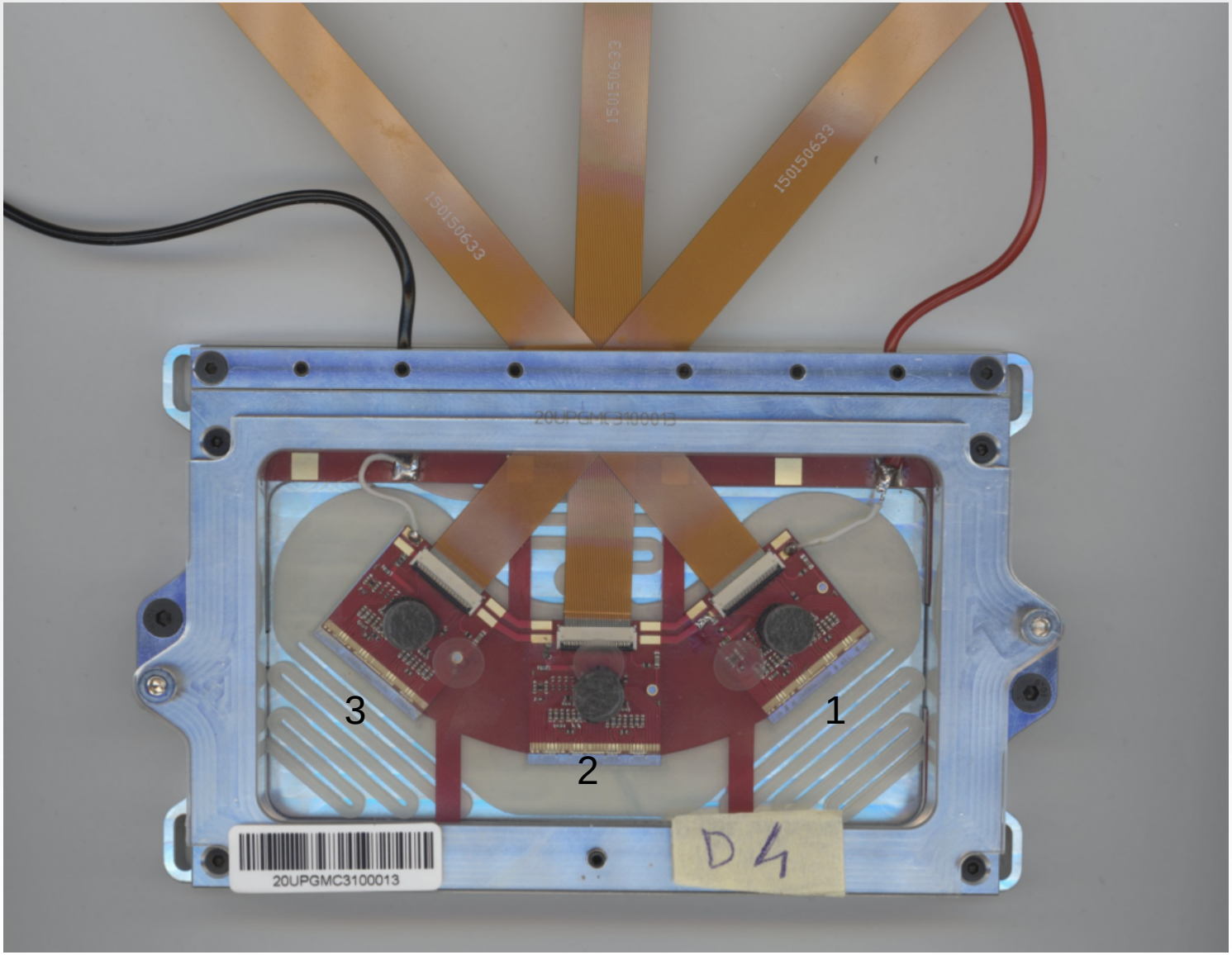
- D4 triplet module placed on top of the cooling unit and kept in place via vacuum
  - Chiller set to at 0°C and dry air was applied
- Data lanes connected to the adapter cards
- During trimming a digital multimeter was connected to the VIN and MUX pins
- Display port cables into the lab PC
- Monitoring the NTC temperature and humidity with the PCTM
- Hardware interlock on chip A





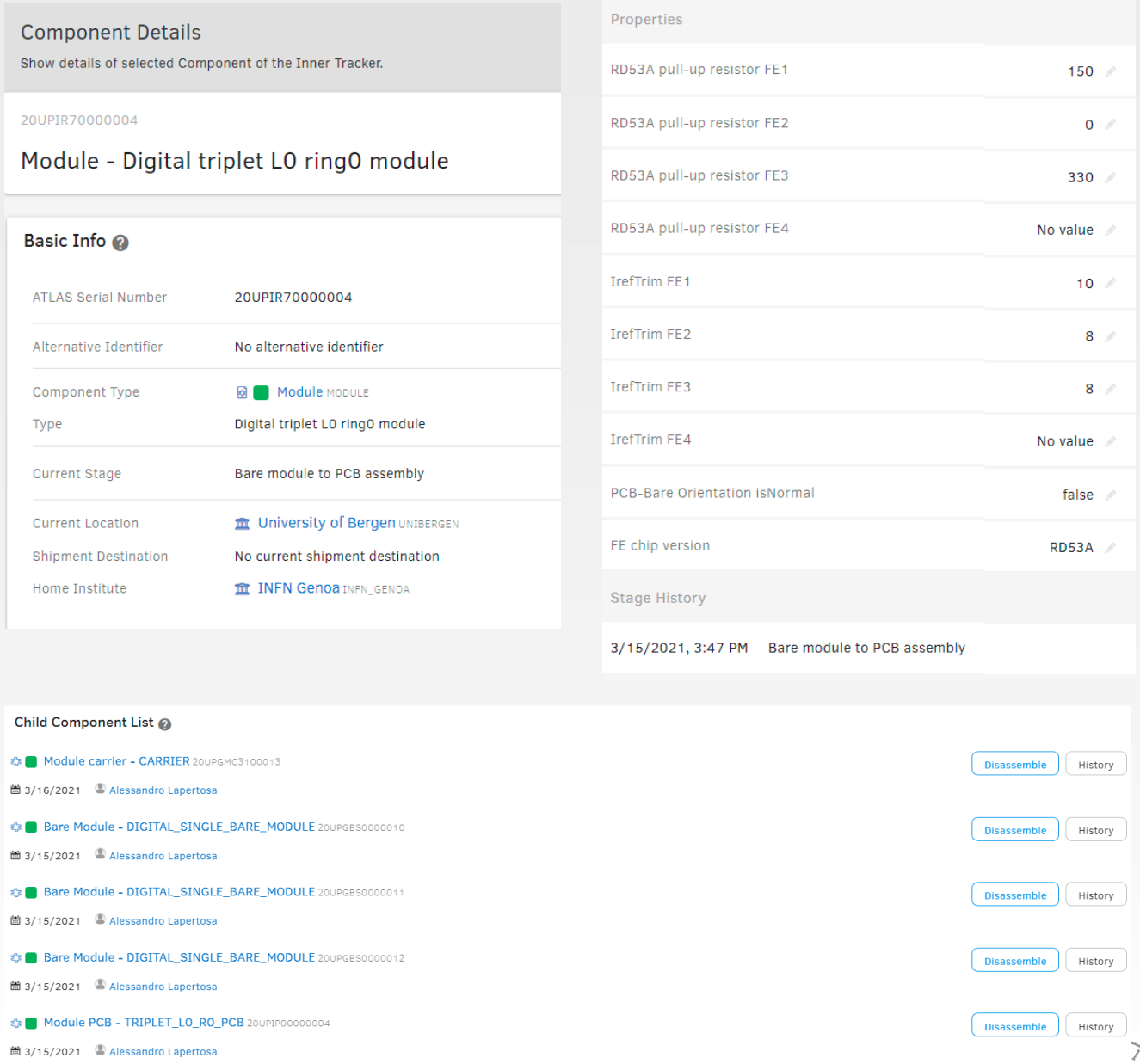


Module inside carrier (Scanner photo)

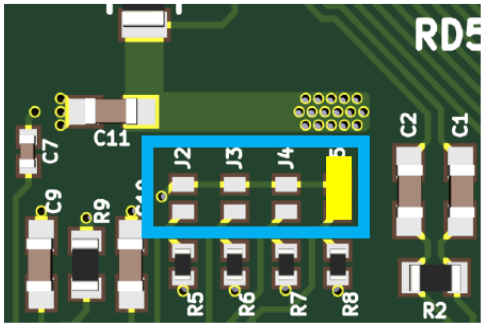
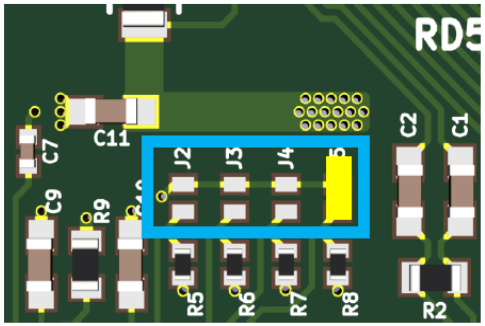
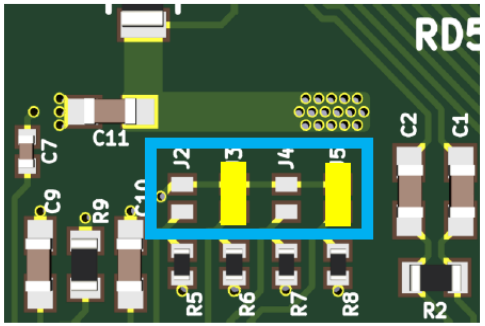
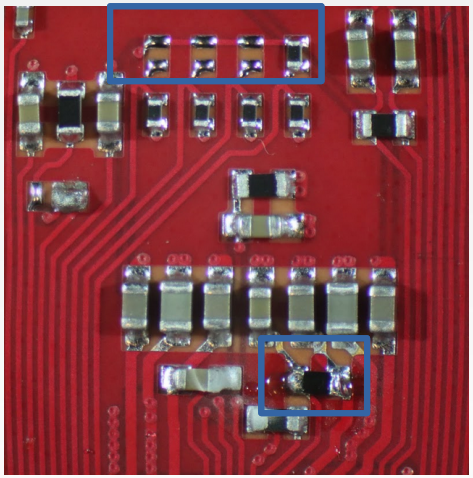
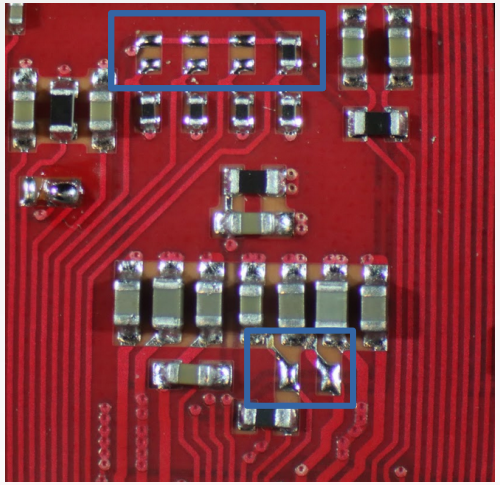
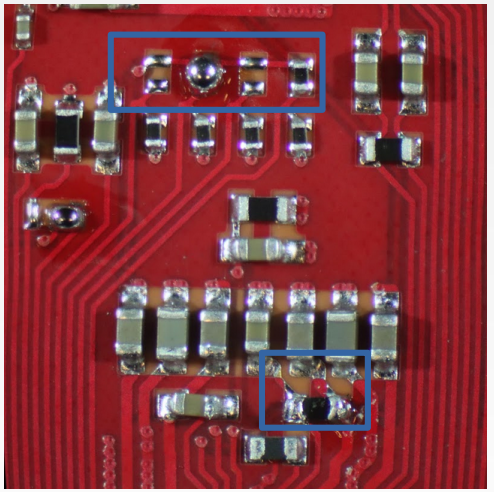


Recival in PDB

- Packaging looked fine
- Added shipment in PDB
- Looked up all information in the PDB
- Everything was in order
- Chip 3: SN: "20UPGFC0029011
- Chip 2: SN: "20UPGFC0029014"
- Chip 1: SN: "20UPGFC0029015

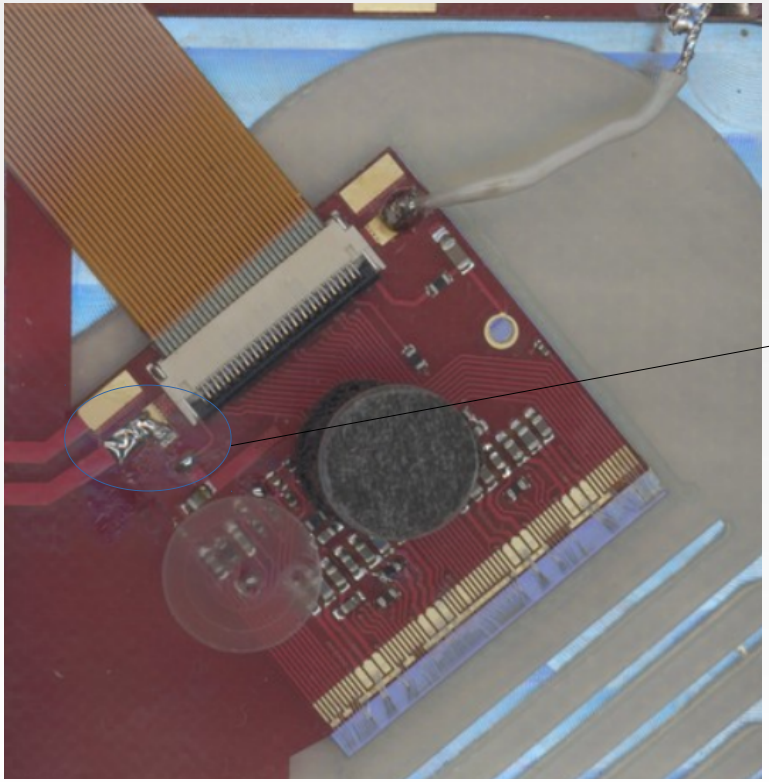


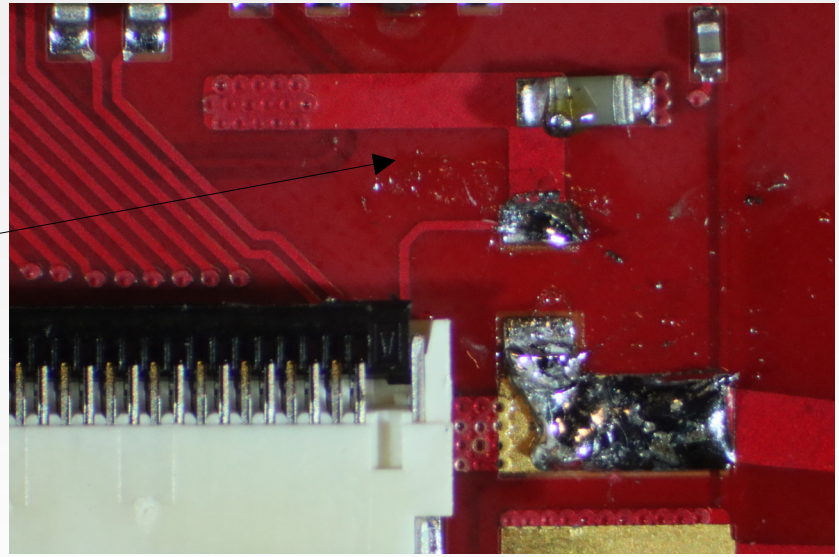
Iref Trims and pull-up resistors

Chip Nr: 3	Chip Nr: 2	Chip Nr: 1
Trim = 8	Trim = 8	Trim = 10
		
		
300 kΩ	No resistor	150 kΩ

Visual inspection on module

- Showed removed resistor on Chip Nr. 3 from the VIN (chip 3 disconnected)
- Matched the module report from Genova
- Left figure taken with scanner when triplet inside the carrier and right figure taken with the digital camera and microscope figure

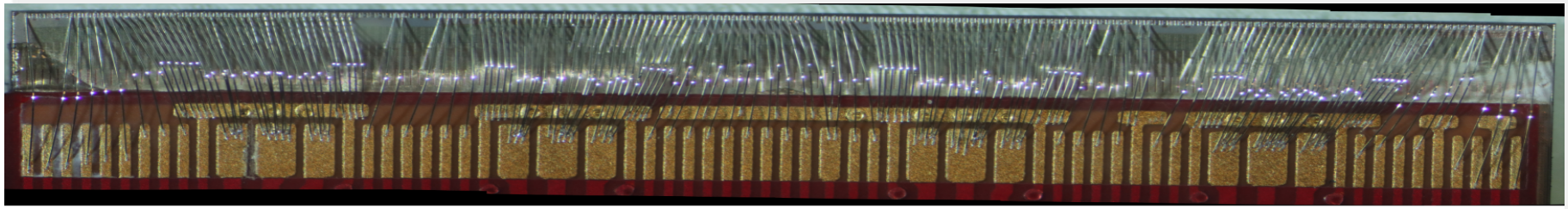




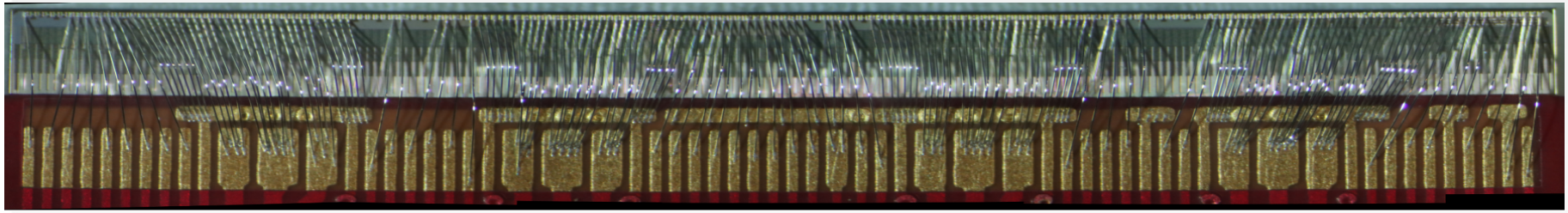
Visual inspection on wirebonds

- Olympus microscope with Canon EOS MK II camera
- Visual inspection showed that the wirebonds was god on chip 3 and chip 2
- Chip 3 had missing GND-pad wirebonds
- As expected as Genova reported a short circuiting on chip 1 and disconnected this chip

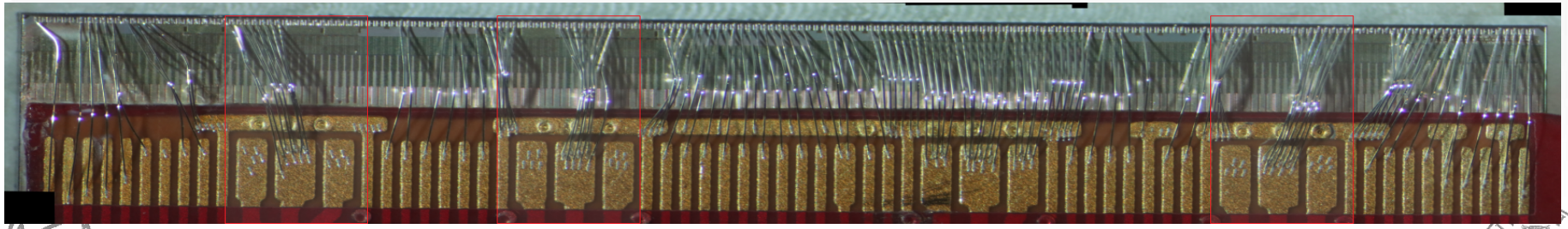
3



2

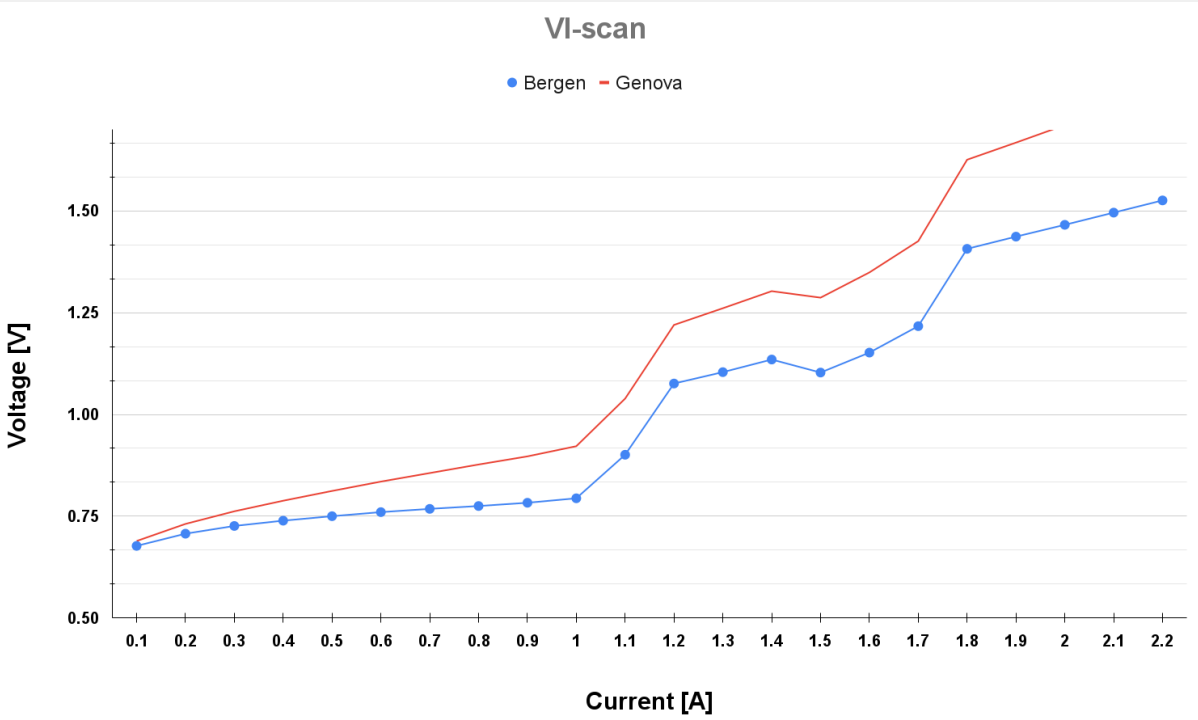


1



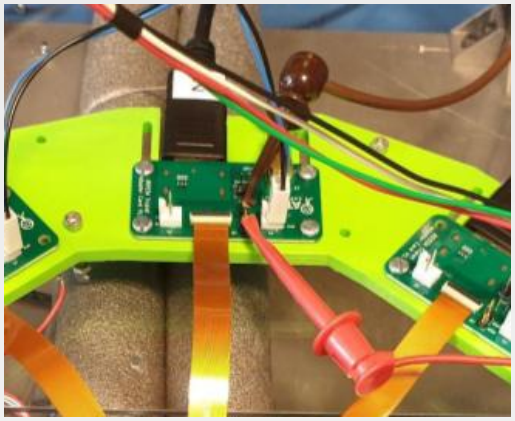
VI-scan

- Set the voltage limit on 1.9 V on the power supply and went in 0.1 A steps down starting at 2.2 A (since only two working chips)
- Turned on/off current from PSU on each step
- Measured voltage over VIN pin on adapter card on chip 3 and GND pin on chip 2.
- VI-scan showed linear dependency above 1.8 A (blue points)
- Matched well with VI-scan results from Genova (red line)



Trimming

- VIN [V] read directly from the pins on the adapter card (4-wire measurement) with a multimeter
- The VDDD/VDDA read from the MUX pins on adapter card by setting the correct output from the JSON file
- E.g. VDDD = 2 x (VMUX(reg 30) - VMUX(reg 27))
- All values already close to target 1.2 V, except for VDDD on Chip 2
  - Setting the SldoDigitalTrim from 22 to 25 gave a new value on VDDD [V] = 1.198 [V] for this chip.



MUX pins on adapter card

Operation voltage = **1.697V and 2A**

D4	VIN [V]	VDDD [V]	VDDA [V]
3	**1.474**	**1.214**	**1.2**
2	**1.483**	**1.16 - > 1.198**	**1.21**

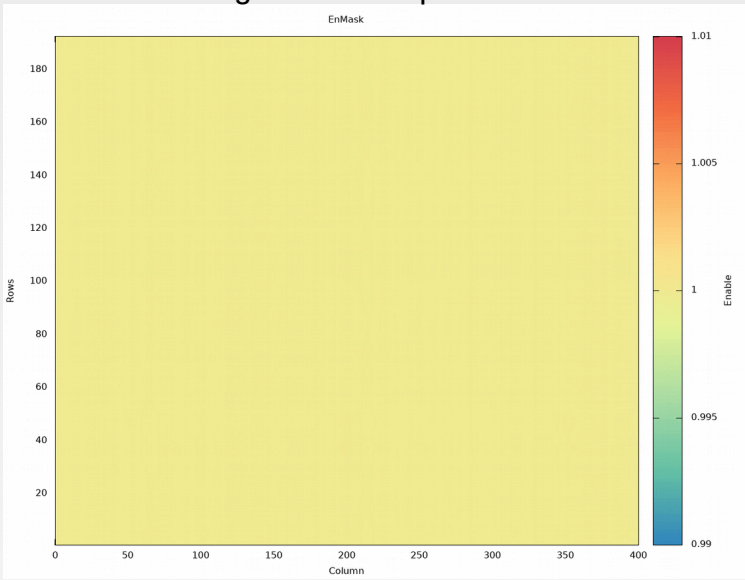
D4	GND [V]	VOUT Dig. ShuLDO [V]	VOUT Ana. ShuLDO [V]
3	0.004	0.611	0.604
2	0.004	0.584 - > 0.603	0.609

Value	Selection
24	VOUT Ana. ShuLDO
25	VREF Ana. ShuLDO
26	VOFF Ana. ShuLDO
27	grounded
28	grounded
29	VIN Dig. ShuLDO
30	VOUT Dig. ShuLDO

Tuning procedure

- First digital and analoge scan looked good for the two working chips and able to tune the two working chips successfully:
  - Target threshold -> 2000e for syn FE and 1000e (diff and linear)
  - Higher threshold target chosen for Syn FE as this FE has earlier reported issues with 1000e tuning and chip Nr 2 didn't even reach the 2000e target
  - Target ToT -> 10ke 7 ToT for all

Digital scan chip Nr 3/2



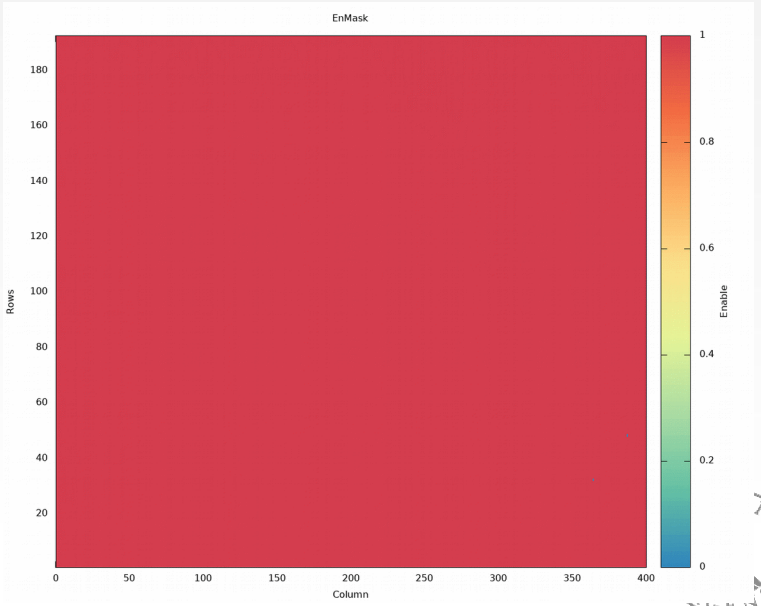
Module json file


```
{
  "module": {
    "serialNumber": "D3",
    "componentType": "Module"
  },
  "stage": "Testing",
  "chipType" : "RD53A",
  "chips" : [
    {
      "config" : "configs/D3/configs/20UPGFC0028997.json",
      "tx" : 0,
      "rx" : 0,
      "enable" : 1,
      "locked" : 0
    },
                {
      "config" : "configs/D3/configs/20UPGFC0028998.json",
      "tx" : 1,
      "rx" : 1,
      "enable" : 1,
      "locked" : 0
    },
```


Spec Config file

- "rxPolarity" : 65535,
- "txPolarity" : 15,

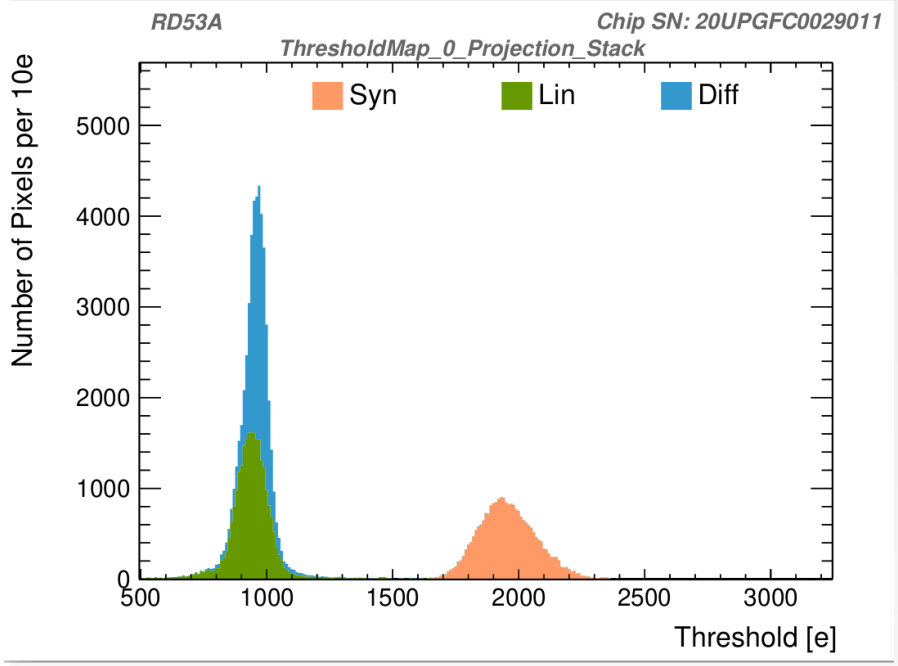
Analogscan chip Nr 3/2

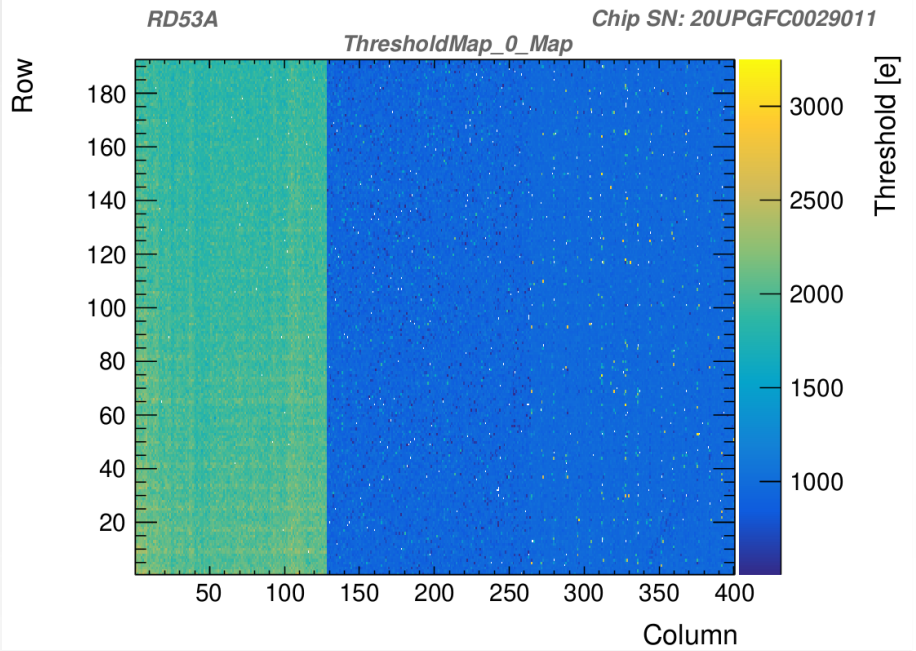


Chip json file

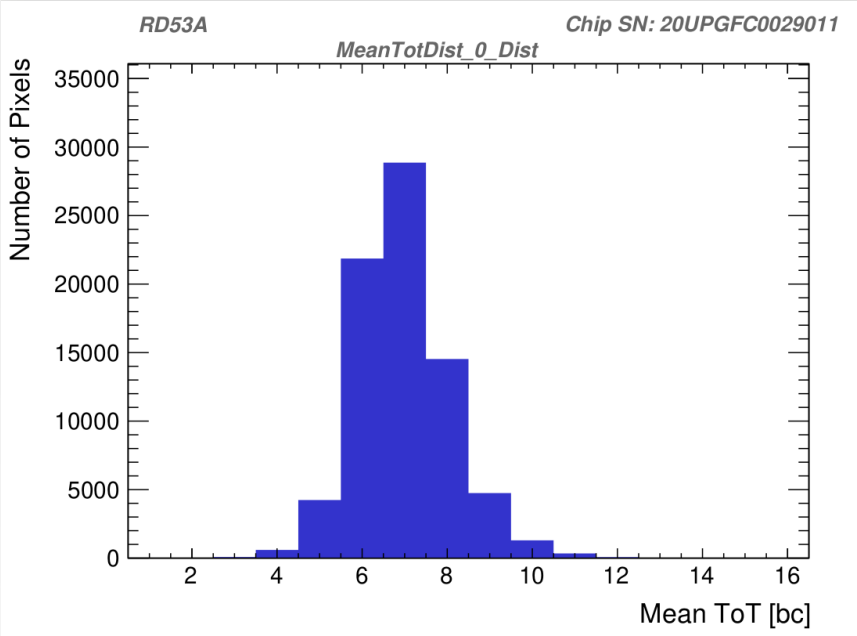
- YARR FW 640 MHz clock → "CdrSelSerClk": 1,
- Chip ID (1, 2 and 3) of each chip → "ChipId": 1,
- Name as the chip Serial Number → "Name": "20UPGFC0028999",

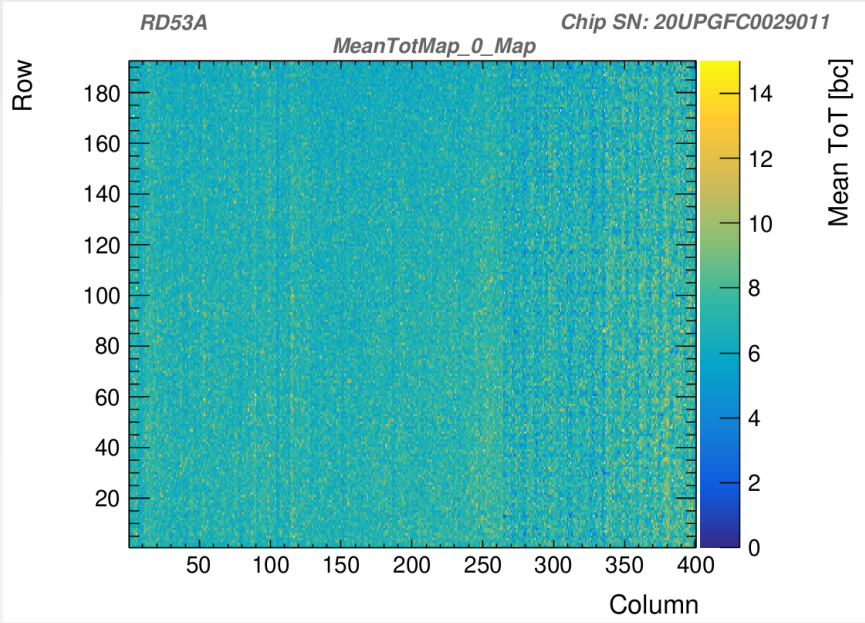
Tuning Results Chip A: Threshold



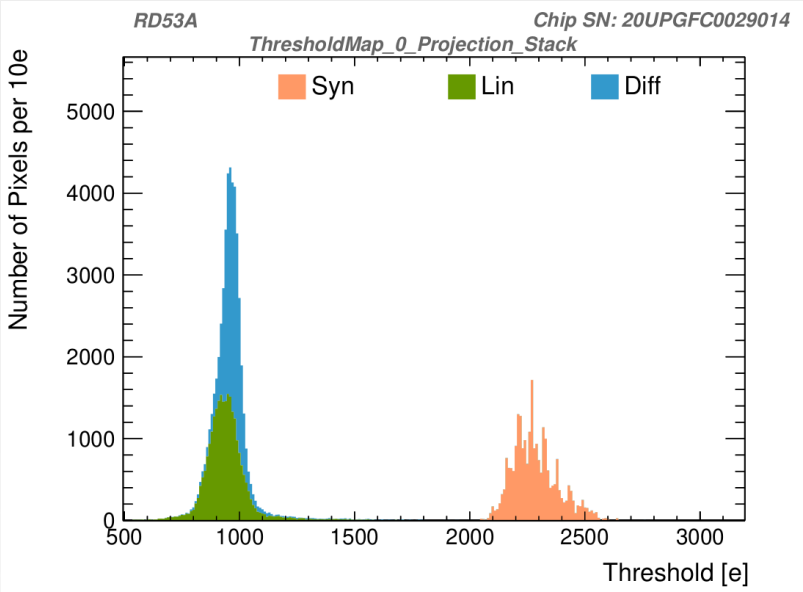


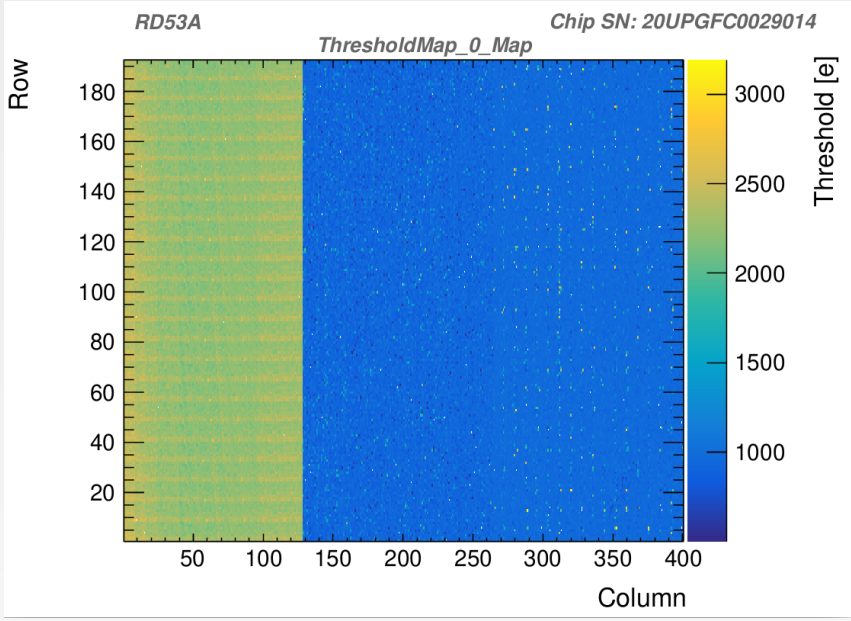
Tuning Results Chip A: ToT



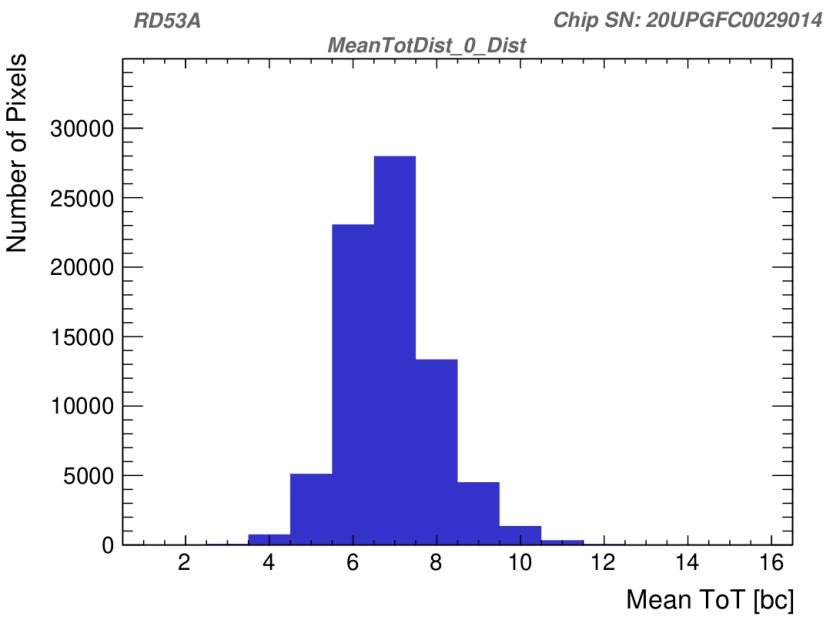


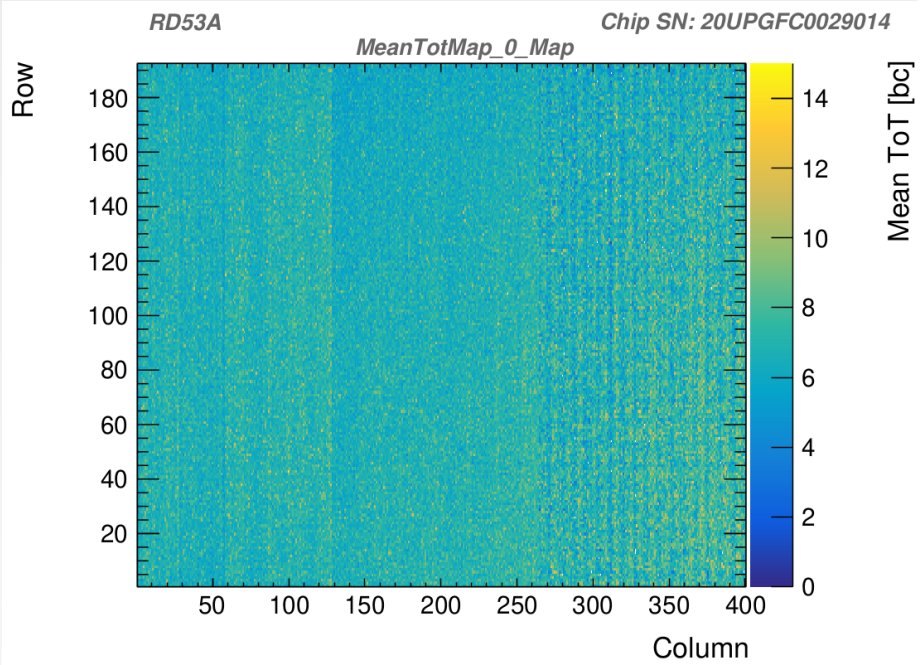
Tuning Results Chip B: Threshold





Tuning Results Chip B: ToT

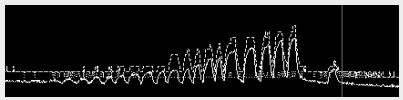


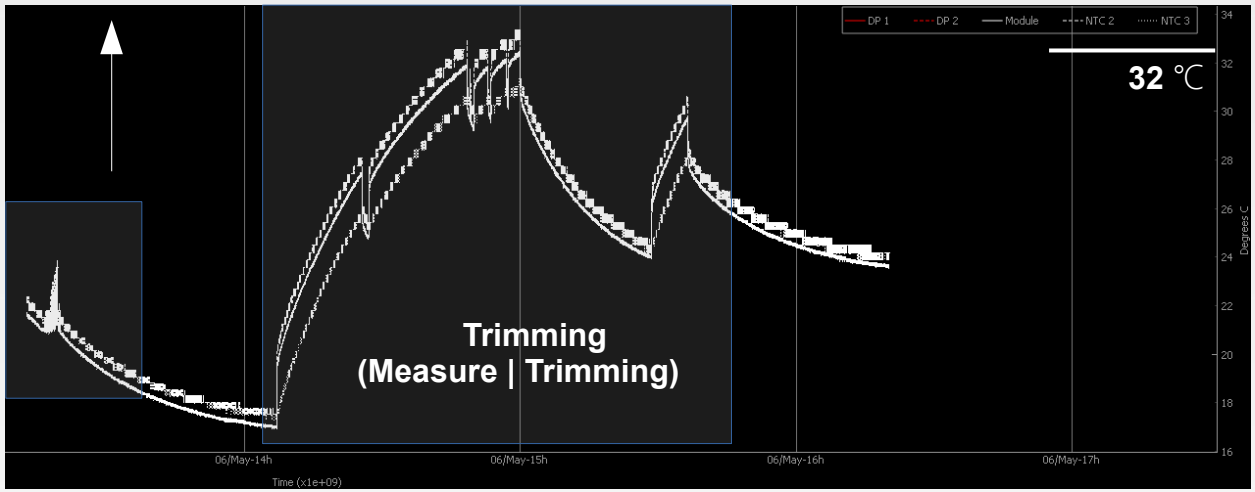


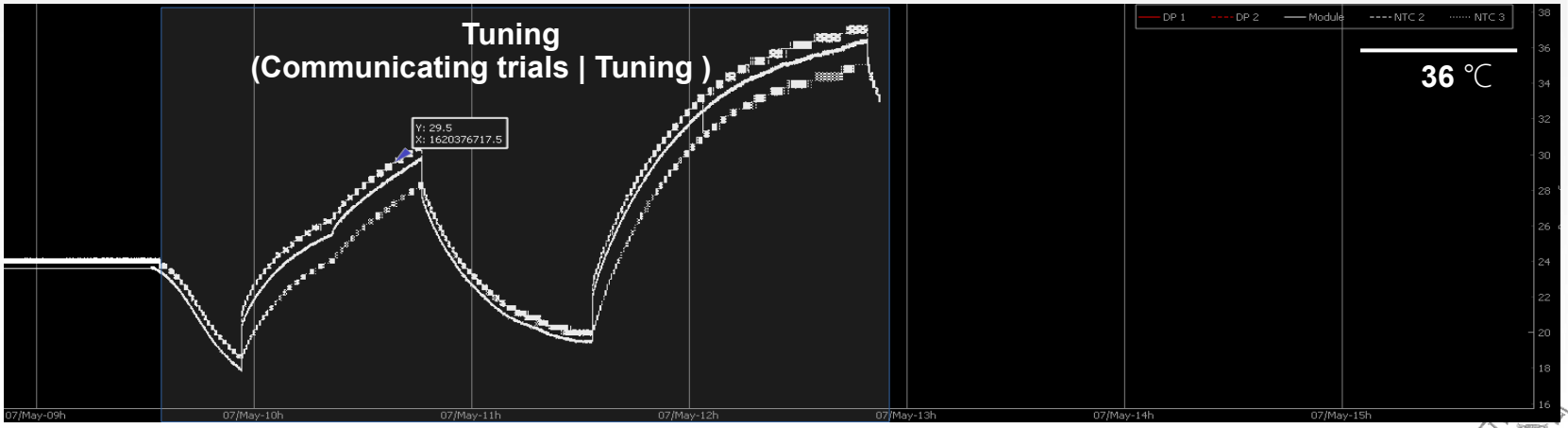
Temperature monitoring

- Monitoring of the NTC temperature of all 3 chips during operation
- Data lanes into pins on adapter card read by PCTM
- Interlock on chip 3 and monitor on 2 and 1
- VI-scan and trimming same day
- Tuning next day
- Never went above 38 ℃

VI-Scan

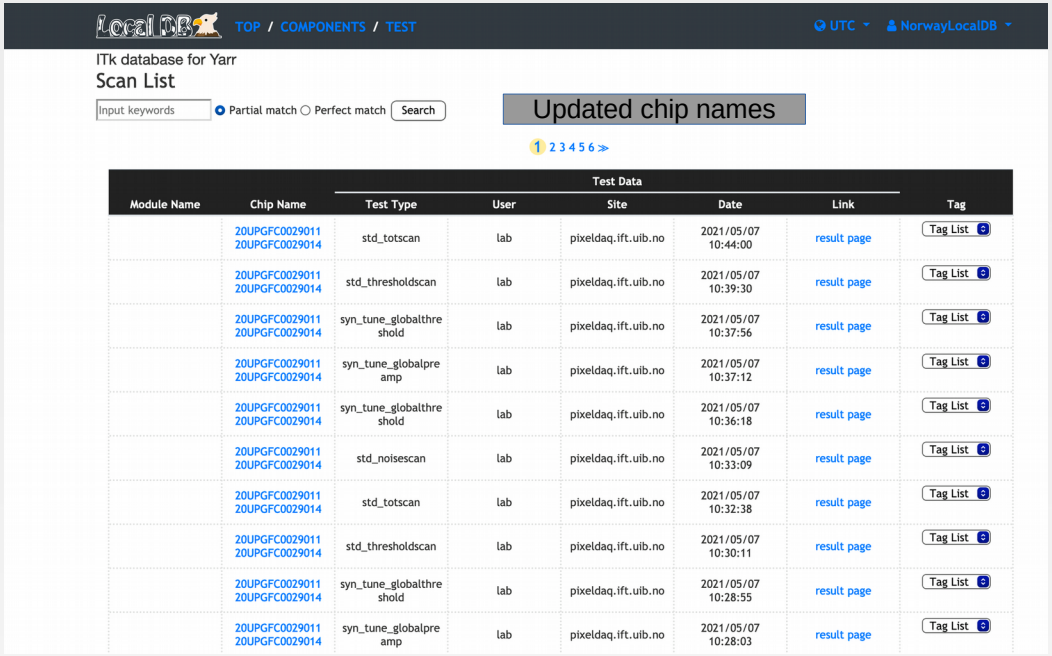


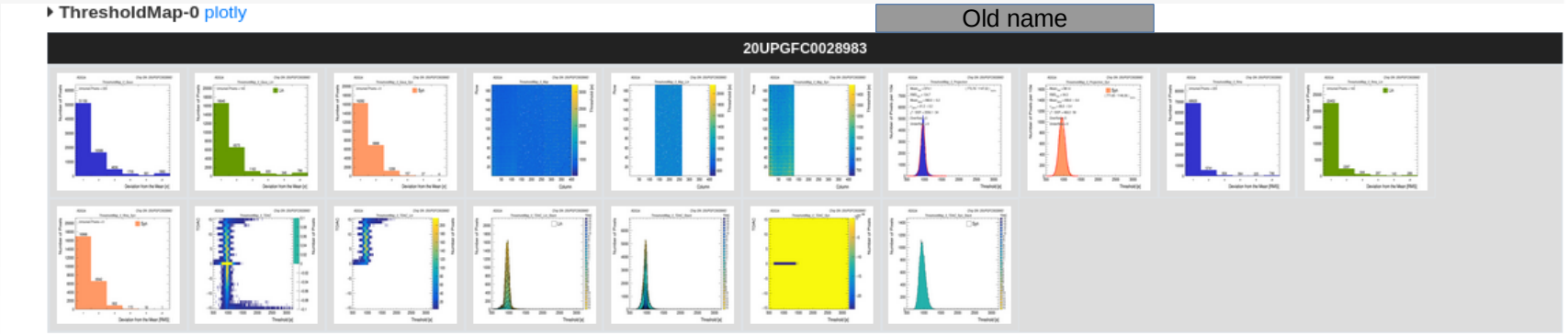




Upload to local DB

- Scan data from D4 was uploaded to local DB
- MongoDB and influxDB running on a server in Oslo: NREC cloud service from UiO
- Accessible from lab computers in Oslo and Bergen
  - Realized afterwards that we accidentally uploaded with wrong SN
  - Changed the SN with update command in MongoDB for component and componentTestRun:
    - db.componentTestRun.update({name:"OldSN", ($set:{name: "New_SN"}})





Summary

- **Bergen site qualification stage #1**
- Digital triplet D4 tested in Bergen
  - Visual inspection
  - VI-scan
  - VDDA/D voltage trimming
  - Tuning: 2000e for syn FE and 1000e (diff and linear), ToT 7 BC at 10ke
  - Scan data uploaded to LocalDB
  - NTC temperature monitoring (max: 38°C)

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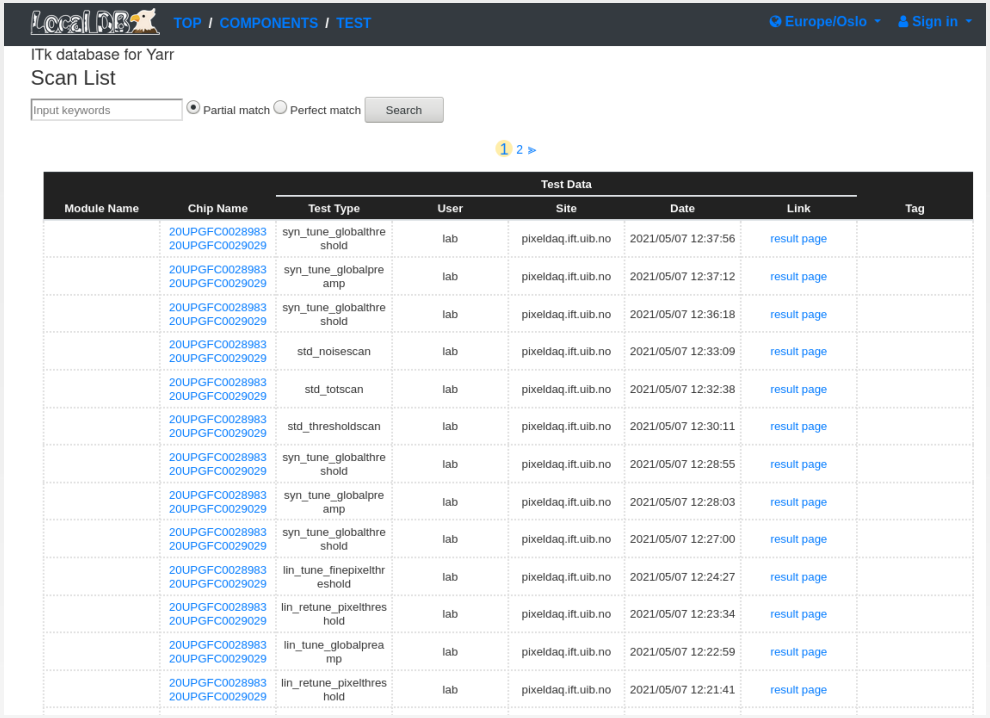
Backup slides

Probe data

	Chip A (3) 20UPGFC0029011	Chip B (2) 20UPGFC0029014	Chip C (1) 20UPGFC0029015
IREF trim bit	8	8	10
Result from link test	green	green	green
Value from link test	1	1	1
Result from VDDA trim	green	green	green
Value from VDDA after trimming	1.190297	1.195921	1.196162
VDDA trim bit	23	19	25
VDDA bit 16	1.117801	1.16845	1.090796

Measured Start-up VDDA [Volts]	Pull-up Resistor Required?	Pull-up Resistor Value [kΩ]	Expected increase in Start-up VDDA [Volts]
<= 1.09	Yes	150	0.1
>1.09 and <= 1.14	Yes	300	0.05
> 1.14	No	n/a	N/a

Fixing all SN in localDB



Module Name	Chip Name	Test Data: Test Type	User	Site	Date	Link	Tag
	20UPGFC0028983 20UPGFC0029029	syn_tune_globalthreshold	lab	pixeldaq.ift.uib.no	2021/05/07 12:37:56	result page	
	20UPGFC0028983 20UPGFC0029029	syn_tune_globalpreamp	lab	pixeldaq.ift.uib.no	2021/05/07 12:37:12	result page	
	20UPGFC0028983 20UPGFC0029029	syn_tune_globalthreshold	lab	pixeldaq.ift.uib.no	2021/05/07 12:36:18	result page	
	20UPGFC0028983 20UPGFC0029029	std_noisescan	lab	pixeldaq.ift.uib.no	2021/05/07 12:33:09	result page	
	20UPGFC0028983 20UPGFC0029029	std_totscan	lab	pixeldaq.ift.uib.no	2021/05/07 12:32:38	result page	
	20UPGFC0028983 20UPGFC0029029	std_thresholdscan	lab	pixeldaq.ift.uib.no	2021/05/07 12:30:11	result page	
	20UPGFC0028983 20UPGFC0029029	syn_tune_globalthreshold	lab	pixeldaq.ift.uib.no	2021/05/07 12:28:55	result page	
	20UPGFC0028983 20UPGFC0029029	syn_tune_globalpreamp	lab	pixeldaq.ift.uib.no	2021/05/07 12:28:03	result page	
	20UPGFC0028983 20UPGFC0029029	syn_tune_globalthreshold	lab	pixeldaq.ift.uib.no	2021/05/07 12:27:00	result page	
	20UPGFC0028983 20UPGFC0029029	lin_tune_finepixelthreshold	lab	pixeldaq.ift.uib.no	2021/05/07 12:24:27	result page	
	20UPGFC0028983 20UPGFC0029029	lin_retune_pixelthreshold	lab	pixeldaq.ift.uib.no	2021/05/07 12:23:34	result page	
	20UPGFC0028983 20UPGFC0029029	lin_tune_globalpreamp	lab	pixeldaq.ift.uib.no	2021/05/07 12:22:59	result page	
	20UPGFC0028983 20UPGFC0029029	lin_retune_pixelthreshold	lab	pixeldaq.ift.uib.no	2021/05/07 12:21:41	result page	

2021-05-18T13:30:16.370+0000 I NETWORK [conn160] received client metadata from 127.0.0.1:55882 conn160: { driver: { name: "PyMongo", version: "3.11.3" }, os: { type: "Linux", name: "Linux", architecture: "x86_64", version: "3.10.0-1160.24.1.el7.x86_64" }, platform: "CPython 3.6.8.final.0" }
2021-05-18T13:30:16.382+0000 I ACCESS [conn160] Successfully authenticated as principal c4963a8d622baa06633c2a43ab68890e on localdb from client 127.0.0.1:55882

```
[15:40:31:896][ info ][ Local DB ]: ----------------------------
[15:40:31:896][ info ][ Local DB ]: Function: Upload scan data from specified directory
[15:40:31:897][ info ][ Local DB ]: Cache Directory: /home/lab/Desktop/Yarr_QA/YARR/data/002107_std_totscan
[15:40:31:897][ info ][ Local DB ]: -> Setting user config: scanLog.json
[15:40:31:898][ info ][ Local DB ]: -> Setting site config: scanLog.json
[15:40:31:940][ info ][ Local DB ]: -> Setting database config: scanLog.json
[15:40:31:940][ info ][ Local DB ]: Checking connection to DB Server: mongodb://127.0.0.1:27017/localdb ...
[15:40:31:945][ info ][ Local DB ]: ---> Good connection!
[15:40:31:949][ info ][ Local DB ]: Loading user information ...
[15:40:31:949][ info ][ Local DB ]: ~~~ {
[15:40:31:949][ info ][ Local DB ]: ~~~     "name": "lab",
[15:40:31:950][ info ][ Local DB ]: ~~~     "institution": "pixeldaq.ift.uib.no"
[15:40:31:950][ info ][ Local DB ]: ~~~ }
[15:40:31:950][ info ][ Local DB ]: Loading site information ...
[15:40:31:950][ info ][ Local DB ]: ~~~ {
[15:40:31:950][ info ][ Local DB ]: ~~~     "institution": "pixeldaq.ift.uib.no"
[15:40:31:950][ info ][ Local DB ]: ~~~ }
[15:40:31:950][ info ][ Local DB ]: Loading component information ...
[15:40:31:950][ info ][ Local DB ]: ~~~ {
[15:40:31:950][ info ][ Local DB ]: ~~~     "parent": {
[15:40:31:950][ info ][ Local DB ]: ~~~         "serialNumber": "D4",
[15:40:31:950][ info ][ Local DB ]: ~~~         "componentType": "Module"
[15:40:31:950][ info ][ Local DB ]: ~~~     },
[15:40:31:950][ info ][ Local DB ]: ~~~     "children": [{
[15:40:31:950][ info ][ Local DB ]: ~~~         "serialNumber": "20UPGFC0029011",
[15:40:31:950][ info ][ Local DB ]: ~~~         "componentType": "front-end_chip",
[15:40:31:950][ info ][ Local DB ]: ~~~         "chipId": "3",
[15:40:31:950][ info ][ Local DB ]: ~~~     },{
[15:40:31:950][ info ][ Local DB ]: ~~~         "serialNumber": "20UPGFC0029014",
[15:40:31:950][ info ][ Local DB ]: ~~~         "componentType": "front-end_chip",
[15:40:31:950][ info ][ Local DB ]: ~~~         "chipId": "2",
[15:40:31:950][ info ][ Local DB ]: ~~~     }],
[15:40:31:950][ info ][ Local DB ]: ~~~     "stage": "Testing"
[15:40:31:951][ info ][ Local DB ]: ~~~ }
[15:40:31:956][warning ][ Local DB ]: Already registered test run data in DB
[15:40:32:144][ info ][ Local DB ]: Succeeded uploading scan data from /home/lab/Desktop/Yarr_QA/YARR/data/002107_std_totscan
[15:40:32:144][warning ][ Local DB ]: Scan data that has not been uploaded is listed in /root/.yarr/localdb/run.dat
[15:40:32:144][ info ][ Local DB ]: ----------------------------
```