



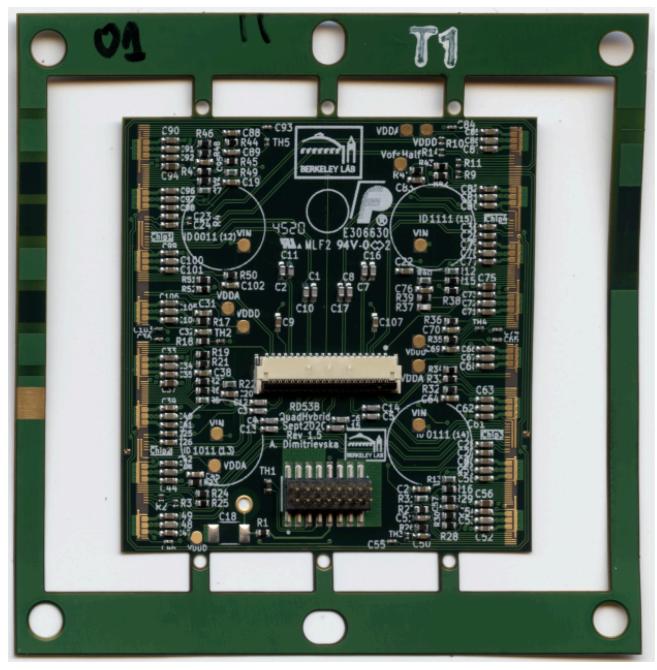
- Student Instrumentation Meeting-

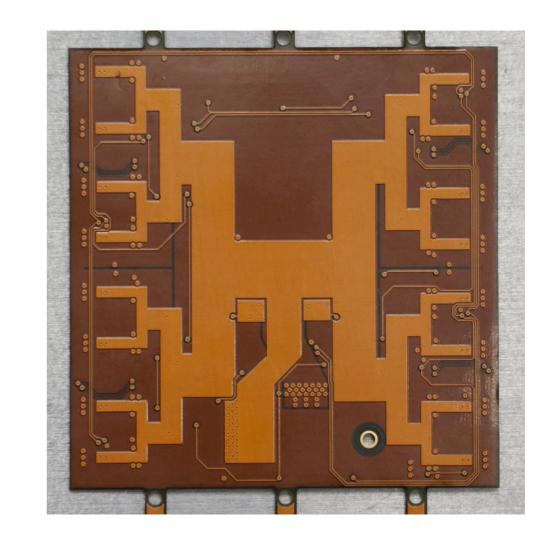
January 22, 2021

<u>Aleksandra Dimitrievska</u>, Timon Heim Lawrence Berkeley National Laboratory

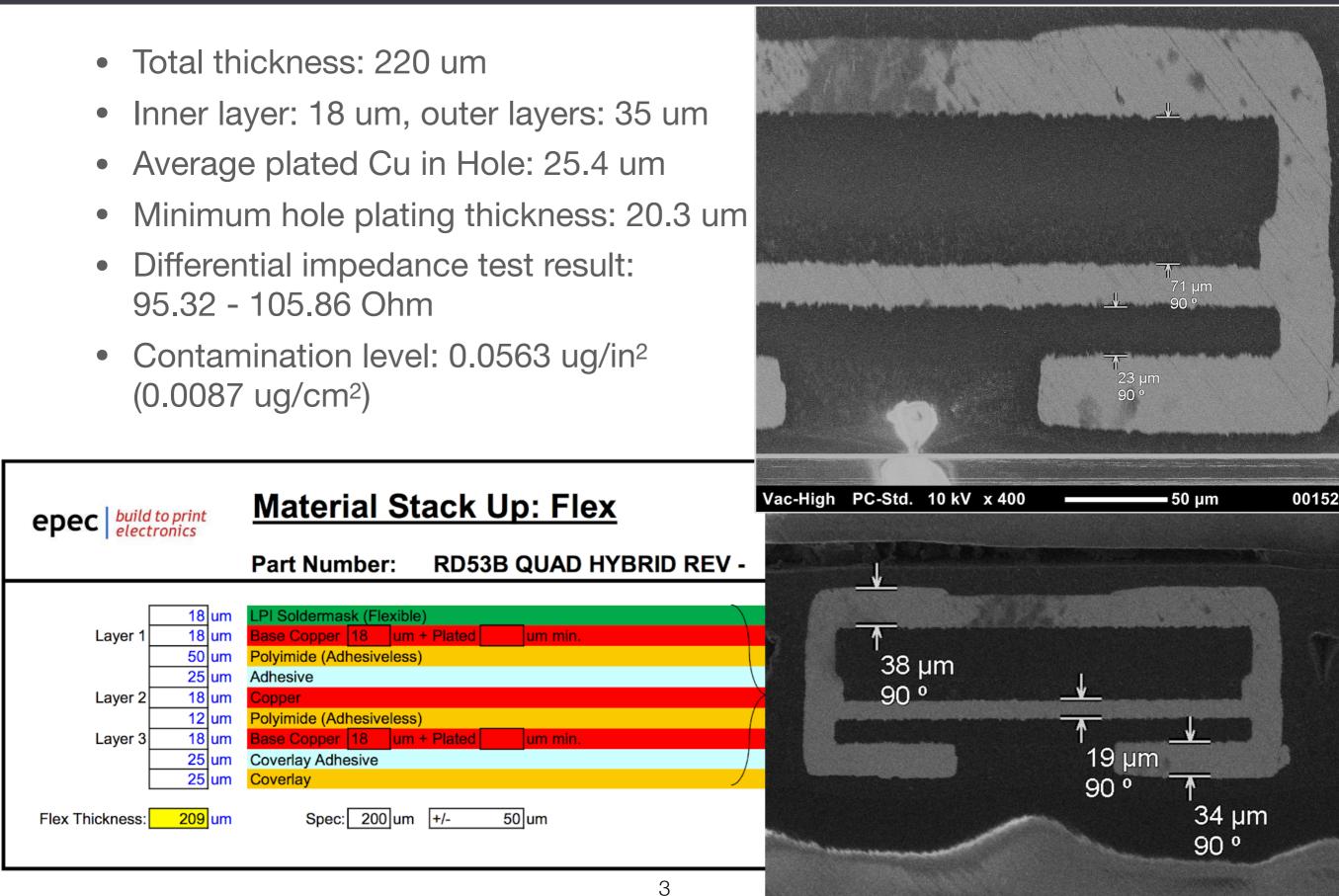
### Quad design for the first prototypes

- Quad Modules for ITk Pixel
- GitLab Design Files
- 3-layer design





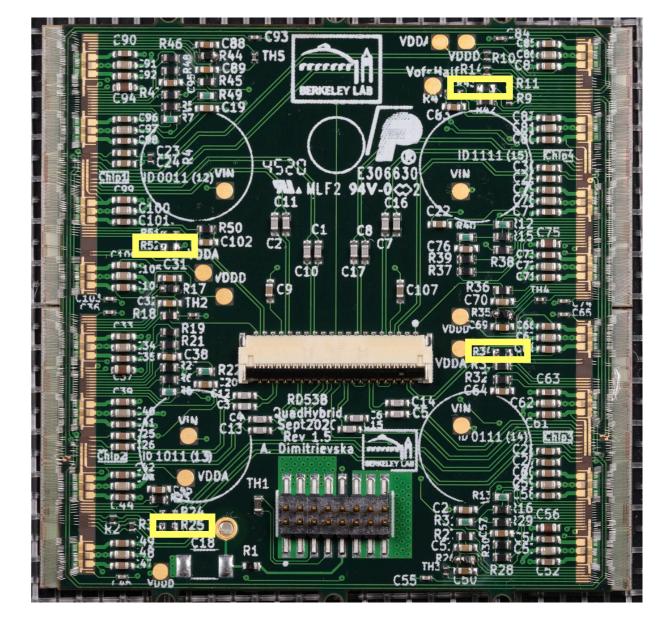
### Quad design for the first prototypes



### • First Digital Quads with ITkPixV1 Chips

Hybrid	Chip1 Id	Chip2 Id	Chip3 Id	Chip4 Id	Configuration	
02	0x10A98	0x10A88	0x10A89	0x10A99	LDO	
03	0x10AB8	0x10AA8	0x10AA9	0x10AB9	LDO	
04	0x10ABA	0x10AAA	0x10AAB	0x10ABB	LDO	
05	0x10A9A	0x10A8A	0x10A8B	0x10A9B	LDO	
<ul> <li>Glueing by hand</li> </ul>						

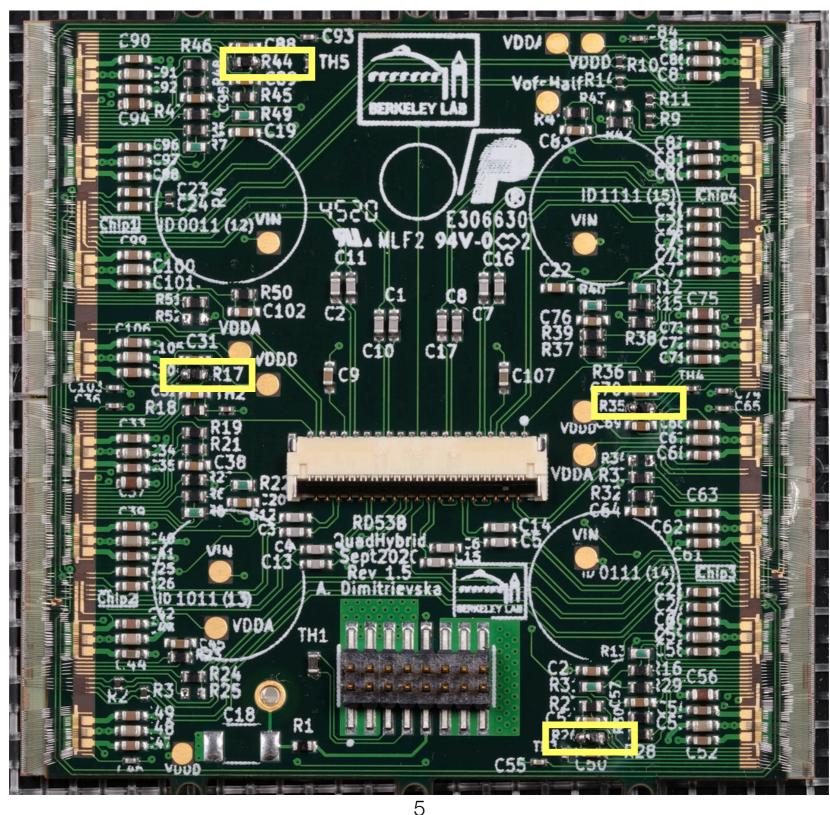
- Glueing by hand (no tooling used)
- ITkPixV1 chips are not probed
- LDO powering, ShuntEn resistor removed
- Reminder there is a bug in ToT memories which induces high digital current



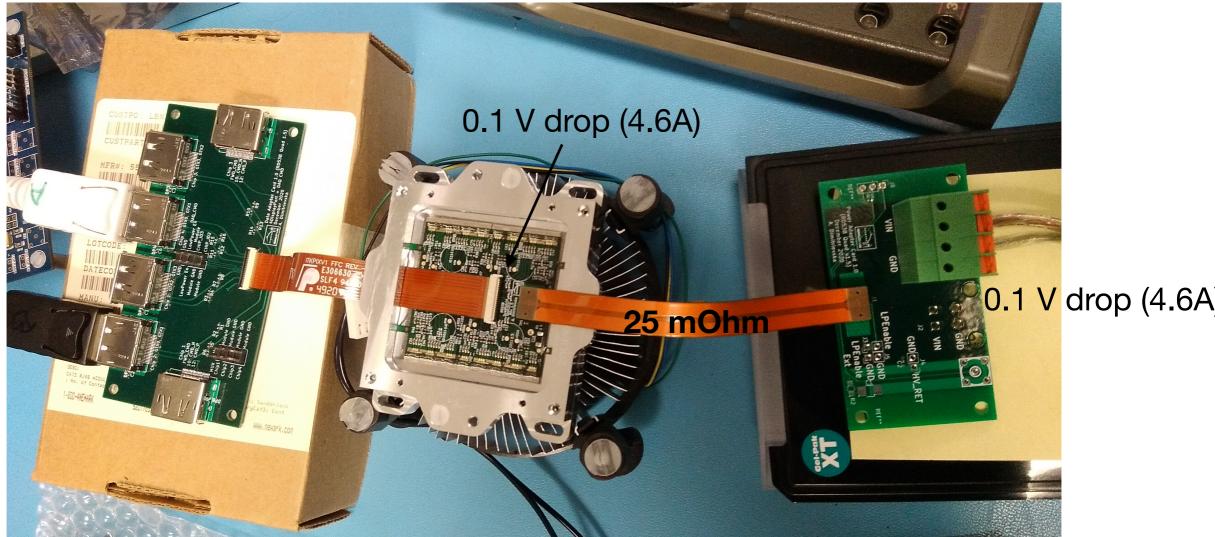
<u>HighRes Image</u>

 ITkPixV1.1 probed chips with bug fix should arrive soon at LBL

• There is a bug in the value of one loaded resistor 84.5->84.5k Ohm

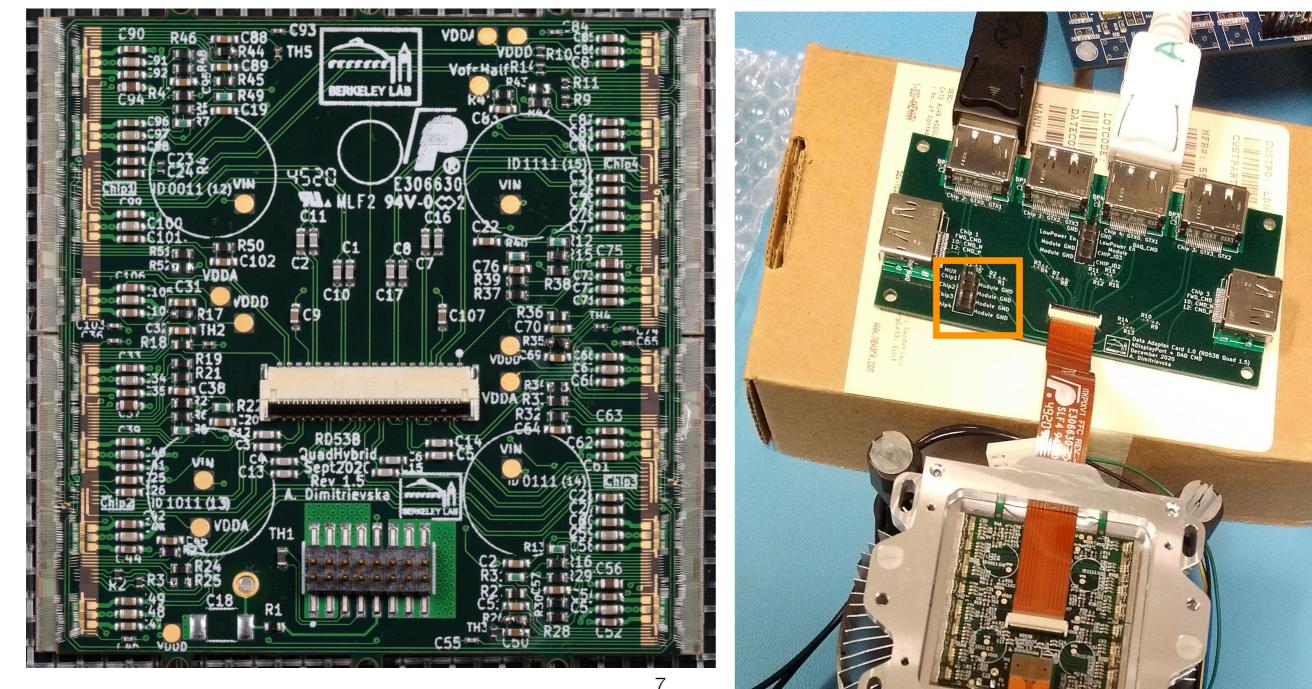


• The setup



- First tested digital quad (02) has some wire bonding bugs, has high current consumption 14 A
- Other two digital quads (03 and 04) are working as expected, depending on configuration settings, the current is about 1 - 1.2 A per chip
- Quad 05 not tested yet

- Vdda/Vddd measure
  - Probe pads on the module
  - Measure from the MUX on the pinheaded on adapter card



• Tuning procedure

**Threshold Distribution** 

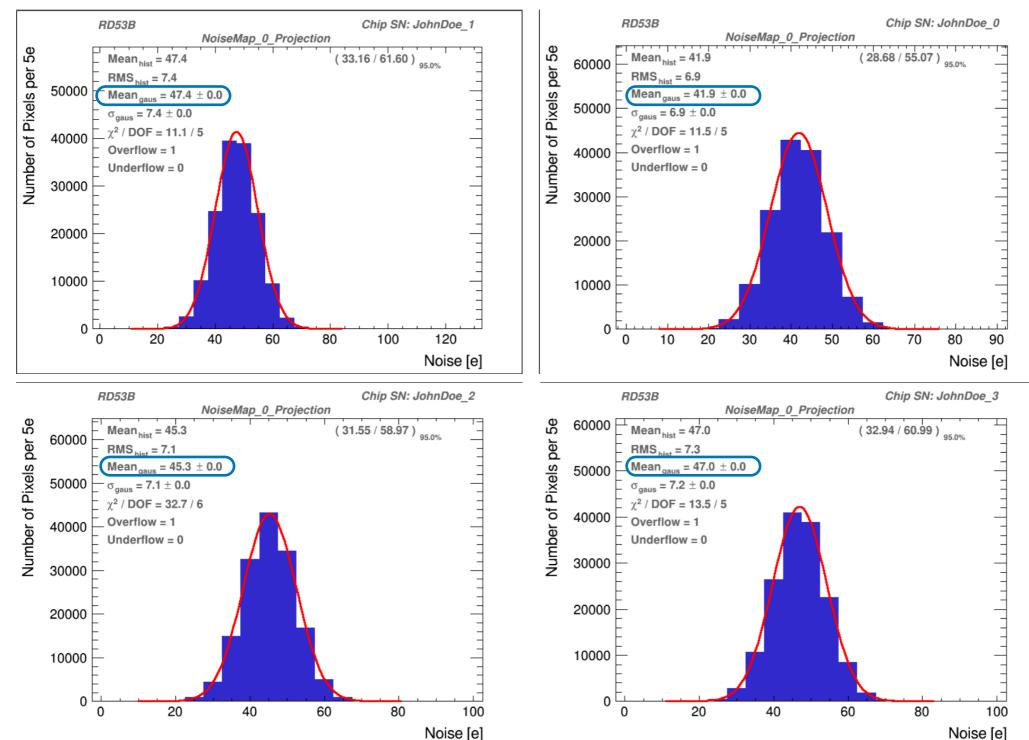
>/ptot\_digitalscan.json -p -n 1 >/ptot\_analogscan.json -p -n 1 >/ptot\_tune\_globalthreshold.json -t 1500 -p -n 1 >/ptot\_tune\_pixelthreshold.json -t 1500 -p -n 1 >/ptot\_retune\_globalthreshold.json -t 1000 -p -n 1 >/ptot\_retune\_pixelthreshold.json -t 1000 -p -n 1 >/ptot\_tretune\_pixelthreshold.json -t 1000 -p -n 1

#### RD53B Chip SN: JohnDoe 1 RD53B Chip SN: JohnDoe\_0 ThresholdMap 0 Projection ThresholdMap 0 Projection Number of Pixels per 10e 10e ( 888.15 / 1032.82 ) 95.0% ( 898.57 / 1037.94 ) 95.0% 30000 Mean<sub>hist</sub> = 960.3 Mean<sub>bist</sub> = 967.9 RMS<sub>bist</sub> = 36.0 RMS hist = 35.5 per 25000 $Mean_{gaus} = 968.3 \pm 0.1$ $Mean_{gaus} = 960.5 \pm 0.1$ 25000 Pixels $\sigma_{gaus} = 34.4 \pm 0.1$ $\sigma_{gaus} = 33.6 \pm 0.1$ $\chi^2$ / DOF = 2404.3 / 18 $\chi^2$ / DOF = 843.5 / 18 20000 ď 20000 Overflow = 1 Overflow = 1 Underflow = 0 Number Underflow = 015000 15000 10000 10000 5000 5000 0 0 900 1000 1100 1200 1300 800 1200 1400 1600 600 700 800 600 1000 500 Threshold [e] Threshold [e] Chip SN: JohnDoe\_3 RD53B Chip SN: JohnDoe\_2 RD53B ThresholdMap 0 Projection ThresholdMap 0 Projection 10e (899.95 / 1035.78 ) 10e ( 898.65 / 1035.67 ) 95.0% 30000 Mean<sub>hist</sub> = 967.7 30000 - Mean ist = 967.1 RMS<sub>biot</sub> = 34.6 RMS<sub>biot</sub> = 35.3 Number of Pixels per of Pixels per $Mean_{gaus} = 967.9 \pm 0.1$ $Mean_{gaus} = 967.2 \pm 0.1$ 25000 25000 $\sigma_{gaus} = 32.9 \pm 0.1$ $\sigma_{gaus}$ = 32.0 $\pm$ 0.1 $\chi^2$ / DOF = 1720.7 / 16 $\chi^2$ / DOF = 1333.0 / 17 20000 Overflow = 120000 Overflow = 0 Number Underflow = 0Underflow = 015000 15000 10000 10000 5000 5000 0 0 400 600 800 1000 1200 600 800 1000 1200 1400 1600 Threshold [e] Threshold [e]

• Tuning procedure

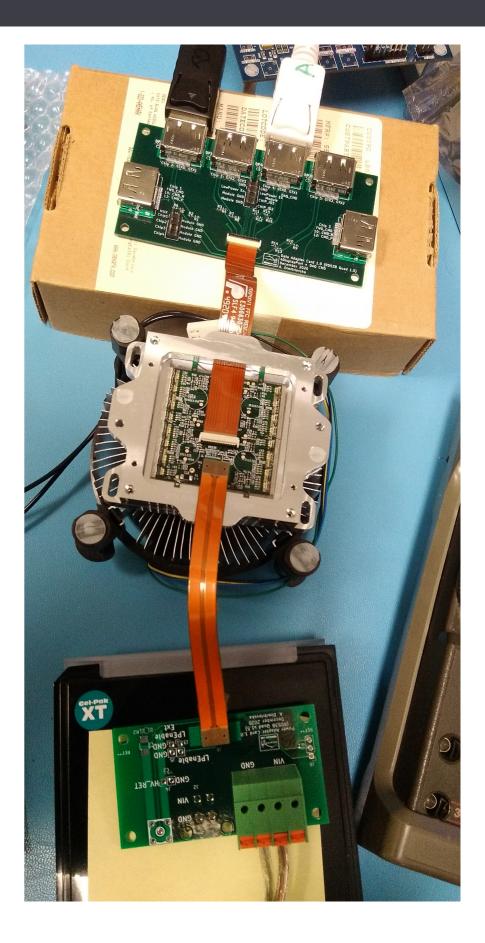
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#### **Noise Distribution**



## Summary

- 25 quad prototype hybrids produced
- 50 data and power pigtails produced
- 10 data and power adapter cards produced
- First ITkPixV1 Digital Quads
   assembled
- Initial tests show that everything is working as expected
- Working on Iref calibration for unprobed chips
- Expected to build and test ITkPixV1.1 digital quads in the next weeks



BACKUP

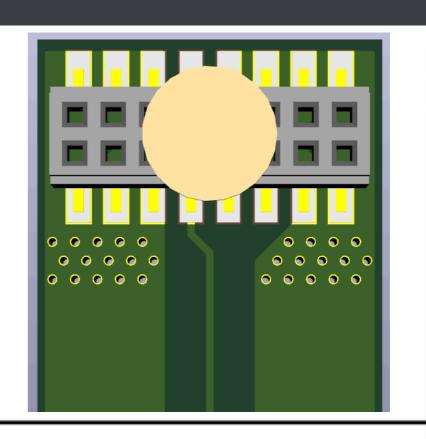
### Quad Data pigtail

- Custom 10 cm long data pigtail with 100 Ohm controlled differential impedance (2-layer design)
- <u>GitLab design files</u>
- 50 produced (20\$)

epec build to print electronics	Material Stack Up: Flex Part Number: ITKPIXV1 FFC				
25 um 25 um Layer 1 18 um 50 um	Coverlay Coverlay Adhesive Base Copper 18 um + Plated um min.	ness ZIF			
Layer 2 18 um 25 um 25 um 25 um 50 um	Coverlay Adhesive Coverlay Adhesive	Adhesive PI Stiffener			
Flex Thickness: 186 um ZIF Thickness: 211 um					
Created By: PT Date: 10/22/2020					

## Quad Power pigtail

- 10 cm long, custom power pigtail (2-layer)
- 1.5 oz of copper to reduce the voltage drop
- <u>GitLab design files</u>
- 50 produced (20\$)

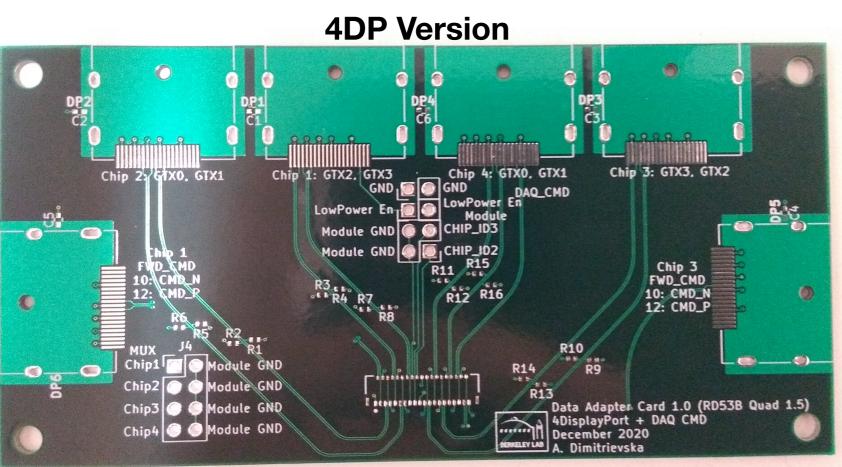


Dote

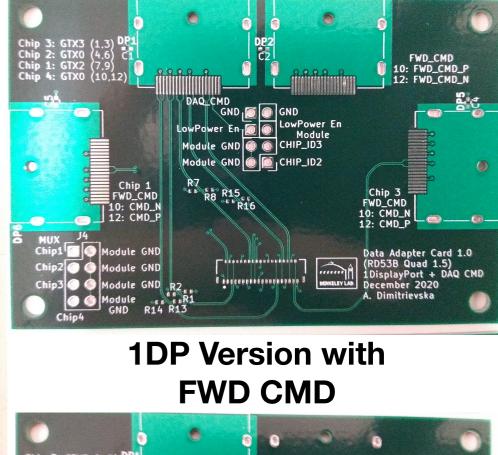
epec build to print electronics	Material Stack Up: Flex					
	Part Number: ITKPIXV1 POWER REV -					
25 um	Coverlay					
50 um	Coverlay Coverlay Adhesive					
Layer 1 47 um	Base Copper 35 um + Plated 12 um min.					
25 um	Polyimide (Adhesiveless) Flex Thickness					
Layer 2 47 um	Base Copper 35 um + Plated 12 um min.		Total			
<u>50</u> um	Coverlay Adhesive		/ Thickness			
<u>25</u> um	Coverlay	A dia si sa				
<u>50</u> um	Adhesive	Adhesive				
500 um	FR4 Stiffener	FR4 Stiffener				
		2				
Total Thickness: 819 um	Spec: 800 um +/- 100 um					
Flex Thickness: 269 um	Spec: 250 um +/- 50 um					

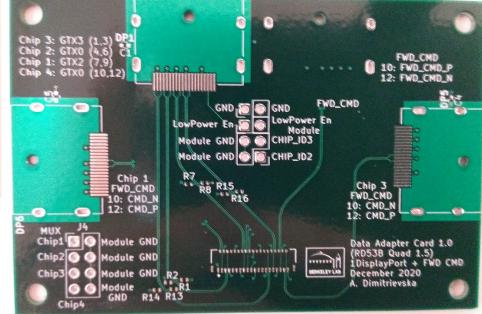
### Quad Data Adapter cards

- 4-layer design, ~100 Ohm differential impedance (impedance is not controlled)
- GitLab design files
- 10 produced



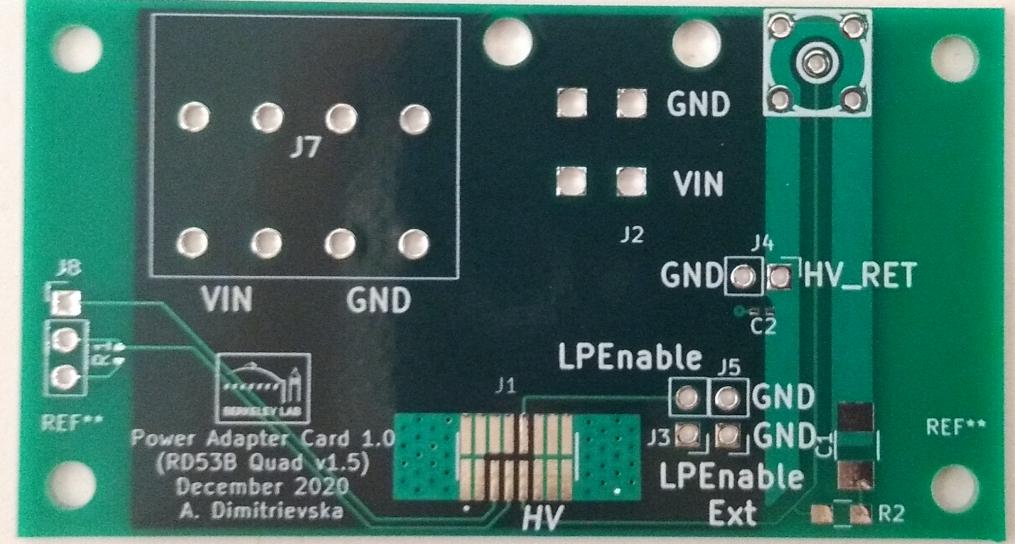
**1DP Version** 



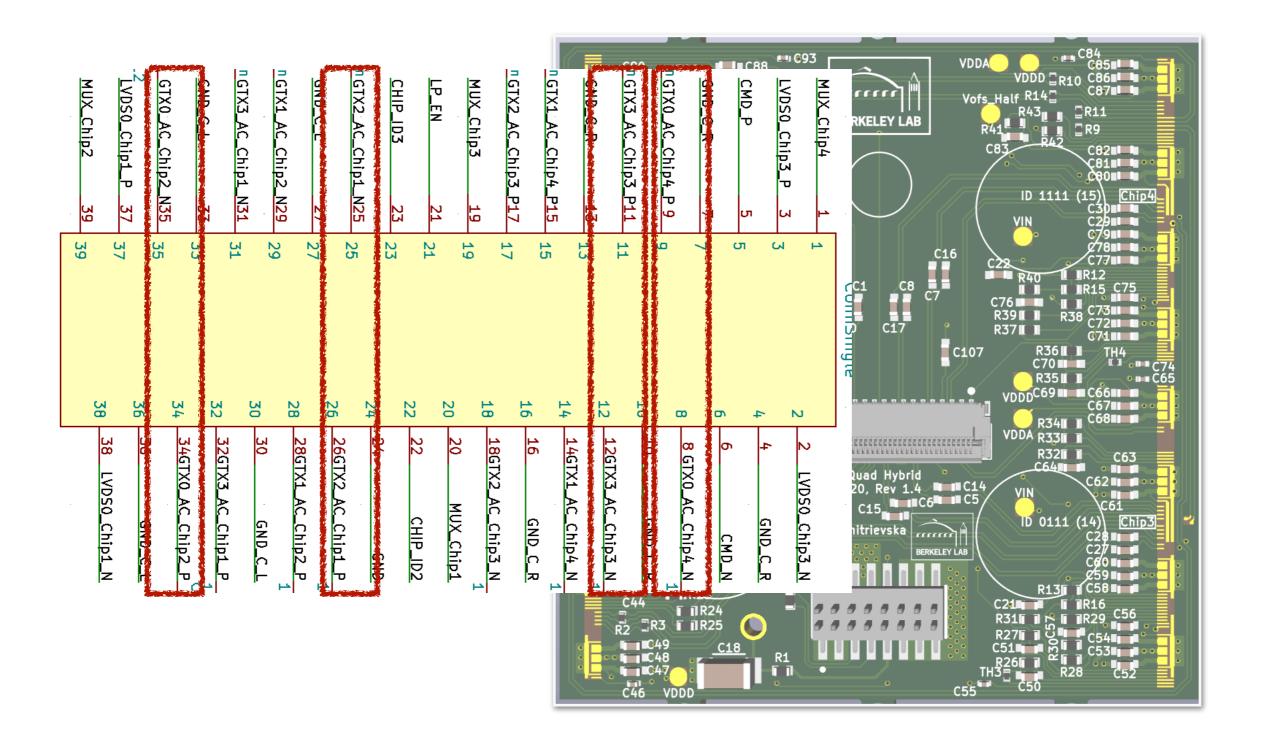


### **Quad Power Adapter cards**

- 4-layer design, 10 produced
- Choice of LV connector
  - Molex (as on SCC)
  - Terminal block
- <u>GitLab design files</u>



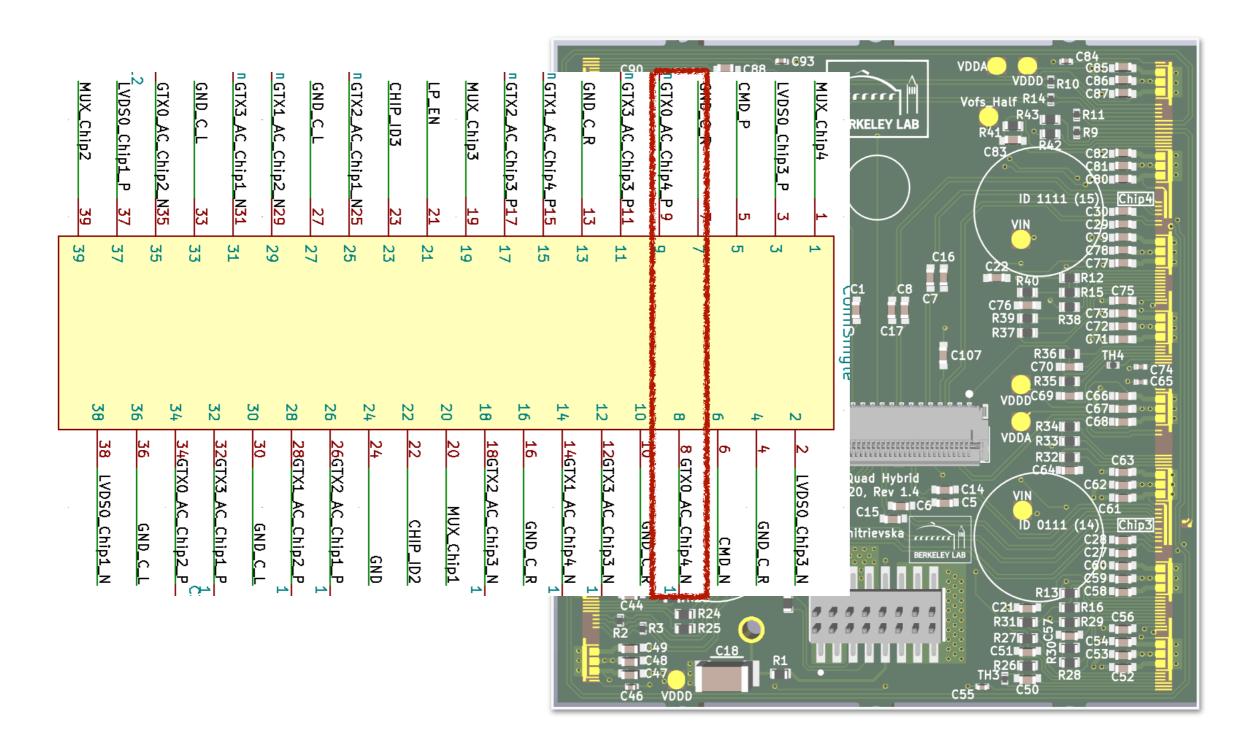
### Data Sharing (1 link per FE)



## Data Sharing (0.5 link per FE)

2 LVDSO_Chip1_P 37 MUX_Chip2 39	GTX0_AC_Chip2_N35	nGTX1_AC_Chip2_N29 nGTX3_AC_Chip1_N31	C_L	LP_EN 21 CHIP_103 23	MUX_Chip3_19	GND_C_R 13	IGTX0_AC_Chip4_P 9	MUX_Chip4 5 3	VDDA       C84 C85         VDDD R10 C86         Vofs_Half R14         R43         R43         R43         R43         R43         C87         R43         R43         C83         C83         C83         C83         C84         C83         C84         C83         C84         C83         C84         C84         C83         C90         ID 11111 (15)         Chip4         VIN         C29
37 39 39	33 35	29 31 32	25 27 27 28	21 21 23 23	15 17 17 18	10 11 13 13	9 <b>-</b>	4 IS 5 4 D	C16 C22 R40 R40 R12 C77 C77 R39 R39 R38 C73 C73 C76 R39 R38 C73 C77 C76 R39 R38 C73 C77 C77 C77 C77 C77 C77 C77
38 LVDSO_Chip1_N	GTXO_A	30 GND_C_L 32GTX3_AC_Chip1_P	26GTX2_AC_Chip1_P 1 28GTX1_AC_Chip2_P	20 MUX_Chip1 22 CHIP_ID2 24 GND	16 GND <u>C_R</u> 18GTX2_AC_Chip3_N 1	12GTX3_AC_Chip3_N 12GTX1_AC_Chip4_N	GTX0_AC_Chip4_N	6 4 2 LVDSO_Chip3_N GND_C_R CMD_N 24 25 C18 R1	WDA       R34       C68         WDA       R33       R32         R32       C63         C15       C6       C5         Nitrievska       C27       C60         BERKELEY LAB       C27       C60         R13       C58         C21       R13       C58         R27       C58       C21         R13       C58       C21         R27       C58       C53         C21       R16       C54         C51       C54       C53         C55       C50       C54

### Data Sharing (0.25 link per FE)



### **CMD** Forwarding

- Chip 1 and Chip3 can forward the CMD
- ChipID of the forwarded module should be changed

