RD53 Status ans Plans

Pixel readout integrated circuits for extreme rate and radiation

6th LHCC Report- Sept. 11, 2019

M. Garcia-Sciveres (LBNL) on behalf of the RD53 Collaboration

Previously on RD53

- Focused R&D to develop pixel chips for both ATLAS and CMS upgrades
- Established in 2013 recognizing that HL-LHC pixel requirements were extremely challenging, yet very similar for both experiment, and a joint effort was the best way to meet them
- Successful R&D culminated in the RD53A prototype chip, fabricated at the end of 2017. This fulfilled the original mandate of RD53.
  - RD53A continues to be extensively used by both experiment to prototype their HL-LHC detectors. 110 RD53A wafers have been purchased to date – 3x as many pixels as current ATLAS and CMS combined.
- At the request of the experiments, last year the mandate of RD53 was extended to design the final production chips for ATLAS and CMS
  - Keep the design team together.
  - Pursue as much as possible a common design to serve the needs of both experiments.
- RD53 has 22 collaborating institutes and many Guests
  - ~100 conference talks/proceedings/papers to date

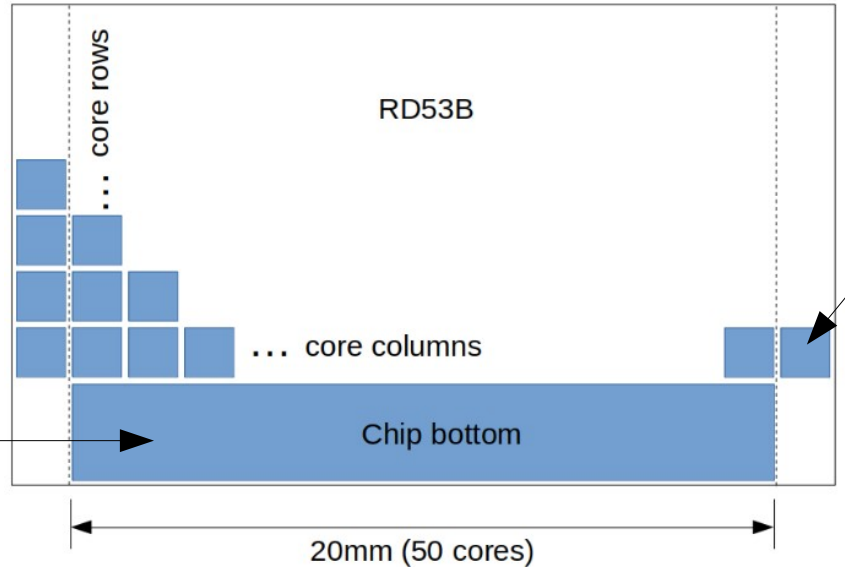
The Most Important Aspect of RD53

The people

RD53 Designs and Chips

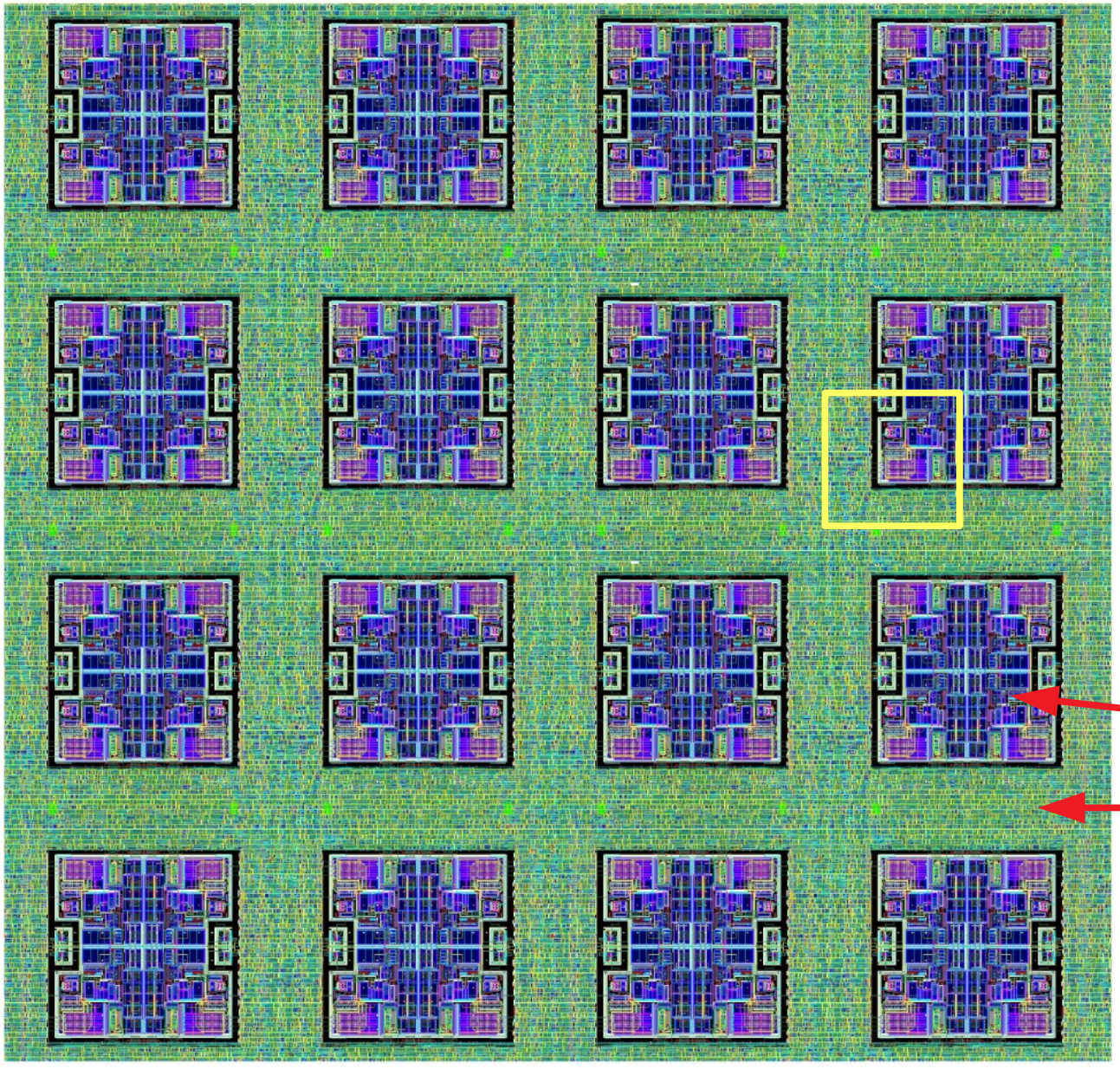
- RD53A is the existing prototype
- RD53B is not a physical chip. It is a design library / environment
- The first incarnation of RD53B will be RD53B-ATLAS (which ATLAS calls ItkPix-V1) To be fabricated this fall.
- The second incarnation will be RD53B-CMS, to be fabricated in 2020 (may be able to take advantage of initial RD53B-ATLAS test results)
- Each chip is made of two RD53B elements: the chip bottom and a matrix of identical “cores”. Each core has 64 pixels .

This is the same for both ATLAS and CMS
All global functions, I/O, power, control, etc. are in here



The main difference between ATLAS and CMS is the number of cores.
The analog front end Inside the core is also different.
The environment was designed to handle such variation.

One Core



One flat synthesized circuit

~ 200k transistors

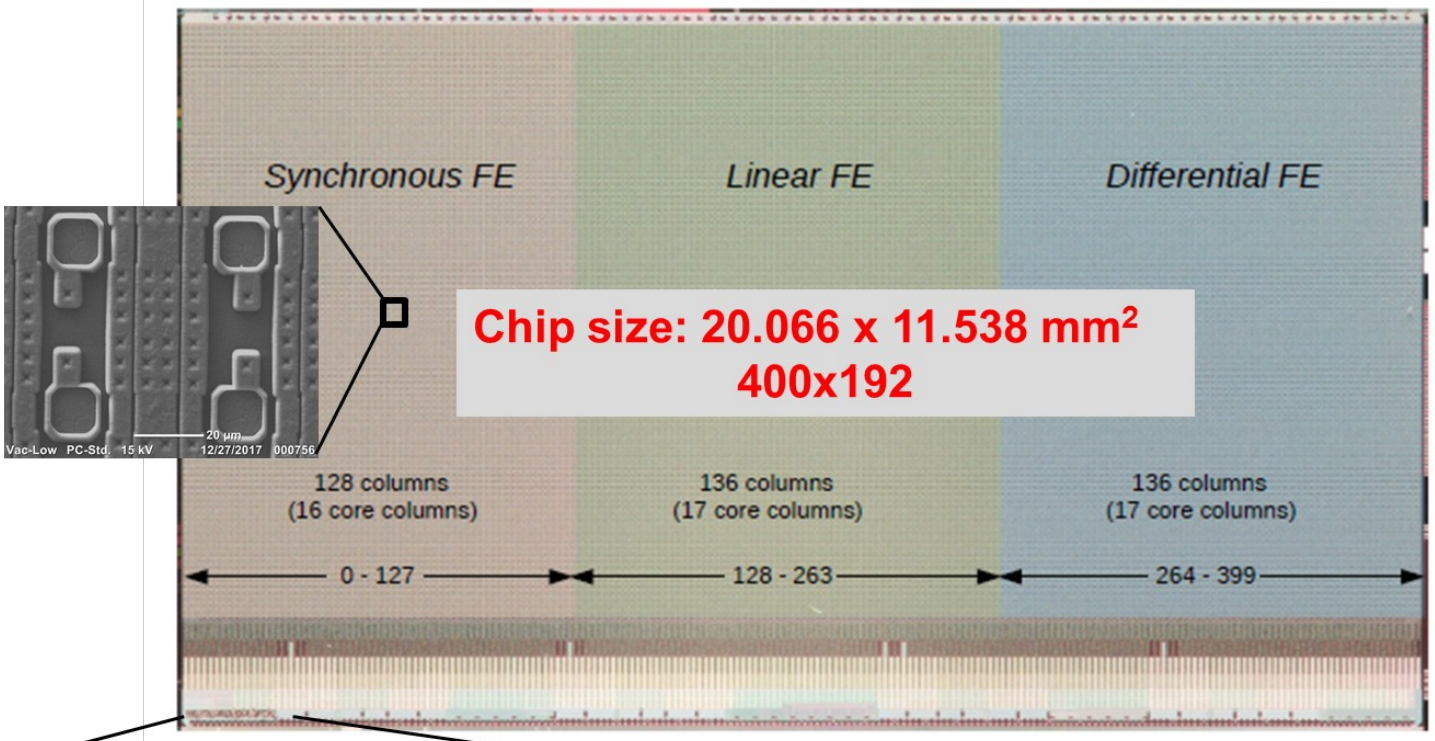
64 pixels in 16 “analog islands”

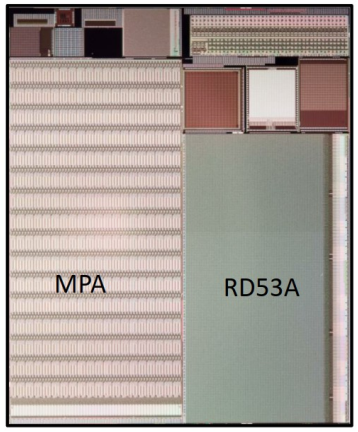
Whole core is stepped and repeated to make the pixel matrix

Hand-drawn transistors

“compiled software”

RD53A



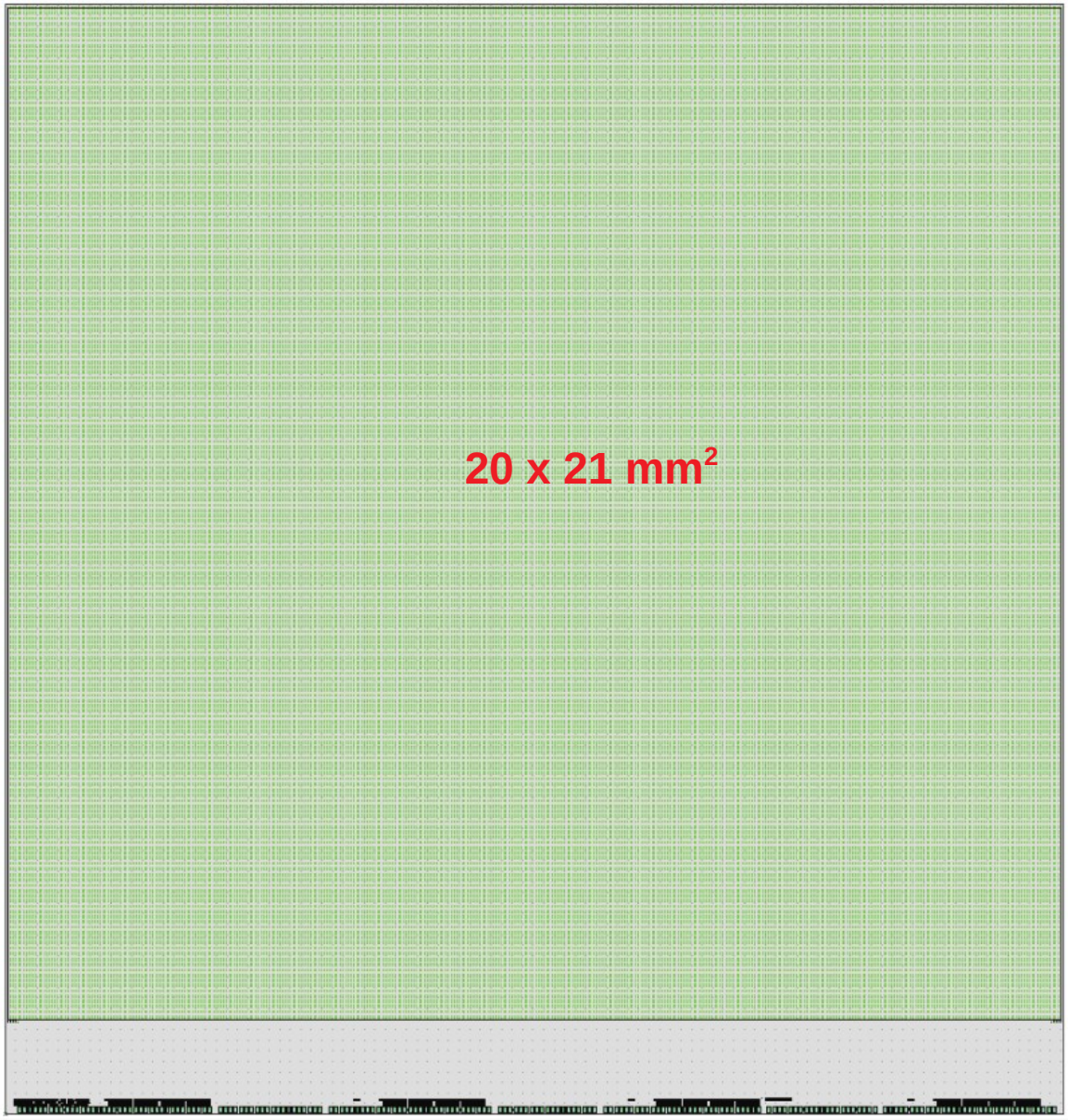


MPW together with
CMS tracker chips

- **Aug. 31, 2017: Submission**
- **Dec. 6, 2017: First chip test**
- **Mar. 15, 2018: 25 wafers ordered**
- **Apr. 13, 2018: First bump-bonded chip test**

Chip doc on CDS: http://cds.cern.ch/record/2287593

RD53B

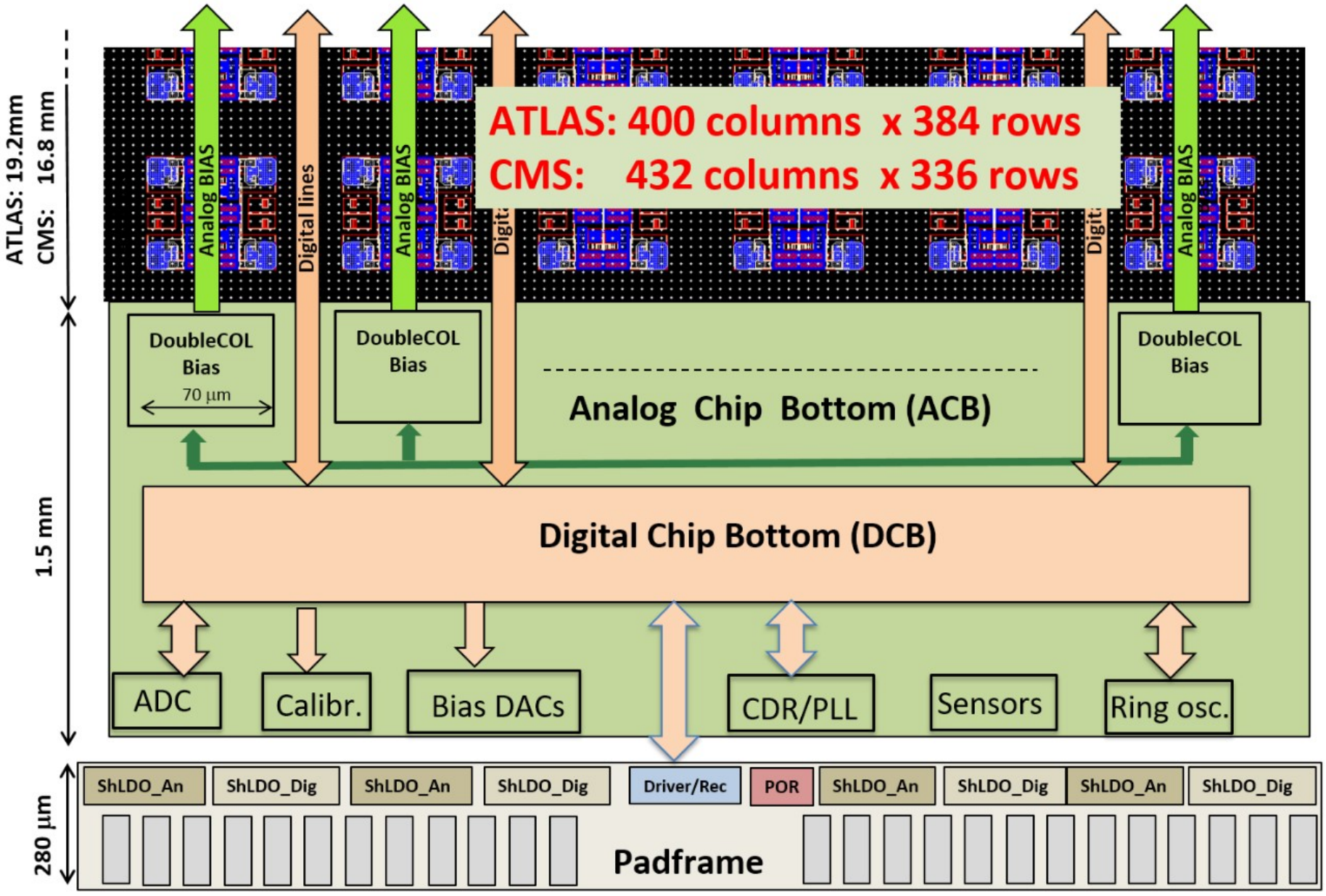


RD53B Basic Specs

Technology	65 nm CMOS
Pixel size	50x50 um^2 & 25x100 um^2
Pixels (ATLAS/CMS)	400 x 384 = 163,600 / 432 x 336 = 145,152
Detector capacitance	< 100 fF (200 fF for edge pixels)
Detector leakage worst case	< 10n A (20 nA for edge pixels)
Detection threshold	<600 e-
In-time threshold	<1200 e-
Noise hits	< 10^{-6}
Hit rate	< 3 GHz/cm^2 (75 kHz avg. per pixel)
Trigger	1 or 2-level configurable. Tag-based
Max. 1-level readout rate	>4 MHz
Max. 2-level readout rate	~1 MHz
1-level max. latency	12.5 us
2nd level max. latency	25 us
Hit loss at max hit rate	≤ 1%
Charge readout / resolution	4 bit readout / 6-bit to 4-bit @ 80 MHz
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Radiation tolerance	500 Mrad at -15°C
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1 W/cm^2 including ShLDO losses
Pixel analog/digital current	3-5uA/3uA
Temperature range	-40°C ÷ 40°C

See requirements doc: https://cds.cern.ch/record/2663161 and manual: https://cds.cern.ch/record/2665301

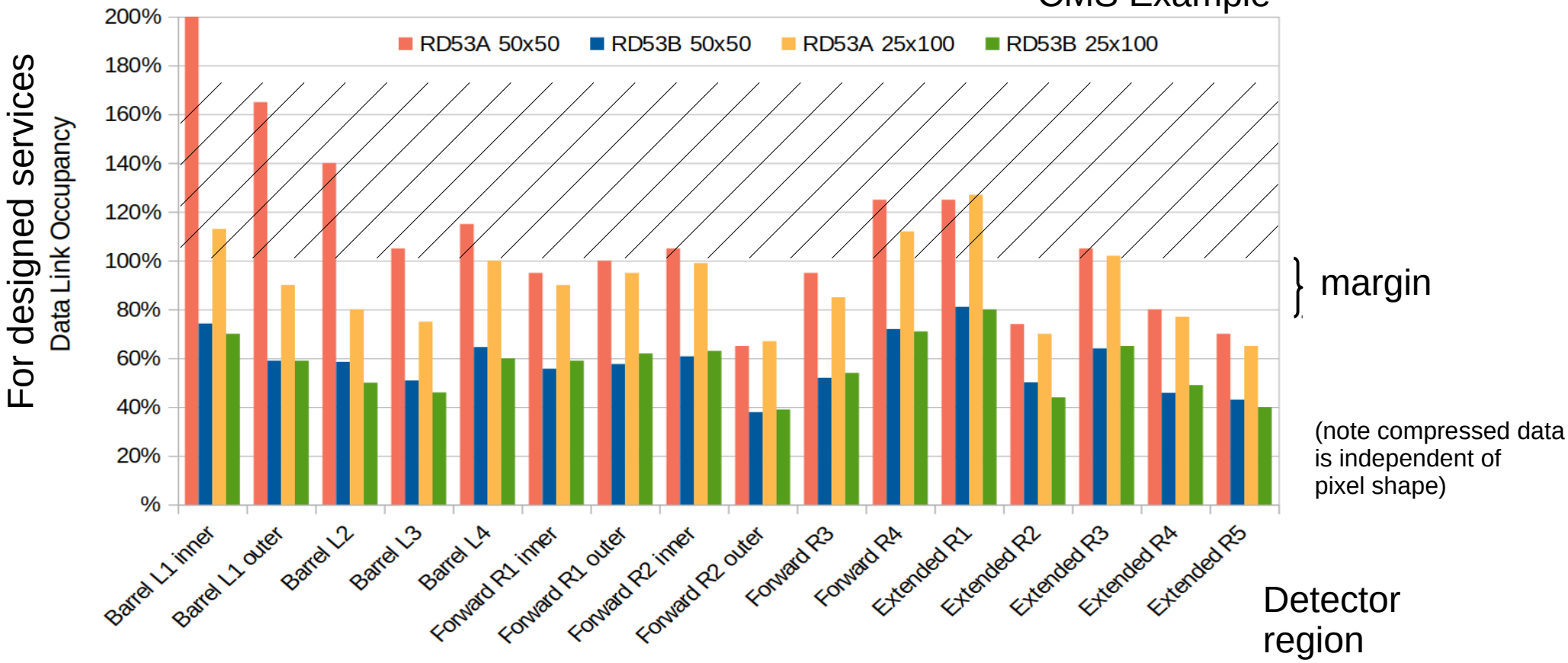
RD53B


ATLAS: 19.2mm
CMS: 16.8 mm
1.5 mm
280 µm
Analog BIAS
Digital lines
Analog BIAS
Digital lines
Analog BIAS
ATLAS: 400 columns x 384 rows
CMS: 432 columns x 336 rows
DoubleCOL Bias
70 µm
DoubleCOL Bias
Analog Chip Bottom (ACB)
DoubleCOL Bias
Digital Chip Bottom (DCB)
ADC
Calibr.
Bias DACs
CDR/PLL
Sensors
Ring osc.
ShLDO_An
ShLDO_Dig
ShLDO_An
ShLDO_Dig
Driver/Rec
POR
ShLDO_An
ShLDO_Dig
ShLDO_An
ShLDO_Dig
Padframe

New Feature Highlight

- Encoding with lossless compression used to send data off chip.
  - Custom serial stream encoding to achieve compression AND be tolerant of corrupted fragments
- Important because, thanks to serial power, services volume (and mass) is dominated by data cables.

CMS Example



(note compressed data is independent of pixel shape)

RD53B Status

- All design work getting finishing touches this month
  - Very significant amount of design work done- not just cut and paste from RD53A
  - Almost every circuit has been touched at some level and several new functions (not in RD53A) have been added
- Verification is critical. Advanced, but not yet completed
- Must reach a high level of confidence through verification in order to submit
  - 143K lines of System Verilog code to verify 26.5K lines of chip code
  - RD53 internal workshop in progress at CERN to check design and pour over all simulation and verification results
- ATLAS Final Design Review of ITkPix-V1 is on Friday
  - Also must be completed before order for wafer run can be placed. https://indico.cern.ch/event/835605/

Verification / Simulation examples

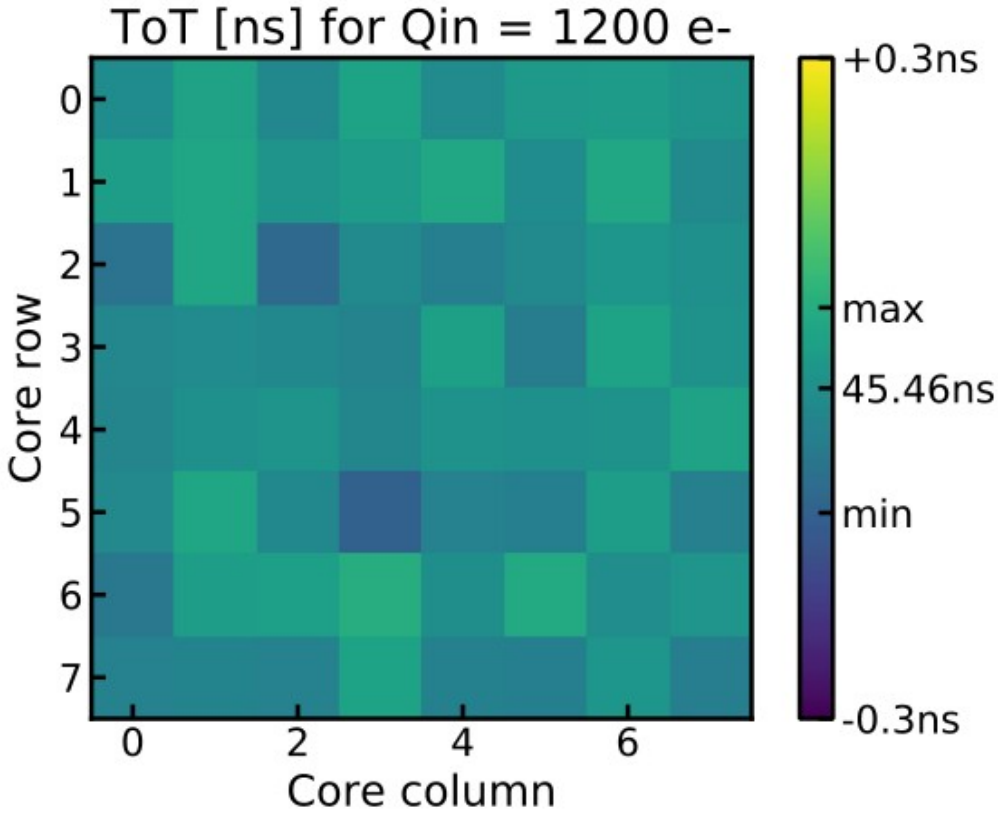
RD53B Full chip digital

Tests Hierarchy

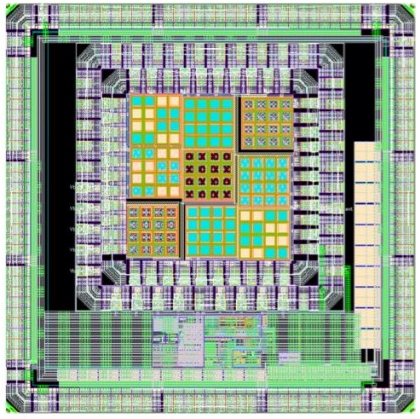
Name	Overall Average Grade	Overall Covered	Test Status
Test-Case Model	96.79%	46 / 48 (95.83%)	95.83%
default	96.79%	46 / 48 (95.83%)	95.83%
VerificationPlanTests	96.79%	46 / 48 (95.83%)	95.83%
SmokeTests	100%	3 / 3 (100%)	100%
top_test_random_hits_and_trigs_4lanes_nodeadtime	100%	1 / 1 (100%)	100%
top_test_read_default_gc	100%	1 / 1 (100%)	100%
top_test_pix_conf_readback_autorow_1corecol	100%	1 / 1 (100%)	100%
PixelArrayDatapath	90%	11 / 12 (91.67%)	91.67%
top_test_random_hits_230mhz_and_trigs_4mhz_1lane	100%	1 / 1 (100%)	100%
top_test_random_hits_230mhz_and_trigs_4mhz_2lanes	100%	1 / 1 (100%)	100%
top_test_random_hits_1d5ghz_and_trigs_1mhz_2lanes	100%	1 / 1 (100%)	100%
top_test_random_hits_2d7ghz_and_trigs_1mhz_3lanes	100%	1 / 1 (100%)	100%
top_test_random_hits_3d5ghz_and_trigs_1mhz_4lanes	100%	1 / 1 (100%)	100%
top_test_random_hits_3d5ghz_and_twolevel_trigs_4mhz_800khz_4lanes	0%	only rejected triggers	
top_test_random_hits_3d5ghz_and_trigs_1mhz_tot80mhz_4lanes	100%	1 / 1 (100%)	100%
top_test_random_hits_3d5ghz_and_trigs_1mhz_tot80mhz_6to4map_4lanes	100%	1 / 1 (100%)	100%
top_test_random_short_hits_2d5ghz_and_trigs_1mhz_4lanes	100%	1 / 1 (100%)	100%
ExtremeTests	100%	3 / 3 (100%)	100%
top_test_extreme_hits_monsters_phi_4lanes	100%	1 / 1 (100%)	100%
top_test_extreme_hits_monsters_z_4lanes	100%	1 / 1 (100%)	100%
top_test_black_event_hit_and_trig	100%	1 / 1 (100%)	100%
ChannelSyncDecodeCmds	87.5%	7 / 8 (87.5%)	87.5%
top_test_channelSynch	0%	SVA (already fixed in branch)	
top_test_cmd_reco_bit_flip	100%	1 / 1 (100%)	100%
top_test_cmd_bit_flip_warn_count	100%	1 / 1 (100%)	100%
top_test_cmd_corrupt_symbol	100%	1 / 1 (100%)	100%
top_test_cmd_bit_flip_error_count	100%	1 / 1 (100%)	100%
top_test_cmd_error_count	100%	1 / 1 (100%)	100%
top_test_cmd_error	100%	1 / 1 (100%)	100%
top_test_debug_commands	100%	1 / 1 (100%)	100%
ConfigurationServiceData	100%	4 / 4 (100%)	100%
top_test_read_default_gc	100%	1 / 1 (100%)	100%
top_test_pix_conf_readback_autorow_1corecol	100%	1 / 1 (100%)	100%
top_test_global_conf_allones	100%	1 / 1 (100%)	100%
top_test_global_conf_allzeros	100%	1 / 1 (100%)	100%
CalibrationInjection	100%	12 / 12 (100%)	100%
top_test_injection_trig	100%	1 / 1 (100%)	100%
top_test_injection_hitor	100%	10 / 10 (100%)	100%
top_test_analog_injection_trig	100%	1 / 1 (100%)	100%
AdditionalTests	100%	1 / 1 (100%)	100%
top_test_custom_cmd_aurora_readback	100%	1 / 1 (100%)	100%
MonteCarlo	100%	8 / 8 (100%)	100%
PixelArray_MC_AtlasBarrel0CenterFlat	100%	1 / 1 (100%)	100%
PixelArray_MC_AtlasBarrel0EndFlat	100%	1 / 1 (100%)	100%
PixelArray_MC_AtlasBarrel0InitInclied	100%	1 / 1 (100%)	100%
PixelArray_MC_AtlasBarrel2CenterFlat	100%	1 / 1 (100%)	100%
PixelArray_MC_AtlasBarrel2EndFlat	100%	1 / 1 (100%)	100%
PixelArray_MC_AtlasBarrel2InitInclined	100%	1 / 1 (100%)	100%
PixelArray_MC_AtlasDisks0	100%	1 / 1 (100%)	100%
PixelArray_MC_AtlasDisks2	100%	1 / 1 (100%)	100%

Showing 50 items

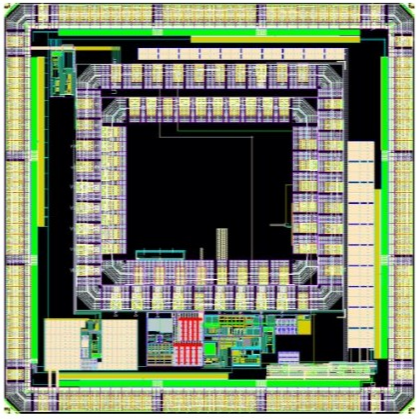
RD53B Full core Analog (with parasitics)



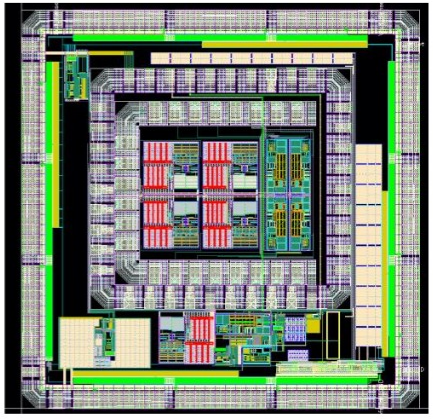
Circuits Validated in Silicon



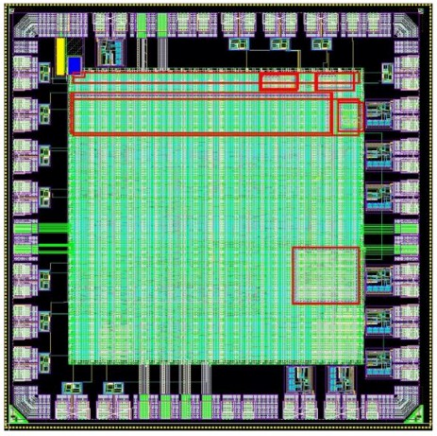
SLDO Testchip_A
Submitted on August 2018



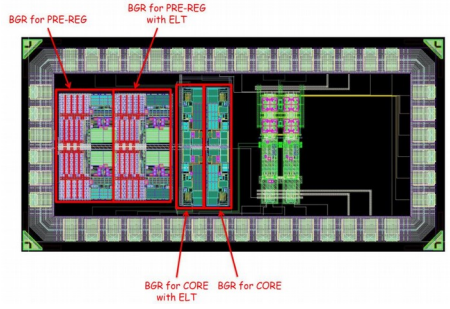
SLDO Testchip_B
Submitted November 2018



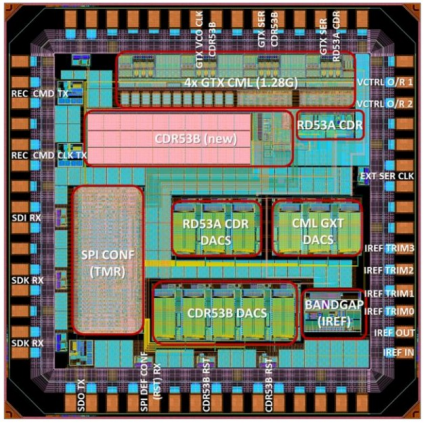
SLDO Testchip_C
Submitted February 2019



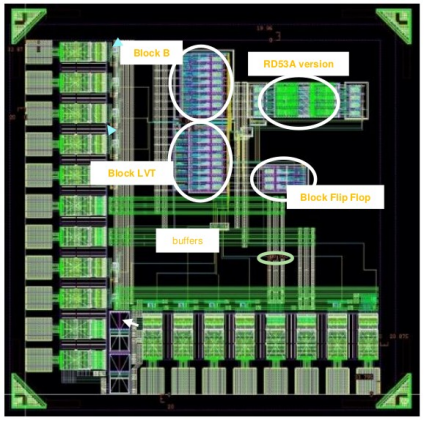
SEU Test Chip
Submitted Aug. 2018



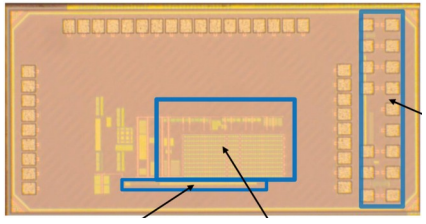
Bandgap Test Chip
Submitted Aug. 2018



CDR/PLL Test Chip
Submitted Aug. 2018



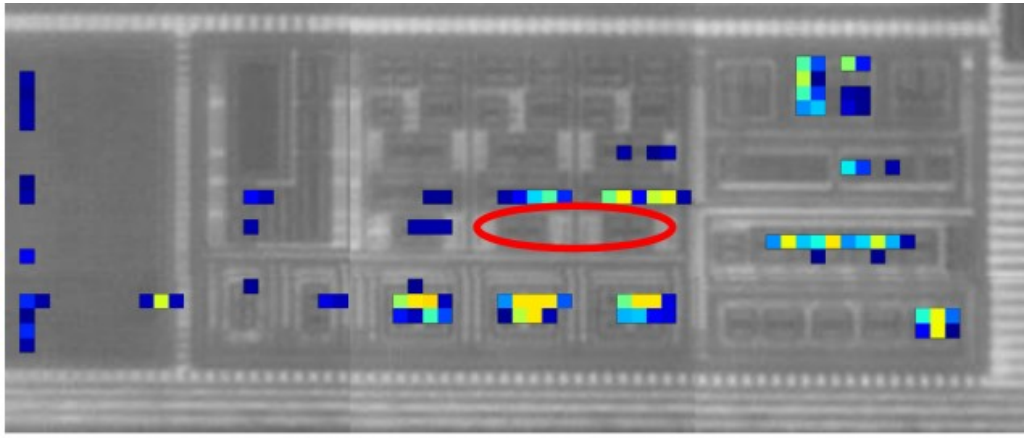
Ring Oscillator Test Chip
Submitted Nov. 2018



ADC Chip
Submitted Aug. 2018

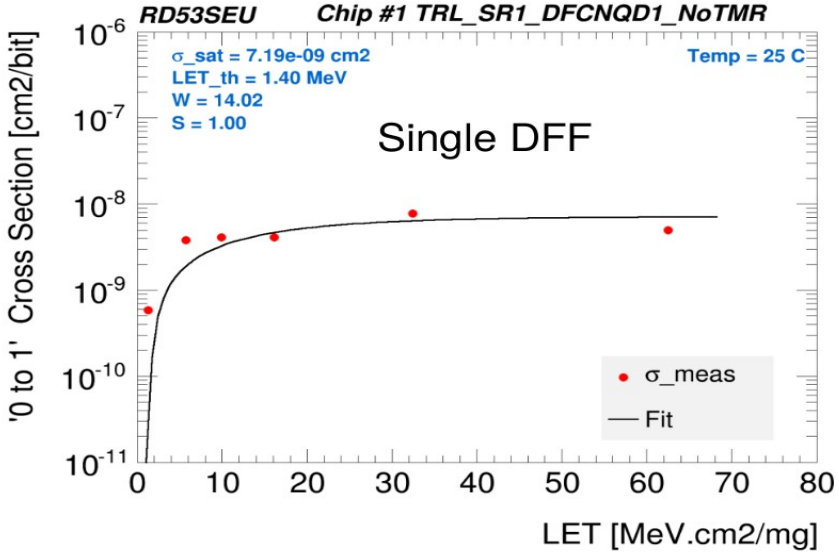
Single Event Effect Testing

Laser Injection on test chips

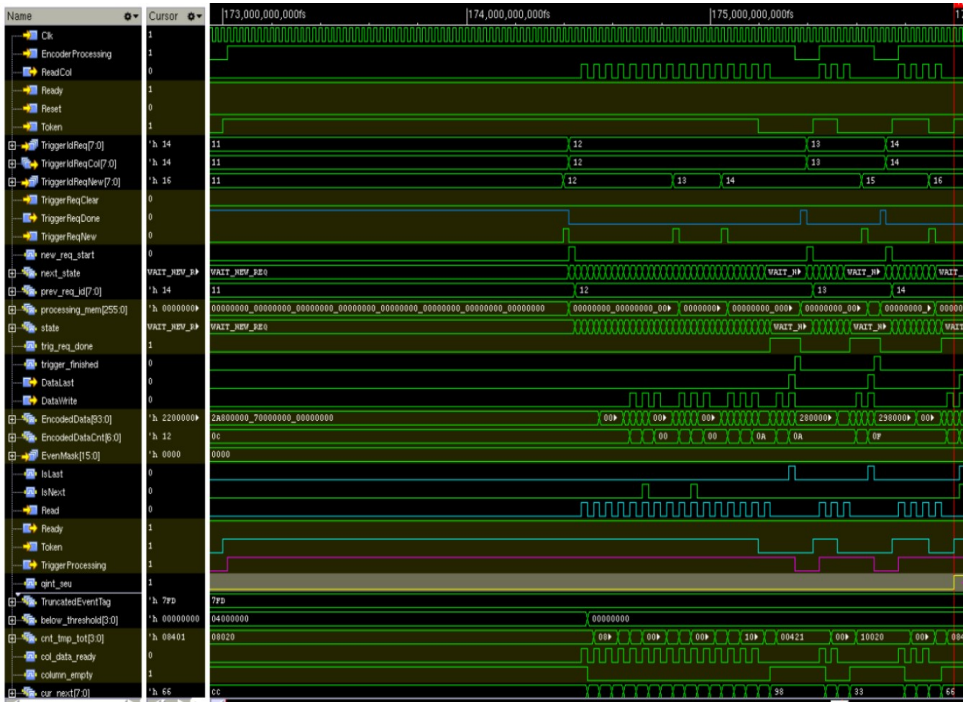


Whole VCO scanned in one run, focus closer to M1

Ions on test chips



Charge injection
in simulation



Conclusions

- RD53 collaboration mandate has been extended to design the production pixel readout chips for ATLAS and CMS
- Configurable design called RD53B
  - Will be instantiated first for ATLAS (submission this fall)
  - ATLAS Final Design Review this Friday
  - CMS chip submission will follow in 2020
- RD53B contains new features needed for production
- Extensive simulation and verification program significantly expanded relative to what was done for RD53A
- More info at cern.ch/RD53

B A C K U P

Design Team

Collaboration board chair:
Lino Demaria, Torino

Interface to experiments: Co-spokespersons
Jorgen Christiansen, CERN (CMS) , **Maurice Garcia-Sciveres, LBNL (**ATLAS)
- General organization, Funding, Specifications,

Experiment observers
Duccio Abbaneo, CERN (CMS) ,
Kevin Einsweiler, LBNL (ATLAS)

RD53 design framework for final pixel chips: Flavio Loddo, Bari; Deputy: Tomasz Hemperek, Bonn

Floorplan/integration:
Flavio Loddo, Bari
- Pixel array, Bump pad, EOC, Power distribution, Bias distribution, Analog/digital isolation, Integration, Verification

Analog FEs with biasing:
Luigi Gaioni, Bergamo;
Ennio Monteil, Torino;
Amanda Krieger, LBNL
- Specification/performance, Interface, Analog isolation, simulation model, Abstract, Integration, Verification

Monitoring:
Mohsine Menouni, CPPM;
Gianluca Traversi, Bergamo,
IP designers
- Specification/performance, Interface, Analog isolation, simulation model, Abstract, Integration, Verification

PAD frame: Hans Krueger, Bonn
CDR/PLL: Piotr Rymaszewski, Bonn
High speed drv: Konstantinos Moustakas, Tianyang Wang, Bonn
Diff. IO: Gianluca Traversi, Bergamo

Digital integration:
Tomasz Hemperek, Bonn; Luca Pacher, Torino
- **Simulation Framework:**
  Sara Marconi, CERN;
  - Framework, Hit generation/ import MC, Reference model / score board, Monitoring/verification tools, Readout rate estimations, Behavioural pixel chip, SEU injection.
- **Pixel array logic:**
  Sara Marconi, CERN
  - FE interface, Latency buffer, Core/column bus
- **Digital chip bottom:**
  Roberto Beccherle, Pisa; Francesco Crescioli, LPNHE;
  - Configuration, Control interface, Readout data format/protocol, Compression
- **Verification:**
  Sara Marconi, CERN; Attiq Rehman, Bergen,
  Joel De Witt, Santa Cruz
  Cesar Gonzales Renteria, LBNL
  Peilian Liu, LBNL
  SEU: Pedro Leitao, CERN; Rafael Girona, Sevilla
  SET: Fernando Munoz Chavero, Sevilla
  LPGBT: Pedro Leitao, CERN
  Mixed signal: Luca Pacher, Torino;
  Aikaterini Papadopoulou, LBNL
  - Functional, SEU, Interfaces, specifications
- **Library cells:**
  DICE: Denis Fougeron, Mohsine Menouni, CPPM
  Timing characterization : Sandeep Miryala, FNL

Serial Power:
SLDO: Michael Karagounis,
Andreas Stiller, Dortmund.
Bandgap: Gianluca Traversi,

Verification: Alvaro Pradas, ITAINNOVA;
Stella Orfanelli, CERN; Dominik Koukola, CERN
- Shunt-LDO integration, On-chip power distribution, Optimization for serial powering, System level power aspects, Power Verification

Design for testability:
Giuseppe De Robertis, Bari
- Scan path, BIST, production test patterns, Fault simulation, bump bonding testing

IPs: Support and possible updates
Current DAC: Bari
Voltage DAC: Prague
ADC, mux, temp: CPMM
Power on reset: Seville
Ring oscillator: LAL
Analog buffer: RAL

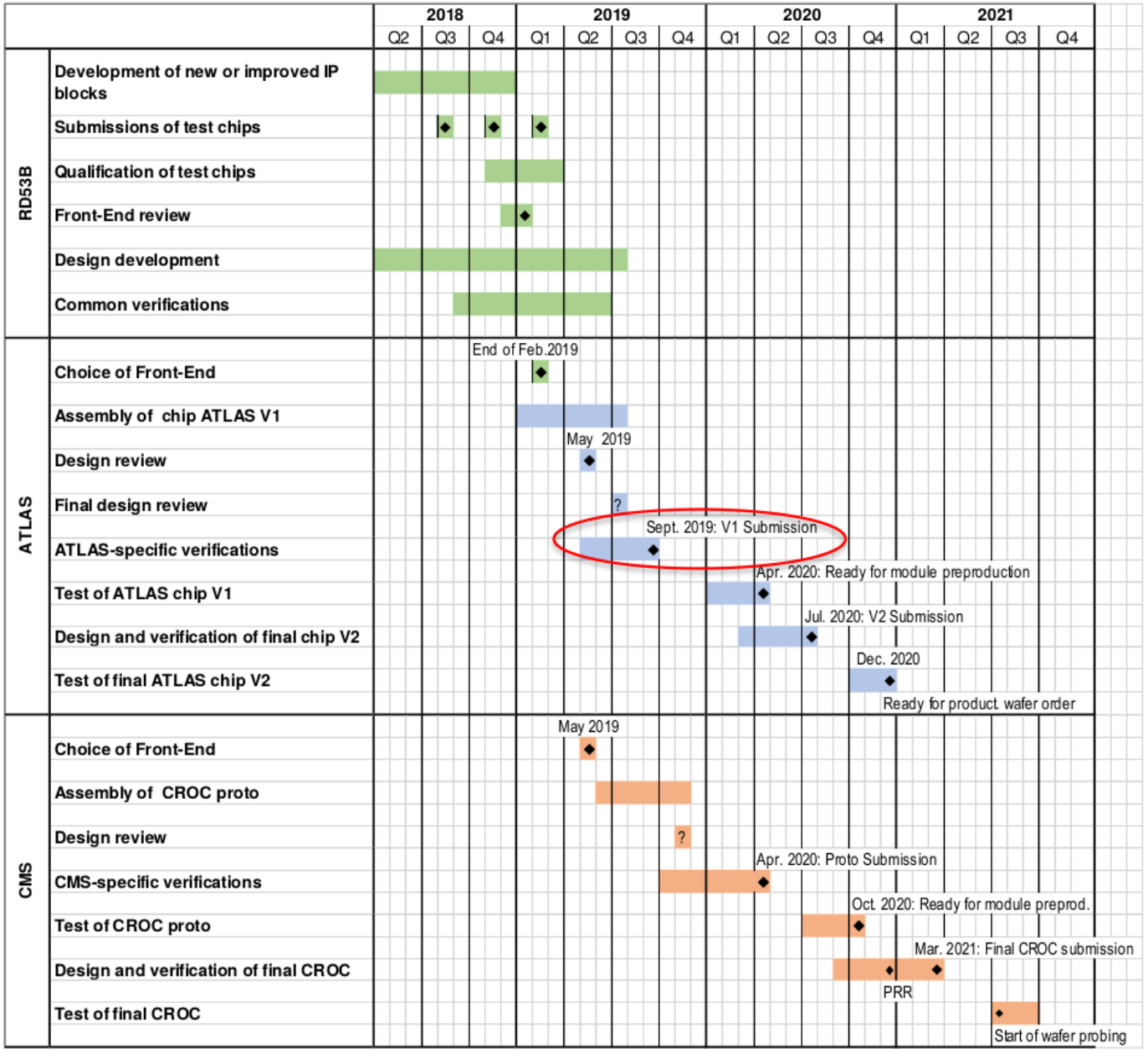
Support and services:
Tools, design kit: Wojciech Bialas, CERN
Repositories: Flavio Loddo, Bari; Luca Pacher, Torino; Tomasz Hemperek, Bonn
Radiation model: Mohsine Menouni, CPPM; CERN

Testing: Timon Heim, LBNL
YARR system: Timon Heim, LBNL
BDAQ53 system: Marco Vogt, Michael Daas, Yannik Dieter, Hans Krueger, Tomasz Hemperek, Mark Standtke Bonn
Radiation test: Luis Miguel Jara Casas, CERN, Mohsine Menouni, CPPM.
Plus many ATLAS/CMS groups not formally part of RD53

Pixel sensor and bump-bonding:
Fabian Huegging, Bonn (ATLAS),
Georg Steinbrueck, Hamburg (CMS)

Names in bold: Member of RD53 management board

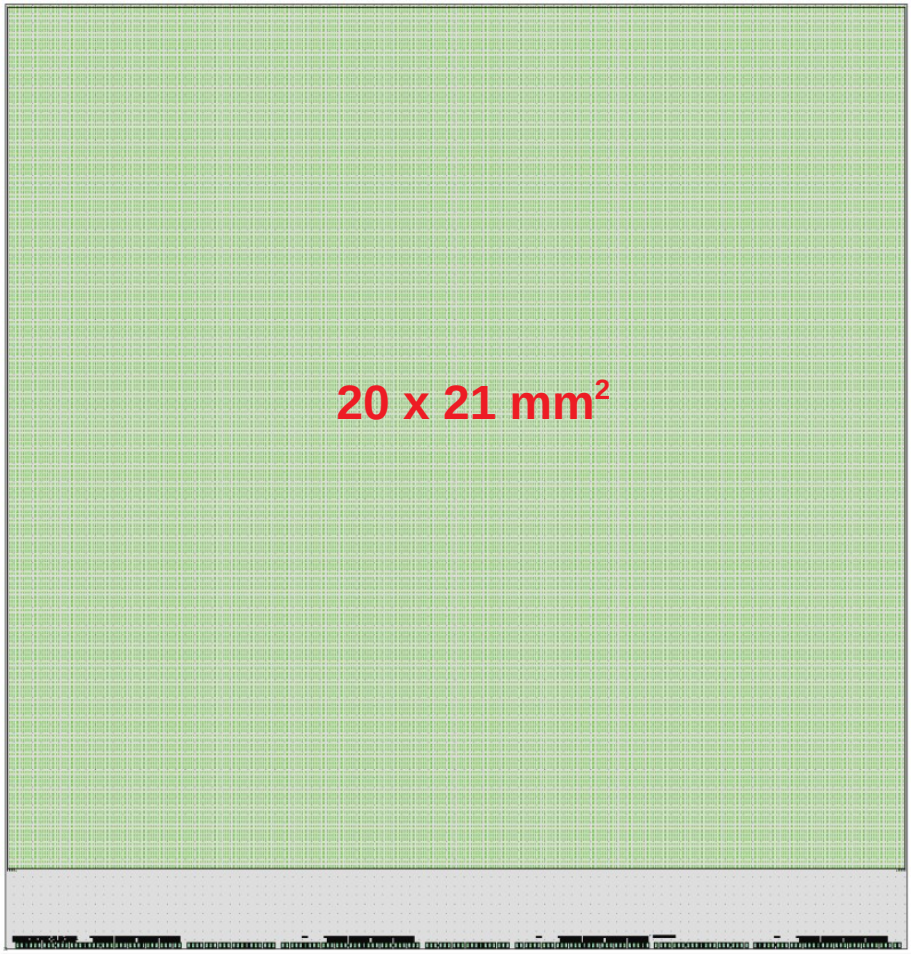
Schedule

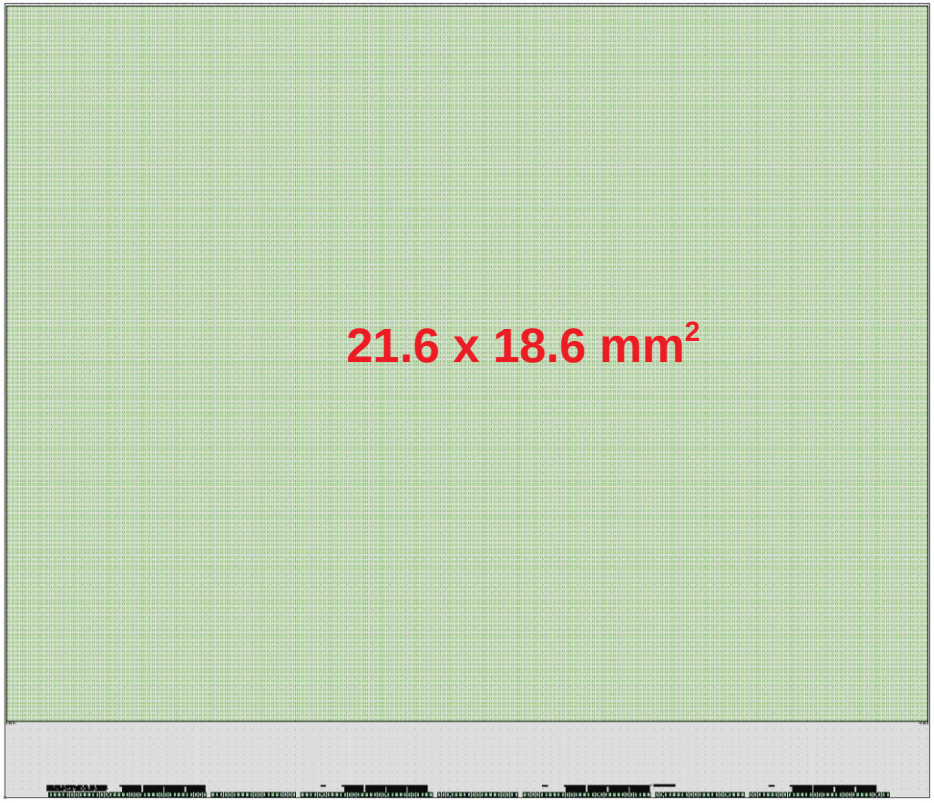

2018
2019
2020
2021
Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4
RD53B
Development of new or improved IP blocks
Submissions of test chips
Qualification of test chips
Front-End review
Design development
Common verifications
ATLAS
End of Feb.2019
Choice of Front-End
Assembly of chip ATLAS V1
May 2019
Design review
Final design review
?
Sept. 2019: V1 Submission
ATLAS-specific verifications
Apr. 2020: Ready for module preproduction
Test of ATLAS chip V1
Jul. 2020: V2 Submission
Design and verification of final chip V2
Dec. 2020
Test of final ATLAS chip V2
Ready for product. wafer order
CMS
May 2019
Choice of Front-End
Assembly of CROC proto
Design review
?
Apr. 2020: Proto Submission
CMS-specific verifications
Oct. 2020: Ready for module preprod.
Test of CROC proto
Mar. 2021: Final CROC submission
Design and verification of final CROC
PRR
Test of final CROC
Start of wafer probing

RD53B New Features

- Selected Diff. Front End for ATLAS, Lin. FE for CMS
- Added edge, top, and corner pixel biases
- Upgraded calibration injection & corrected column variation
- New hit synchronization and ToT with 6b-to-4b compression
- Redesign of the startup and generation of reference voltages
- Improvement of SLDO and addition of low power mode
- Addition of overcurrent and overvoltage protection
- Redesigned PLL for lower jitter and robust locking
- Added trigger tags and new readout format with compression
- Added 2-lever trigger for ATLAS and self-trigger
- Added suppression of low charge isolated hit backgrounds
- Added data aggregation between chips
- Changed reset scheme to synchronous and added CMD activity reset
- Extensive triplication and SEU hardening
- Added new resistive temperature sensors and E-fuses for SN
- Added precision ToT and ToA
- Enlarged wire bond pads

RD53B-ATLAS & CMS side-by-side





RD53A Database

- Database of RD53A chips in use at cern.ch/rd53a-chips

Current Wafer: 3

			05-01 MISSING	06-01 MISSING					
		04-02 CERN	05-02 CERN	06-02 DEMOKRITOS	07-02 CERN	08-02 CERN			
	02-03 CERN	03-03 RBI	04-03 CERN	05-03 CERN	06-03 LBNL	07-03 LBNL	08-03 CERN	09-03 CERN	
	02-04 CERN	03-04 CERN	04-04 CERN	05-04 CERN	06-04 LBNL	07-04 ETH	08-04 CERN	09-04 COLORADO	
	02-05 CERN	03-05 CERN	04-05 CERN	05-05 CERN	06-05 CERN	07-05 ETH	08-05 UNM	09-05 COLORADO	10-05 ETH
01-06 CERN	02-06 CERN	03-06 CERN	04-06 CERN	05-06 CERN	06-06 CERN	07-06 ETH	08-06 ETH	09-06 COLORADO	10-06 ETH
01-07 CERN	02-07 ETH	03-07 CERN	04-07 CERN	05-07 CERN	06-07 CERN	07-07 ETH	08-07 CERN	09-07 COLORADO	10-07 ETH
01-08 CERN	02-08 CERN	03-08 CERN	04-08 FIRENZE	05-08 DEMOKRITOS	06-08 CERN	07-08 ETH	08-08 CERN	09-08 PURDUE	10-08 ETH
	02-09 CERN	03-09 CERN	04-09 CERN	05-09 CERN	06-09 CERN	07-09 CERN	08-09 CERN	09-09 PURDUE	10-09 CERN
	02-10 CERN	03-10 CERN	04-10 CERN	05-10 DEMOKRITOS	06-10 ETH	07-10 CERN	08-10 CERN	09-10 ETH	
		03-11 RBI	04-11 CERN	05-11 CERN	06-11 CERN	07-11 CERN	08-11 CERN		
			04-12 CERN	05-12 CERN	06-12 CERN	07-12 CERN			

Serial Number	0x0385
Diced Location	IZM
Diced Date	2018-08-01 12:00:00
Thickness	350 nm
Bumped	False
Sensor	NONE
Flip Date	2019-04-30 12:00:00
Board	365
Board Date	2018-11-14 12:00:00
Status History	2019-04-30 - All Good 2018-11-14 - Untested
Location History	2019-04-30 - UNM 2018-11-14 - FIRENZE 2018-08-27 - CERN
Radiation (Mrad)	None
Chip Comment	
Board Comment	In SCC card
Board Type	1: Bonn SCC

RD53A Wafer Probing

- Wafer Probing

- Probed 58 wafers in total
  - 41 in Bonn (for RD53 and ATLAS)
  - 17 at CERN (for CMS)
- 89 chips per wafer: Over 5000 chips for statistical analysis
- Designated in parts for RD53, ATLAS and CMS

- Test procedure very stable
- Results look as expected