



RD53A Digital Quads

Weekly Instrumentation Meeting

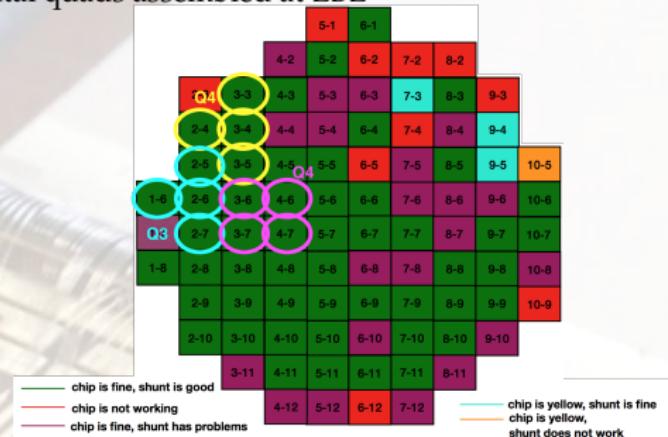
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RD53A Digital Quads

Assembly

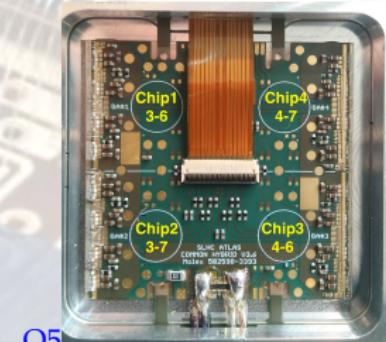
- Notes from the debugging: GDoc
 - Three working digital quads assembled at LBL



Q3



Q4



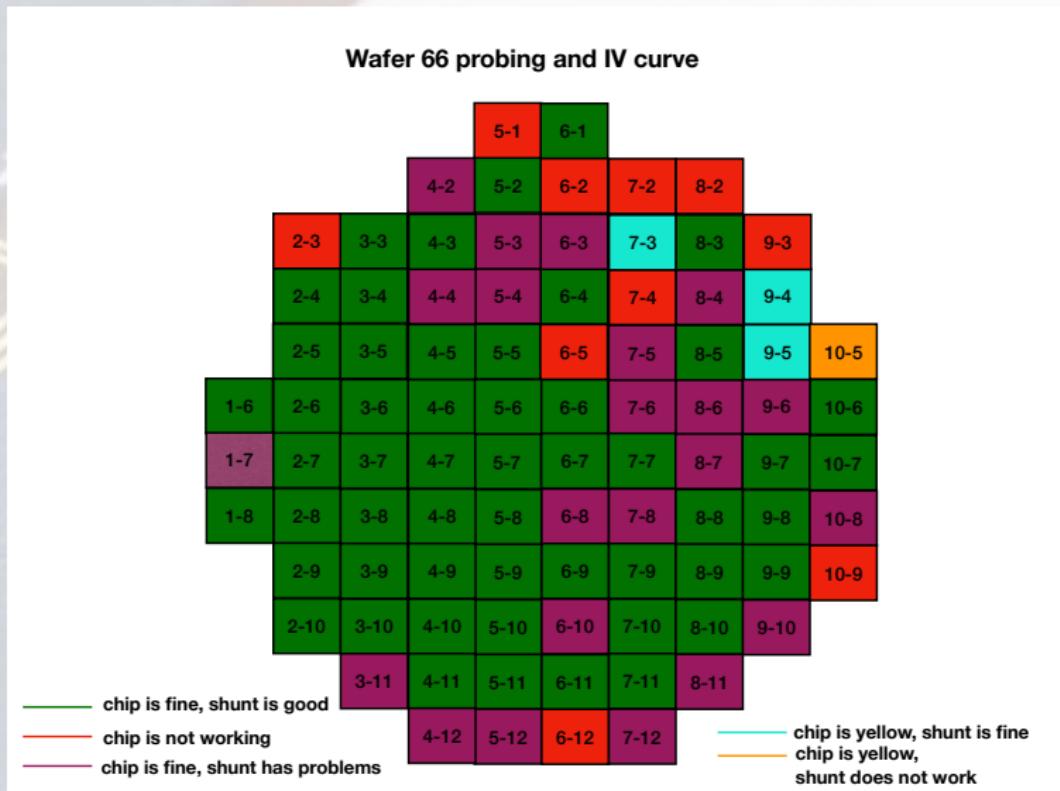
Q5

- Wafer probing results: wafer66
- RD53A database wafer66

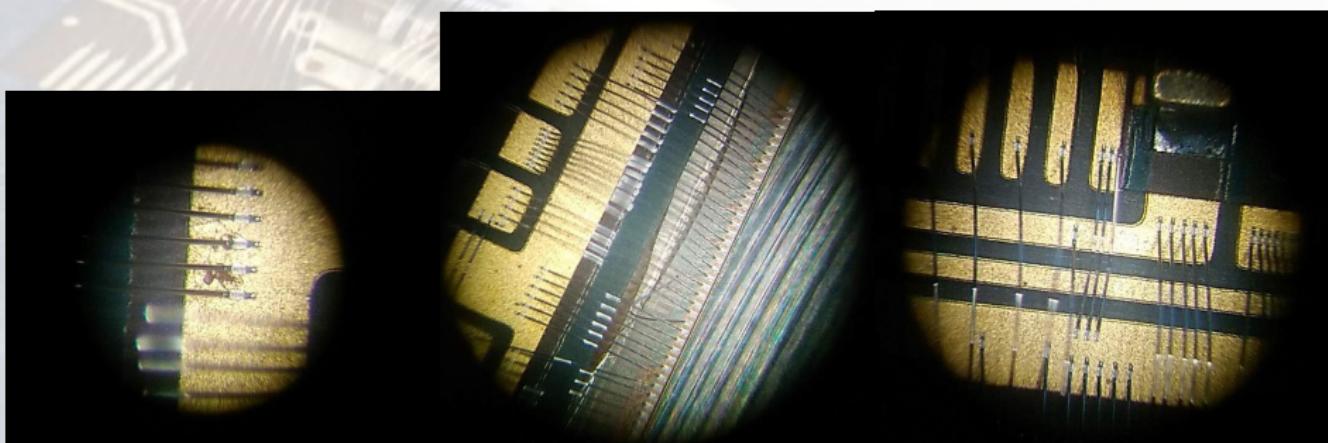
Current Wafer: 66

		05-01 LBNL		06-01 LBNL							
		04-02 LBNL	05-02 LBNL	06-02 LBNL	07-02 LBNL	08-02 LBNL					
02-03 LBNL		03-03 LBNL	04-03 LBNL	05-03 LBNL	06-03 LBNL	07-03 LBNL	08-03 LBNL	09-03 LBNL			
02-04 LBNL		03-04 LBNL	04-04 LBNL	05-04 LBNL	06-04 LBNL	07-04 LBNL	08-04 LBNL	09-04 LBNL			
02-05 LBNL		03-05 LBNL	04-05 LBNL	05-05 LBNL	06-05 LBNL	07-05 LBNL	08-05 LBNL	09-05 LBNL	10-05 LBNL		
01-06 LBNL	02-06 LBNL	03-06 LBNL	04-06 LBNL	05-06 LBNL	06-06 LBNL	07-06 LBNL	08-06 LBNL	09-06 LBNL	10-06 LBNL		
01-07 LBNL	02-07 LBNL	03-07 LBNL	04-07 LBNL	05-07 LBNL	06-07 LBNL	07-07 LBNL	08-07 LBNL	09-07 LBNL	10-07 LBNL		
01-08 LBNL	02-08 LBNL	03-08 LBNL	04-08 LBNL	05-08 LBNL	06-08 LBNL	07-08 LBNL	08-08 LBNL	09-08 LBNL	10-08 LBNL		
	02-09 LBNL	03-09 LBNL	04-09 LBNL	05-09 LBNL	06-09 LBNL	07-09 LBNL	08-09 LBNL	09-09 LBNL	10-09 LBNL		
	02-10 LBNL	03-10 LBNL	04-10 LBNL	05-10 LBNL	06-10 LBNL	07-10 LBNL	08-10 LBNL	09-10 LBNL			
		03-11 LBNL	04-11 LBNL	05-11 LBNL	06-11 LBNL	07-11 LBNL	08-11 LBNL				
			04-12 LBNL	05-12 LBNL	06-12 LBNL	07-12 LBNL					

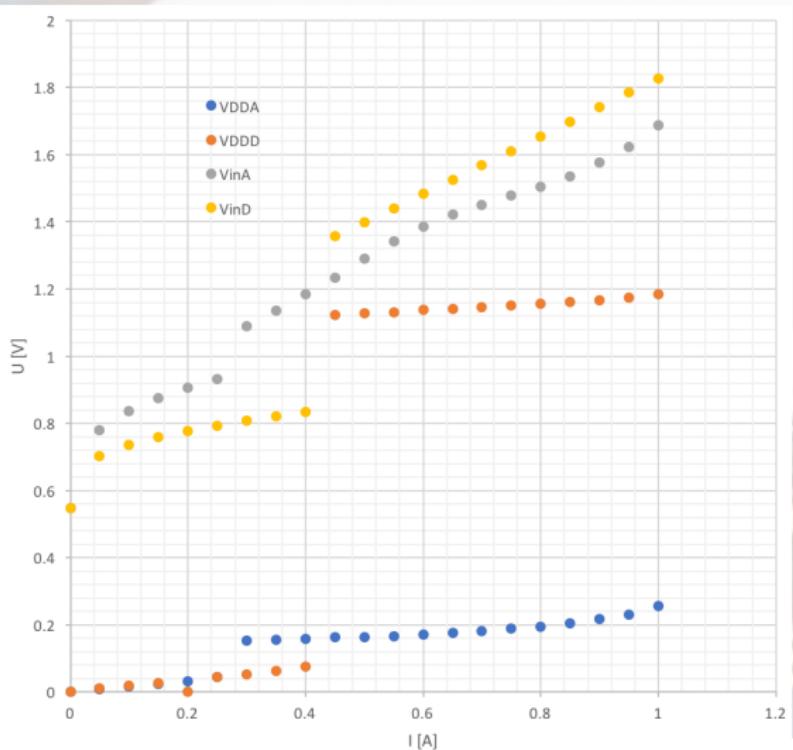
- Elodie made maps for wafers 66 and 69 looking additionally to the VI curves
<https://cernbox.cern.ch/index.php/s/MW3yXsmqehwxaoH>



- Q5: Chip1 3-6, Chip2 3-7, Chip3 4-6, Chip4 4-7
- WaferProbing Vdda@16: 3-6: 1.046677 V, 3-7: 1.167013 V, 4-6: 1.045003 V, 4-7: 1.078216 V
- VI: One wirebond for Vdda for Chip 4 is not connected (first regulator) but there are 4 more which are bonded
- VI: Chip 2 has one wirebond not connected for GND module



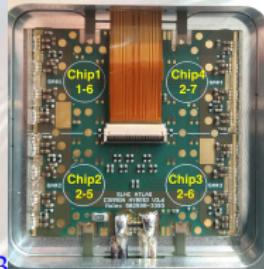
- Q5: Chip1 3-6, Chip2 3-7, Chip3 4-6, Chip4 4-7
- WaferProbing Vdda@16: 3-6: 1.046677 V, 3-7: 1.167013 V, 4-6: 1.045003 V, 4-7: 1.078216 V
- V-I curve for Chip3: 4-6 (Vdda < 0.3 V for the full range)



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Summary

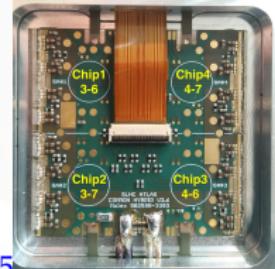
- Notes from the debugging: GDoc
- Three working digital quads assembled at LBL
 - **Q3** wafer 66, Chip1 1-6, Chip2 2-5, Chip3 2-6, Chip4 2-7
 - **Q4** wafer 66, Chip1 2-4, Chip2 3-3, Chip3 3-4, Chip4 3-5
 - **Q5** wafer 66, Chip1 3-6, Chip2 3-7, Chip3 4-6, Chip4 4-7



Q3



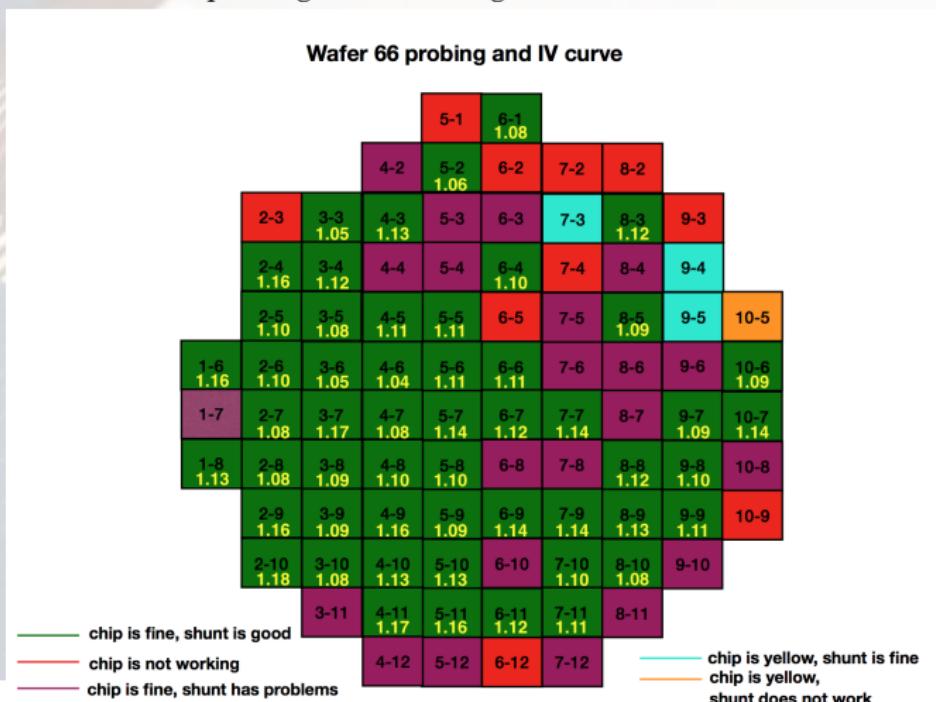
Q4



Q5

	Vdda (Chip1) [V]	Vdda (Chip2) [V]	Vdda (Chip3) [V]	Vdda (Chip4) [V]
Q3 (WaferProbing)	1.165464	1.096592	1.099969	1.080992
Q3 (Measured@4.4A)	1.17	1.09	1.09	1.08
Q3 (pull-up)	-	300k	300k	150k
Q3 (final)	1.17	1.14	1.14	1.18
Q4 (WaferProbing)	1.163635	1.0557	1.122478	1.077563
Q4 (Measured@4.4A)	1.17	1.06	1.12	1.08
Q4 (pull-up)	-	150k	300k	150k
Q4 (final)	1.17	1.15	1.18	1.18
Q5 (WaferProbing)	1.046677	1.167013	1.045003	1.078216
Q5 (Measured@4.4A)	1.04	1.16	1.05	1.07
Q5 (pull-up)	150k	-	150k	300k
Q5 (final)	1.14	1.17	1.14	1.17

- General rule for pull-up resistor application: (53 chips on wafer 66)
 - if $V_{DDA} < 1.08 \text{ V}$ add 150k pull-up (11 chips => 21 %)
 - if $1.08 \text{ V} < V_{DDA} < 1.14 \text{ V}$ add 300k pull-up (35 chips => 66 %)
 - no pull-up (7 chips => 13 %)
- V_{DDA} values from wafer probing at trim setting 16:



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Wafer Probing Data

- Need to reanalyze VI curves

