University of Barcelona
Department of Electronics

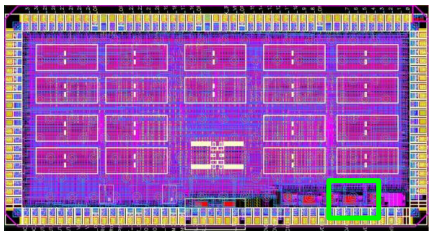
GAPDs in standard CMOS technologies for tracker detectors

Technical talk at Berkeley Lab

Eva Vilella Figueras

January 28, 2014

Involvement in prototype chips.



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- With enclosed layout transistors
- Belongs to DHP 0.1, a readout chip for the DEPFET technology
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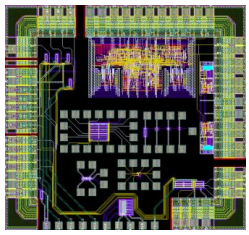
- 1 conference paper



- APDs chip (Run 2), HV-AMS 0.35 µm, April 2010
- Several GAPD pixels with different readout circuits + small GAPD arrays
- First GAPD pixels with digital output at the Univ. Barcelona
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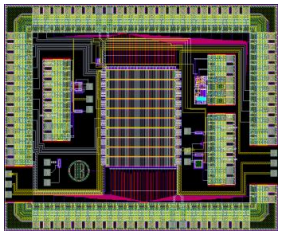

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- Characterization in beam-tests at CERN
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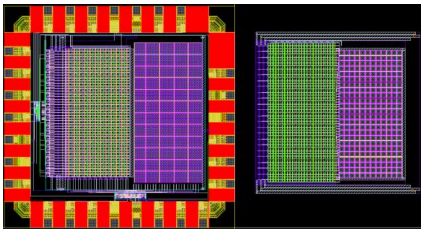

- 3D APDs chip, Global Foundries 130 nm/Tezzaron 3D, not submitted
- Large GAPD array
- Explore a 3D technology (improve GAPD fill-factor)
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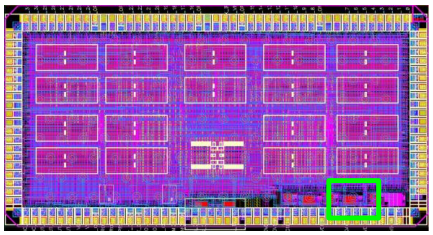

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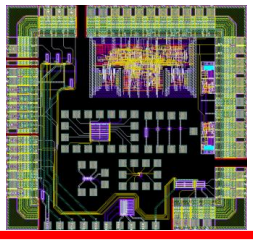

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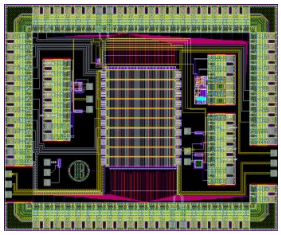

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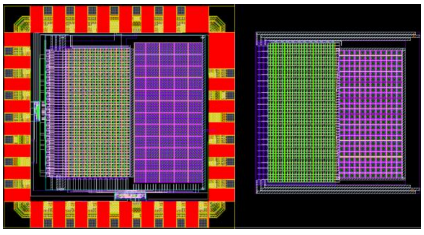

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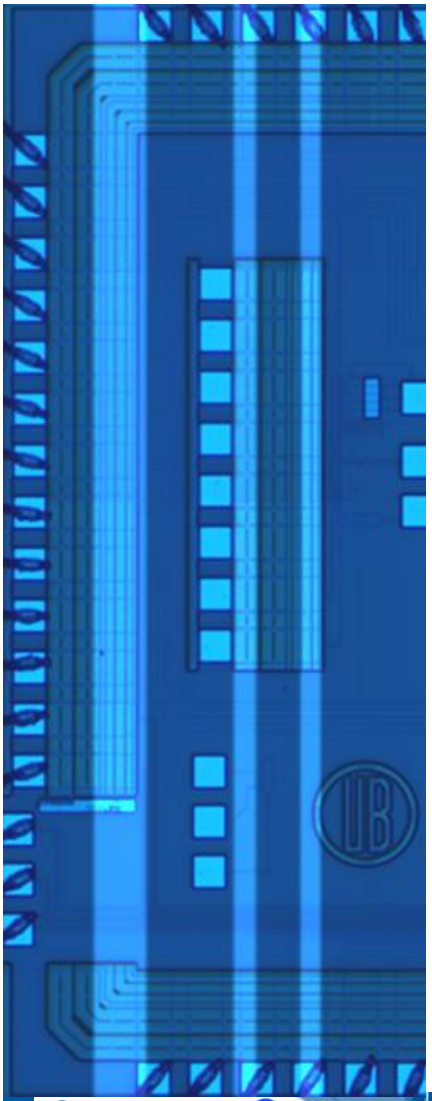
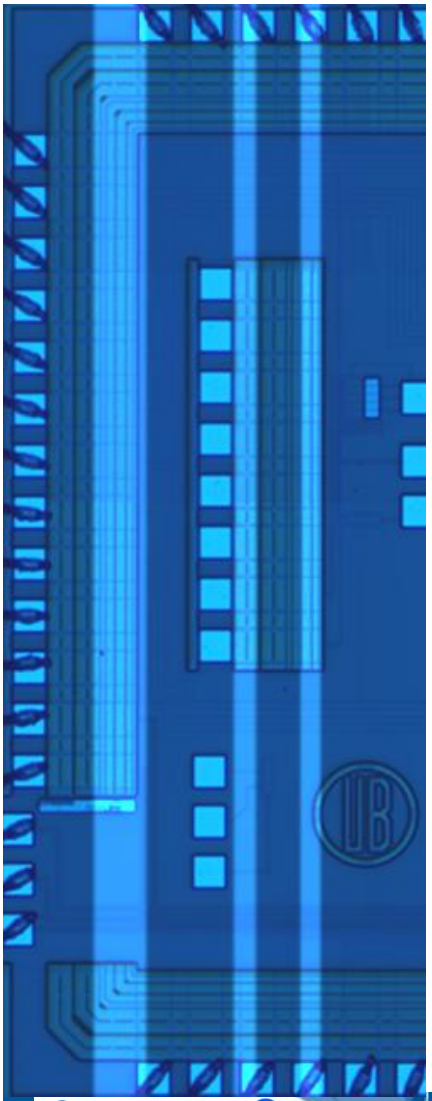


➢Outline

1. **Potential applications**
   - Future linear lepton colliders
   - Detector systems in ILC/CLIC
2. **GAPDs in CMOS technologies**
   - Principle of operation and figures of merit
   - State-of-the-art
   - Front-end electronics
3. **Large arrays in a HV-CMOS process**
   - Design and characterization
4. **Large arrays in a 3D process**
   - Design

Conclusion



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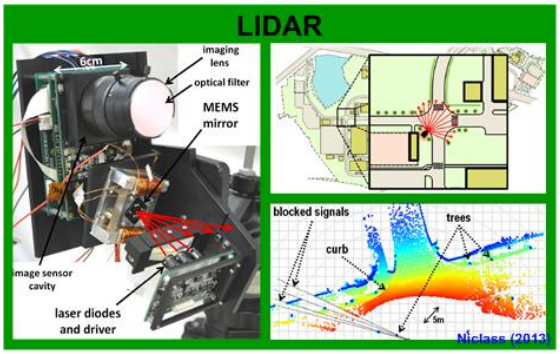
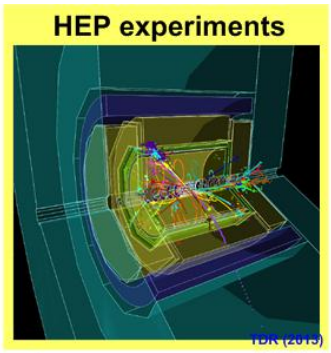
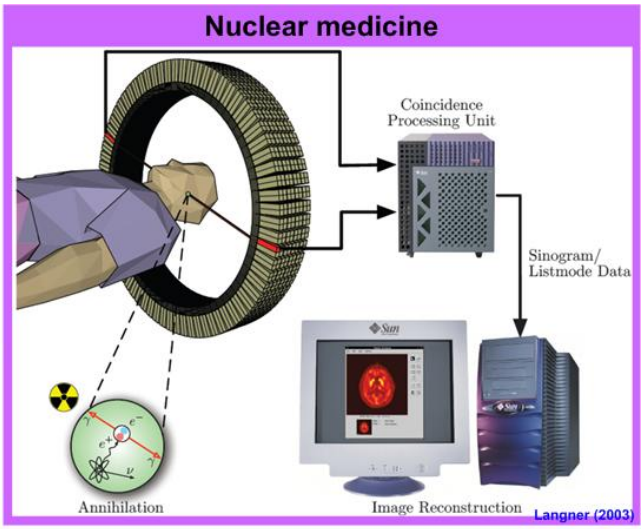
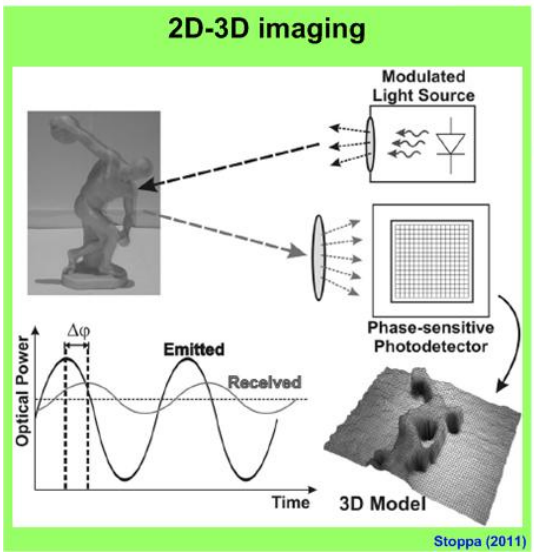
Potential applications.

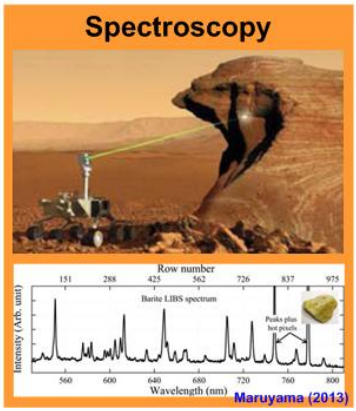


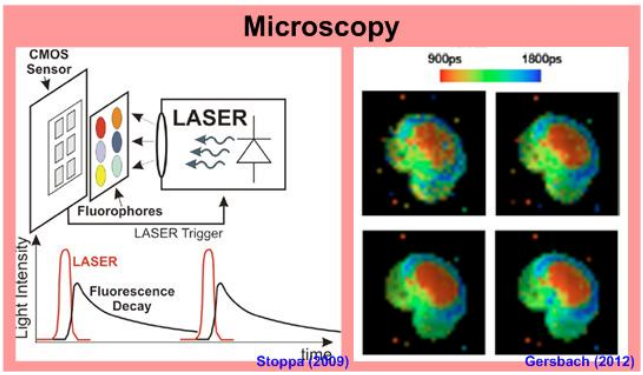






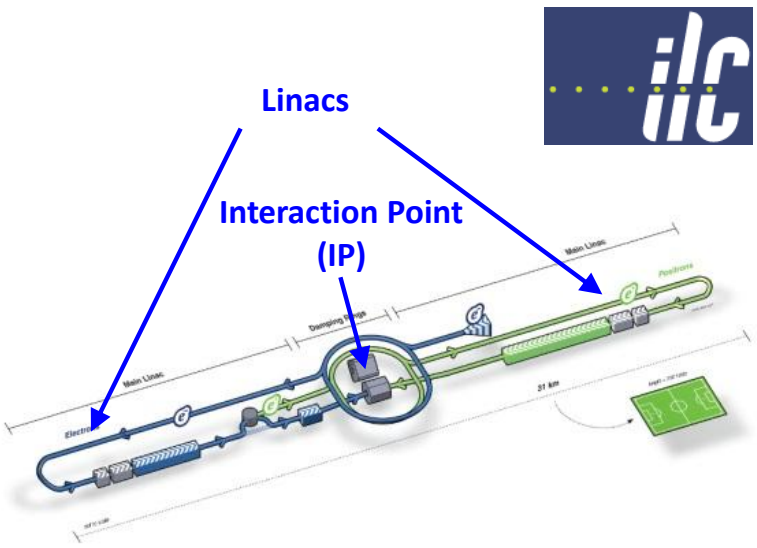
Single-photon sensing

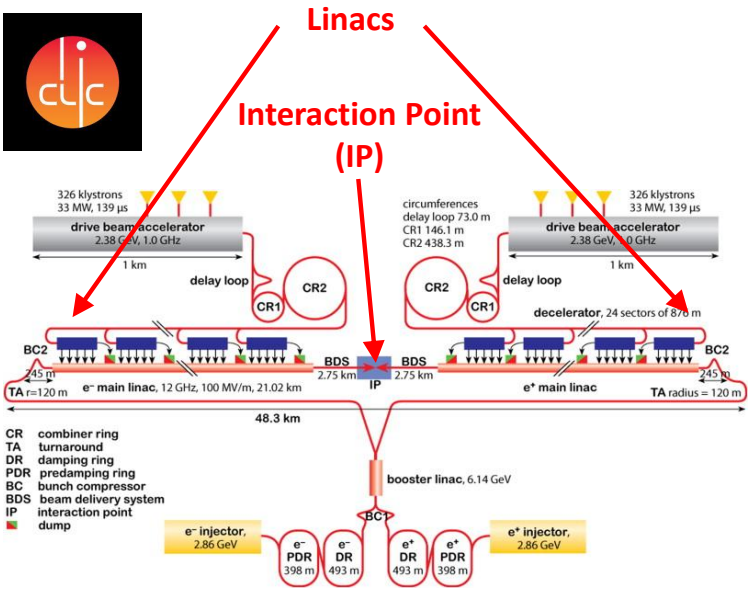




HEP experiments. Future linear lepton colliders.

- Target → Study in great detail the Higgs boson discovered recently at CERN
- How? → At a future linear positron-electron collider
- Two alternative proposals underway:

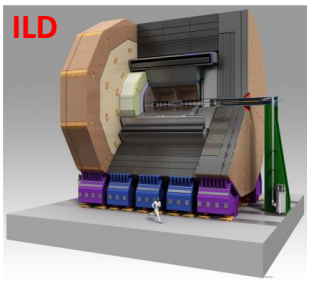


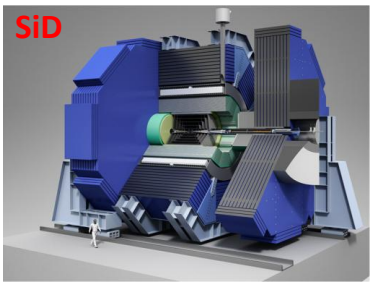


• **Energy**	500 GeV (1 TeV upgrade)	500 GeV (3 TeV upgrade)
• **Accelerating gradient**	31.4 MeV/m (SCRF)	100 MeV/m (2-beam acceleration scheme)
• **Luminosity**	$2.70 \cdot 10^{34}$ cm^{-2}s^{-1}	$5.90 \cdot 10^{34}$ cm^{-2}s^{-1}

HEP experiments. Detector systems for ILC/CLIC.

- Detectors → To reconstruct the events generated right after the collisions
- Two validated detector proposals → (adopted by ILC and CLIC)





- **Subdetector arrangement (ILD):**

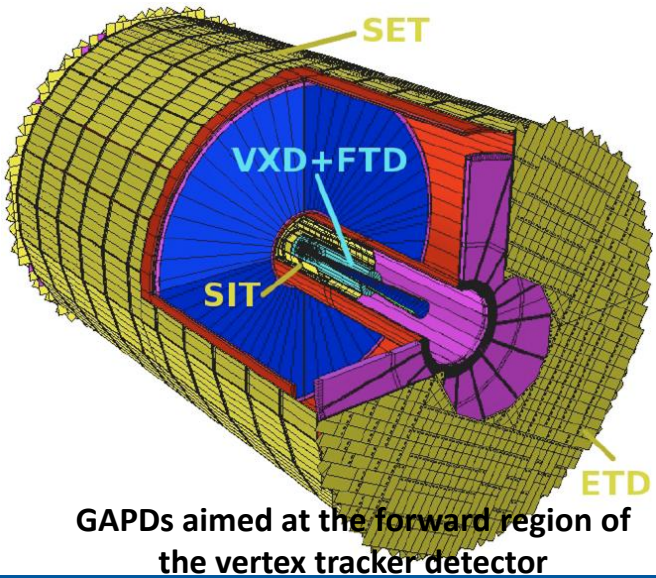
Vertex detector

- Barrel
- VTX **(3 double Si pix layers)**
- To measure space points where particles are produced

Tracker detector

- Barrel
- SIT + SET **(2 + 2 Si strips)**
- TPC (MPGD readout)

- End cap
- FTD **(2 Si pix + 5 Si strip disks)**
- ETD **(2 Si trip layers)**
- To measure track curvature of charged particles (momentum)



GAPDs aimed at the forward region of the vertex tracker detector

Electromagnetic calorimetry

- ECAL (W absorber)
- To measure particles energy

Hadronic calorimetry

- HCAL (Fe absorber)
- To measure particles energy

Muon system
- To identify isolated muons

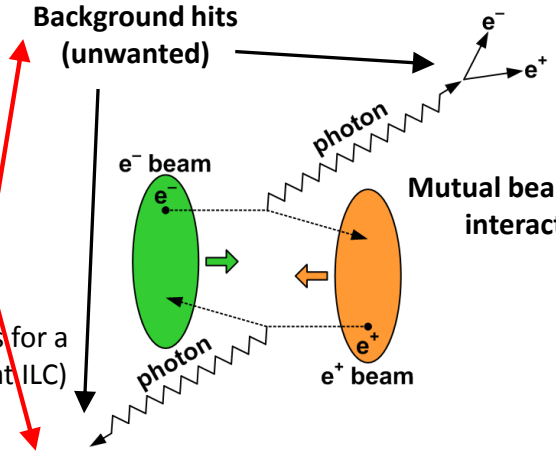
Coil
- Magnet system (3.5 T)

HEP experiments. Tracking detector requirements.

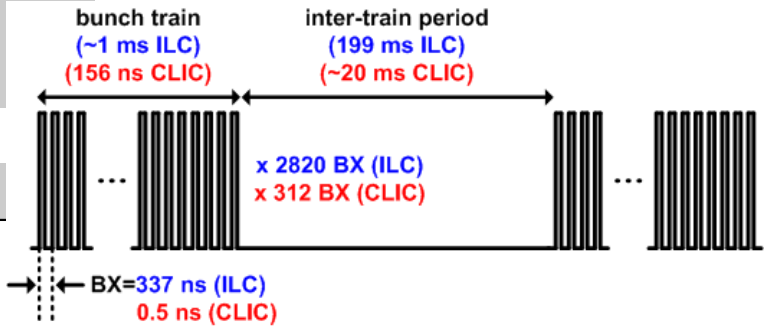
- The physics targets at ILC and CLIC impose very demanding requirements on tracking detectors:

Requirement	Value	Detector design
σ_{point}	<5 µm	Pixel size <17 µm
Material budget	<0.15% X_0 per layer (ILD) <0.30% X_0 per layer (SiD) (↓ Coulomb multiscatt.)	<150 µm per layer (ILD) <300 µm per layer (SiD) + no active cooling
Granularity	High	High number of pixels
Occupancy	<1% (with background hits)	High timing resolution: - Single BX - Time-slicing (each 50 µs for a 25 µm x 25 µm sensor at ILC) - Time-stamping
Radiation tolerance	ILC → 1 kGy/year (TID) + 10^{11} n_{eq}/cm^2/year (NIEL) CLIC → 200 Gy/year (TID) + 10^{10} n_{eq}/cm^2/year (NIEL)	Include mitigation techniques
Power	<a few mW/cm^2	Low power
+ EMI immunity and affordable cost		

Beamstrahlung process:



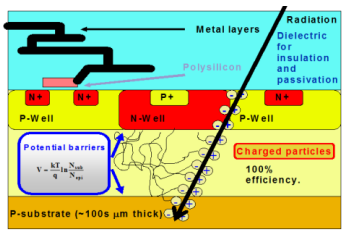
ILC/CLIC beam structure:

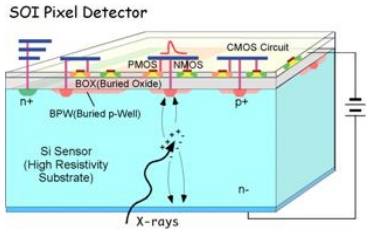


HEP experiments. Tracking technology options.

- **<u>New CMOS pixel technologies are being developed in parallel with the accelerator</u>:**

Requirem./Detector	DEPFET	MAPS	FPCCD	Chrono.	Timepix	GAPD	SOI
σ_{point} (µm)	~1	~3	–	~3	2.3	~5	~1
Material budget (µm)	50	50	50	50-100	300	250	70
Granularity (µm x µm)	20 x 20	18.4 x 18.4	5 x 5	10 x 10	55 x 55	20 x 100	13.75 x 13.75
Timing	integration	integration	integration	stamping	stamping	single BX	integration
Radiation tolerance	10 kGy	10 kGy 10^{13} n_{eq}/cm^2	10^{12} e–/cm^2	–	4 Mgy	–	1 kGy
Power	5 W/detec.	250 mW/cm^2	16 mW/ch	–	886 mW/cm^2	–	–
Fill-factor (%)	100	100	100	100	87	67 (90)	100





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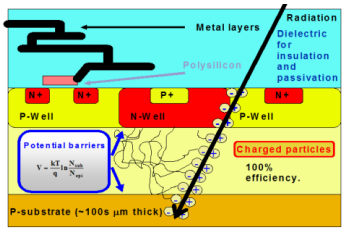

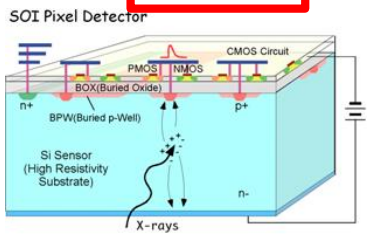

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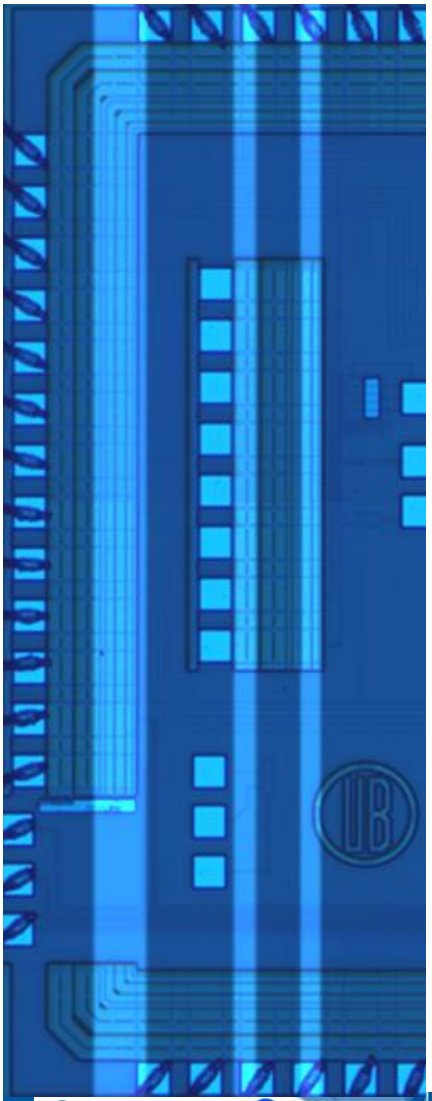

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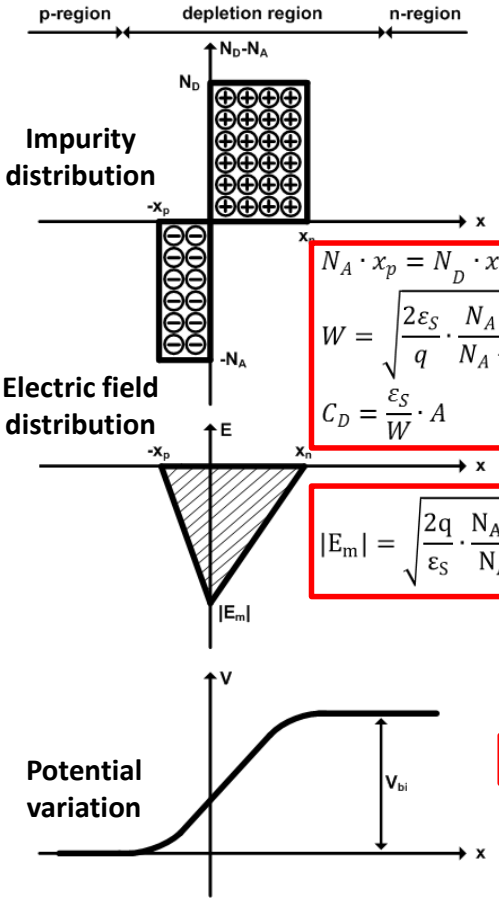
Principle of operation of GAPDs.

An avalanche photodiode is based on a p-n junction



Impurity distribution

Electric field distribution

Potential variation

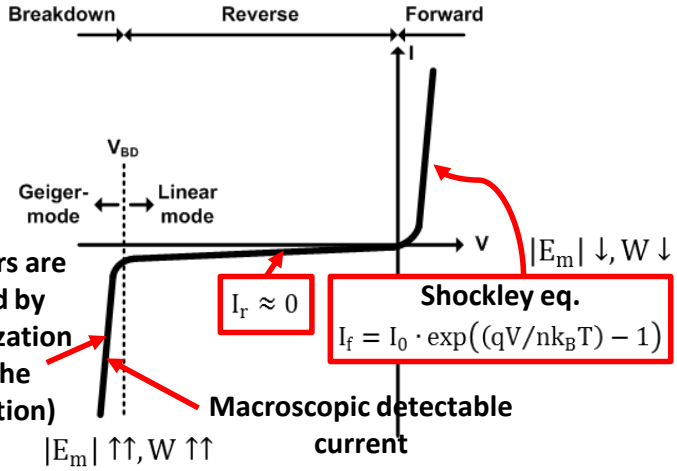
$$N_A \cdot x_p = N_D \cdot x_n$$

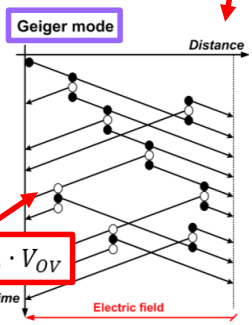
$$W = \sqrt{\frac{2\varepsilon_S}{q} \cdot \frac{N_A \cdot N_D}{N_A + N_D} \cdot V_{bi}}$$

$$C_D = \frac{\varepsilon_S}{W} \cdot A$$

$$|E_m| = \sqrt{\frac{2q}{\varepsilon_S} \cdot \frac{N_A + N_D}{N_A \cdot N_D} \cdot V_{bi}}$$

If an external bias is applied





$$Gain_{GAPD} = C_D \cdot V_{OV}$$

e– and h+ (self-sustained)

Geiger APD (GAPD)

- $Gain_{GAPD} \approx 10^5$-10^6
- Binary device
- To detect single photons and MIPs

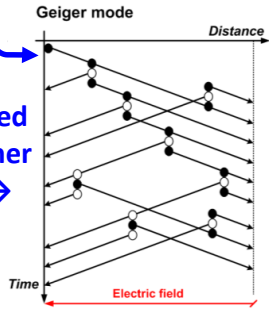
Linear APD

- Not self-sustained
- $Gain_{APD} \approx$ impinging radiation flux
- To determine energy

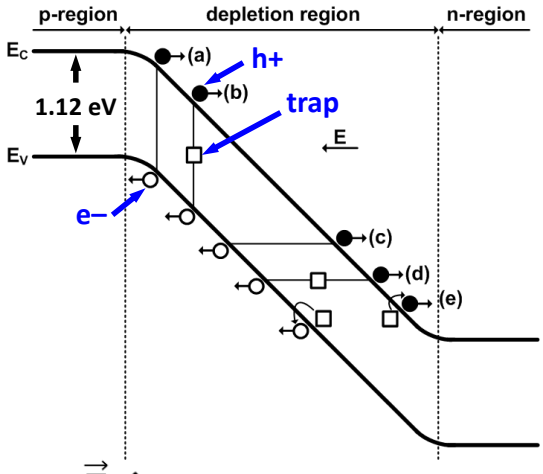
Main figures of merit. Noise.

Primary carrier triggers avalanche

(due to absorbed radiation or other phenomena → noise)



Sources of noise counts in GAPDs:



1. Dark counts (uncorrelated noise)

(a) Thermal generation (SRH)
(b) Trap assisted thermal/SRH generation
(c) Band-to-band tunneling
(d) Trap assisted tunneling

- Measured as **dark counts/s (Dark Count Rate)**
- Dependent on - fabrication process (traps)
  - sensor surface (area)
  - reverse bias overvoltage (V_{OV})
  - working T
- Reduced by - area ↓, V_{OV} ↓, T ↓

2. Afterpulses (correlated noise)

(e) e– (left) and h+ (hole) afterpulses

- Dependent on - trapping centers
  - number of charge carriers
- Reduced by - C_P (parasitic capacitance) ↓
  - active quenching
  - dead time ↑

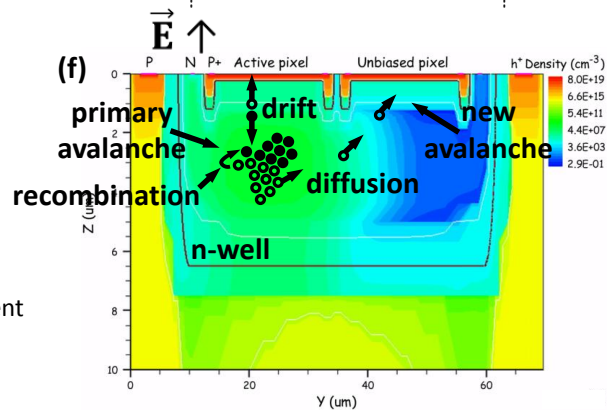
3. Crosstalk (correlated noise)

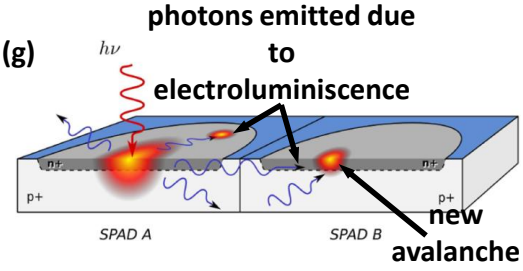
(f) Electrical crosstalk

- Dependent on - pixel separation
- Suppressed by - using different wells

(g) Optical crosstalk

- Dependent on - pixel separation
- Reduced by - limiting Geiger current
  - using trenches





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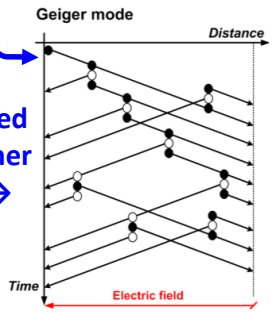
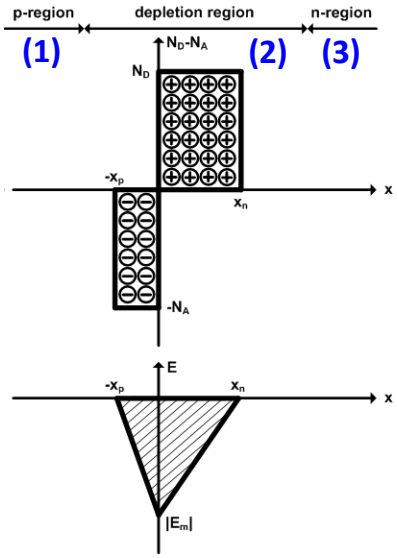


High energy particle detection:



- MIPs → **80 e^--h^+ per Si µm**
- Probability for a primary e^--h^+ pair to trigger an avalanche:

$$P_{trigger}(x) = P_e(x) + [1 - P_e(x)] \cdot P_h(x)$$

$$\frac{d}{dx}P_e(x) = (1 - P_e) \cdot \alpha_e \cdot P_{trigger}$$

$$\frac{d}{dx}P_h(x) = -(1 - P_h) \cdot \alpha_h \cdot P_{trigger}$$

ionization coefficients

- $P_e(x) >> P_h(x)$
- **$P_{trigger}(x)$ is maximum at the center of the junction and decreases to 0 at $-x_p$, x_n**
- **In 2, carriers may start an avalanche breakdown**
- **In 1 and 3, carriers have to diffuse to 2**

Photon detection probability

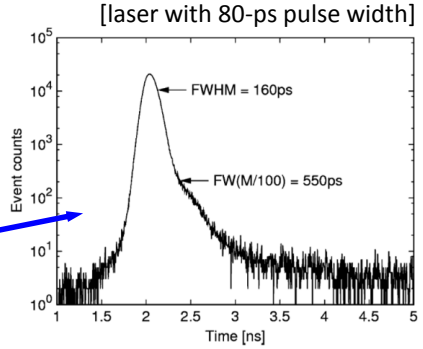
$$PDP = QE(\lambda) \cdot P_{trigger} \cdot FF, \qquad QE(\lambda) = \frac{\text{num } e^- - h^+ \text{ created}}{\text{num incident photons}}$$

- It ranges from 350 nm to 1000 nm in CMOS GAPDs

Time resolution

- Time delay between the arrival of radiation and the leading edge of the output pulse
- Depends on sensor and readout electronics
- Affected by fluctuations (sensor → depth and position)

[laser with 80-ps pulse width]

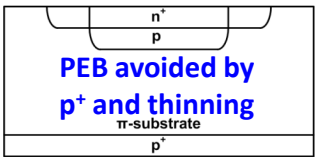


D. Stoppa et al., IEEE Sens. J., 2009

State-of-the-art. Custom vs CMOS GAPDs.

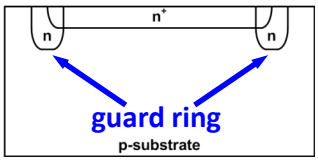
Custom GAPDs

a. Reach-through



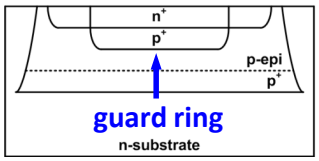
McIntyre (1970's)

b. Planar



Haitz (1960's)

c. Double epitaxial

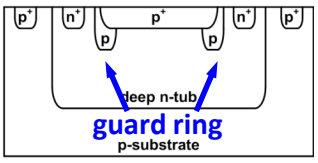


Cova (1980's)

- Excellent detection and timing properties
- Low DCR < 1 kHz (ultra-clean fabrication)
- Low afterpulsing
- Large area detectors are possible
- Not suitable for integration of sensors + readout electronics

CMOS GAPDs

d. HV-CMOS

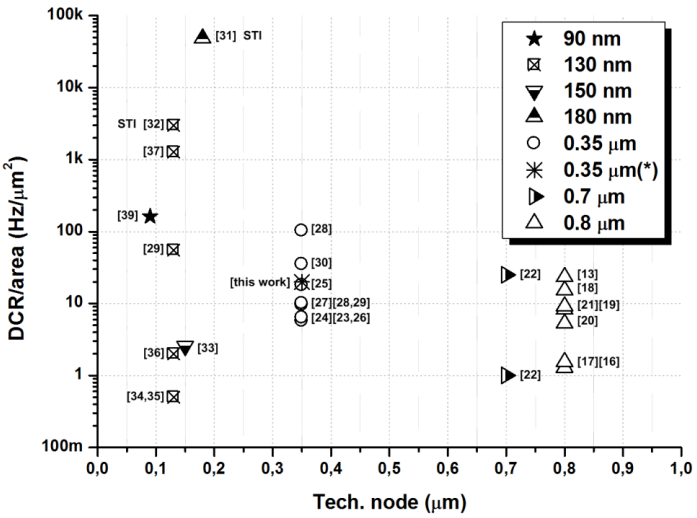


Rochas (2003)

- Several different configurations are possbible:
- n^+ on p-substrate, n-well as guard ring
- p^+-diff in deep n-well, low doped p as guard ring

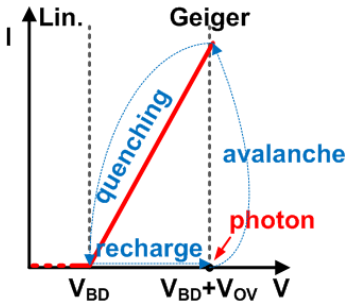
- Possibility to integrate sensors + readout electronics on the same chip
- Possibility to include advanced functions in the in-pixel electronics
- Very good timing properties
- Acceptable detection properties
- Moderate DCR without STI (1 Hz/μm² < DCR < 10^2 Hz/μm²)
- High DCR with STI (DCR ≈ 50 kHz/μm²)
- Low fill-factor (< 10% in many cases)
- Low cost

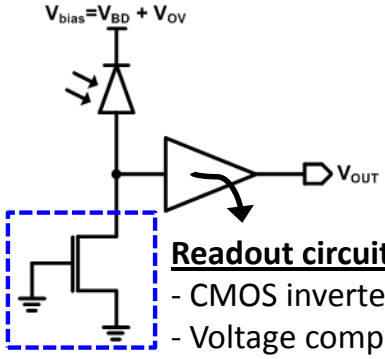
Typical noise trend in CMOS GAPDs



Front-end electronics. Quenching and recharge circuits.

Passive quenching and recharge

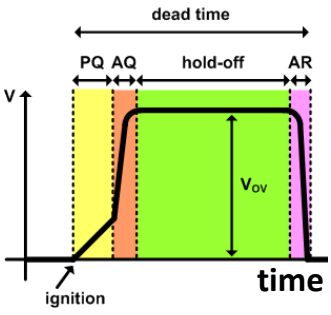


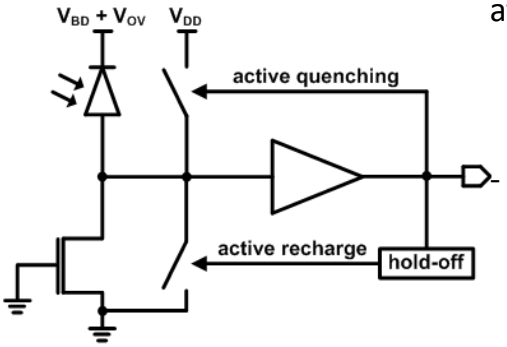


Readout circuit:
- CMOS inverter
- Voltage comparator
- Source follower

- **Quenching** → lower $V_{bias}=V_{BD}$ after an avalanche
  - Resistive element in series with the sensor
  - Resistor with 10^2 kΩ (area ↑) or MOS transistor with proper (W/L) and bias
  - $\tau_Q=(C_D+C_P)\cdot R_D$
- **Recharge** → increase $V_{bias}>V_{BD}$ after quenching
  - Quenching element is used for recharge too
  - $\tau_R=(C_D+C_P)\cdot R_Q$
  - Poor control over quenching and recharge times
  - R_Q ↑, τ_Q ↓, τ_R ↑ (and vice versa)

Active quenching and recharge





- **Quenching** → sense the rising edge of the avalanche and react back on the sensor ($V_{bias}<V_{BD}$)
  - To minimize the number of generated carriers
  - Difficult to implement
  - Required circuits have to be faster than 10^2 ps
- **Recharge** → full control over the recharge time
  - MOS switch
  - Possibility to introduce a hold-off time to release the trapped carriers (afterpulsing ↓)

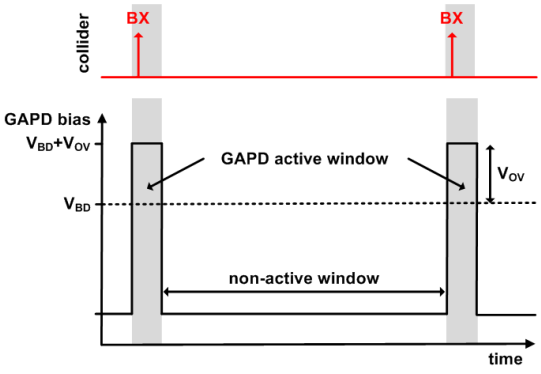
Front-end electronics. Sensor mode of operation.

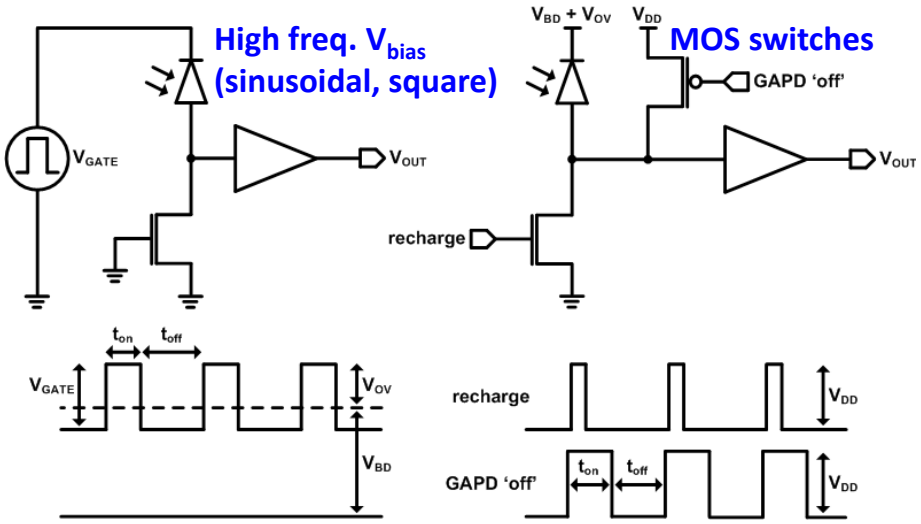
Free running

- The sensor is always ready to trigger an avalanche

Time-gated mode

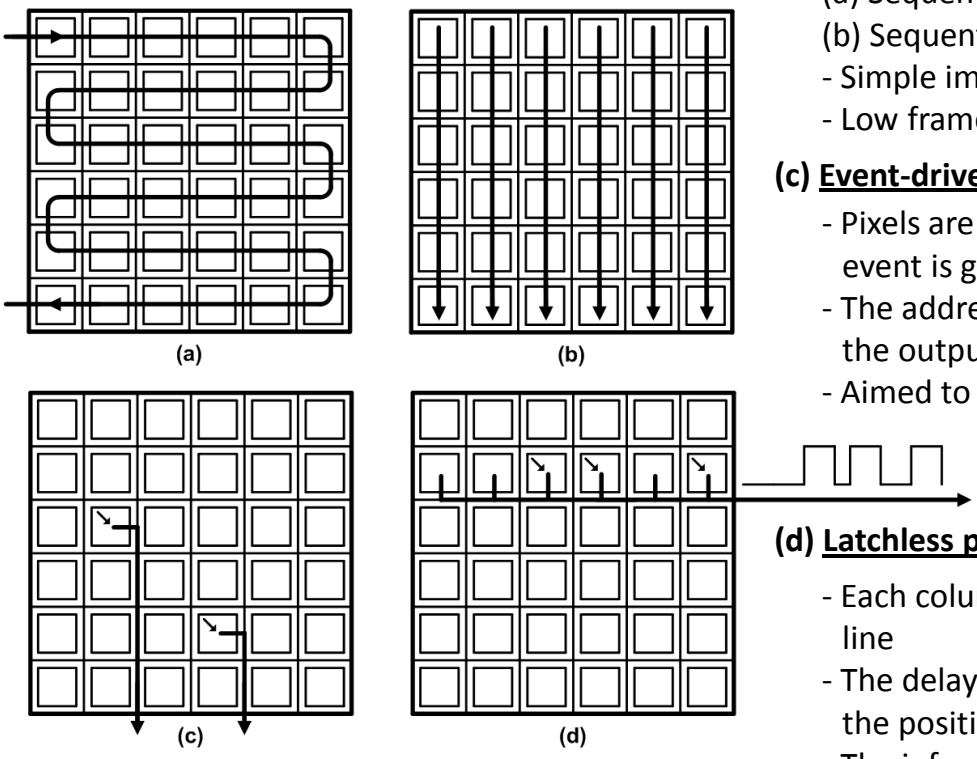
- Valid for those applications where the signal time arrival can be known in advance (HEP experiments, time-gated FLIM or gated-SPECT)
- The sensor is periodically activated and deactivated under the command of a trigger signal
- The active short periods (discretized measurements) can be made coincident with the expected signal arrival
- Reduces the detected dark counts, avoids afterpulses, reduces the detected crosstalks
- Improves efficiency





Front-end electronics. Array architecture.

GAPD cameras are composed of a moderate or large number of pixels



Random access

(a) Sequential readout pixel-by-pixel
(b) Sequential readout by columns
- Simple implementation
- Low frame rates

(c) Event-driven readout

- Pixels are read out asynchronously when an event is generated
- The address (row) of the pixel is sent through the output column
- Aimed to very low intensity applications

(d) Latchless pipelined readout

- Each column is used as a time-preserving delay line
- The delay time contains the information about the position of the pixel
- The information can be reconstructed by a TDC at the end of the column

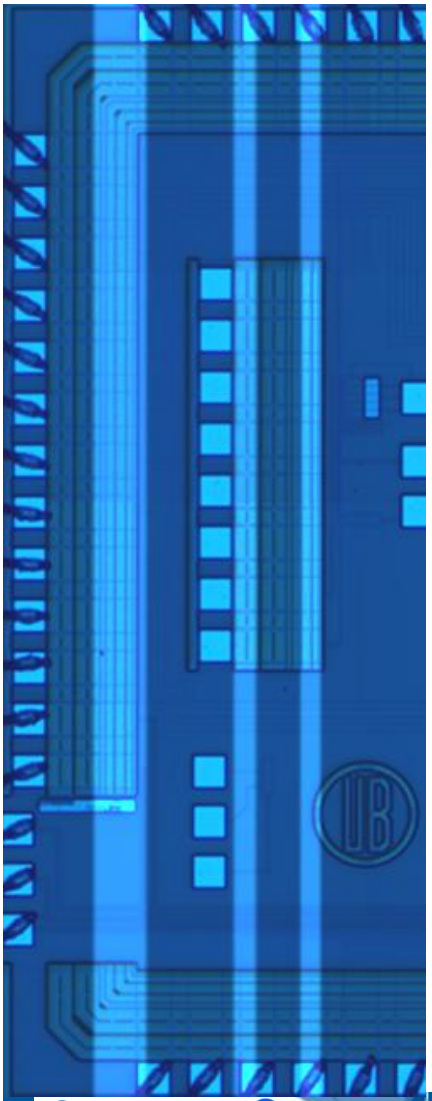
Why Geiger-APDs for tracking?

- A particle tracker is a yes/no application
- It is not necessary to measure the energy of the particle
- A binary device like a GAPD suits the application

- **Performance of GAPDs:**
  - Virtually infinite gain of 10^5-10^6
  - High sensitivity (single-photon sensitivity)
  - Fast timing response (possibility of single BX in some future colliders)

- **Implementation:**
  - Possible in CMOS technology
  - Simple design
  - Simple readout (it's a binary sensor)

- **Questions to answer:**
  - Noise? Fits collider requirements?
  - Sensitivity of GAPDs in particle tracking?
  - Fill-factor? Need to cover >90% of the area



➢Outline

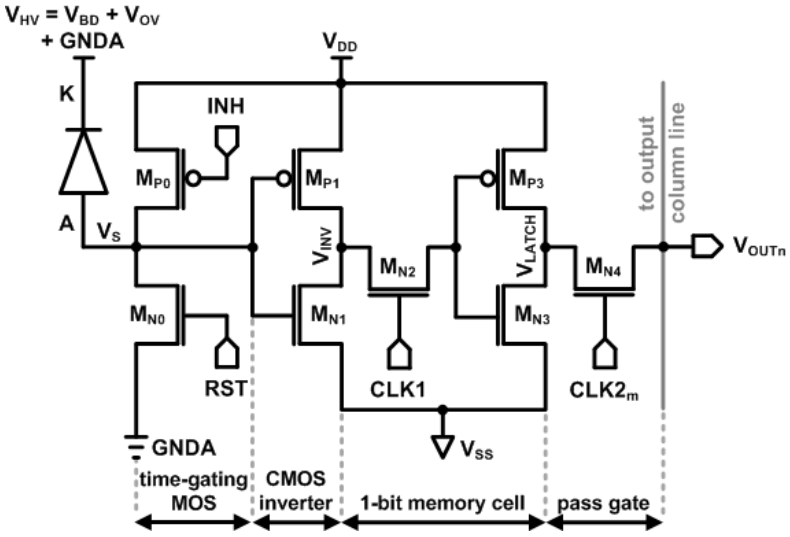
1. Potential applications
   - Future linear lepton colliders
   - Detector systems in ILC/CLIC
2. GAPDs in CMOS technologies
   - Principle of operation and figures of merit
   - State-of-the-art
   - Front-end electronics
3. **Large arrays in a HV-CMOS process**
   - Design and characterization
4. Large arrays in a 3D process
   - Design

Conclusion

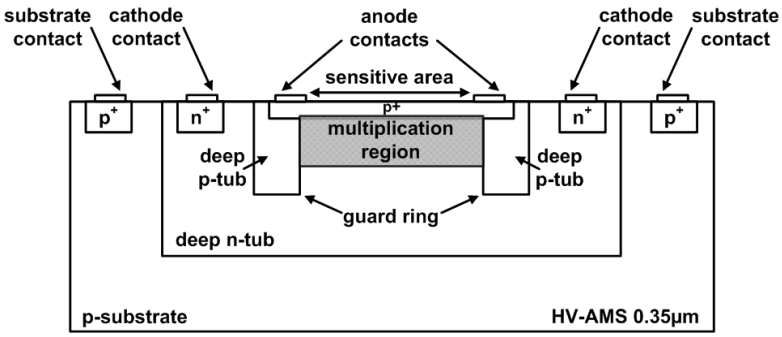
GAPD pixel array for particle detection. Design.

- Target → Reduce the high pattern noise typical of GAPDs
- How? → Analysis of different possible solutions:
  - Dedicated technologies with lower doping profiles → expensive (in favor of standard CMOS) ☹
  - Active quenching → increase of area occupation + reduction of afterpulses only ☹
  - Cooling methods with air cooling → ok, but not main idea ☺
  - Time-gated operation → ok (fine for HEP applications) ☺
  - + operate at low V_{OV} to reduce the DCR (fine for HEP applications) ☺

Time-gated GAPD pixel with low V_{OV}



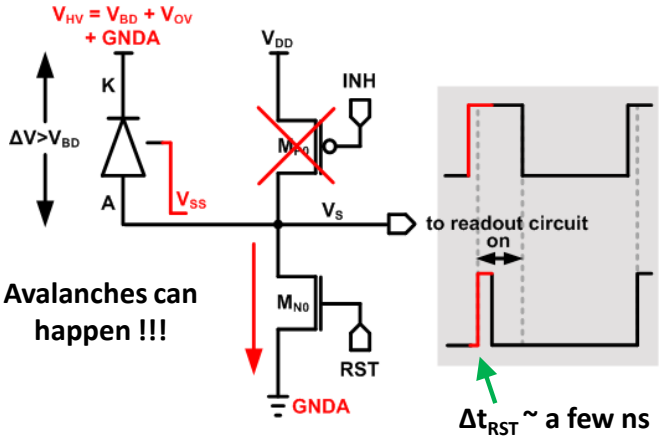
GAPD design in a 0.35 µm HV process



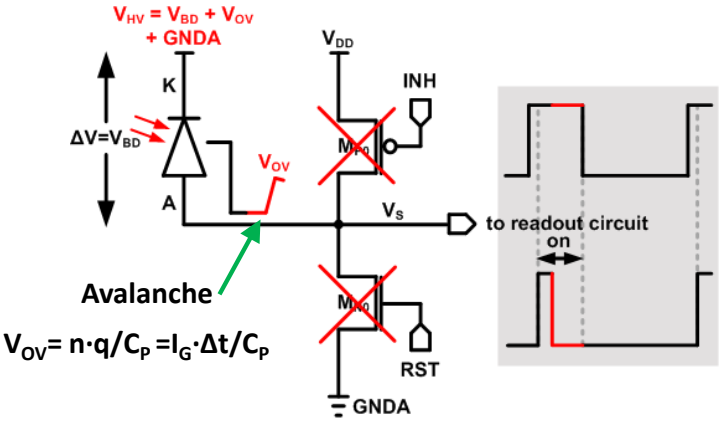
- p^+ diffusion on an n-well
- p implantation as guard ring
- Round shaped corners
- Size → 20 µm (x) x 100 µm (y)
- Based on A. Rochas et al., Rev. Sci. Instrum., 2003

Time-gated GAPD pixel with low V_{OV}. Design.

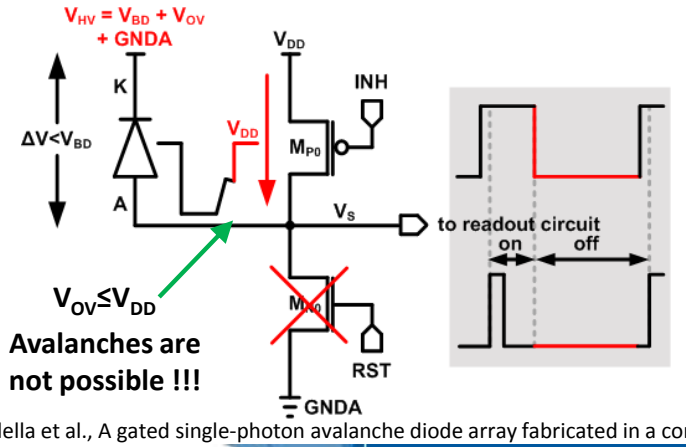
1) Gate-on period is started. Recharge and observation.



2) Gate-on period. Observation (only).



3) Gate-off period.



Time-gated photodiode

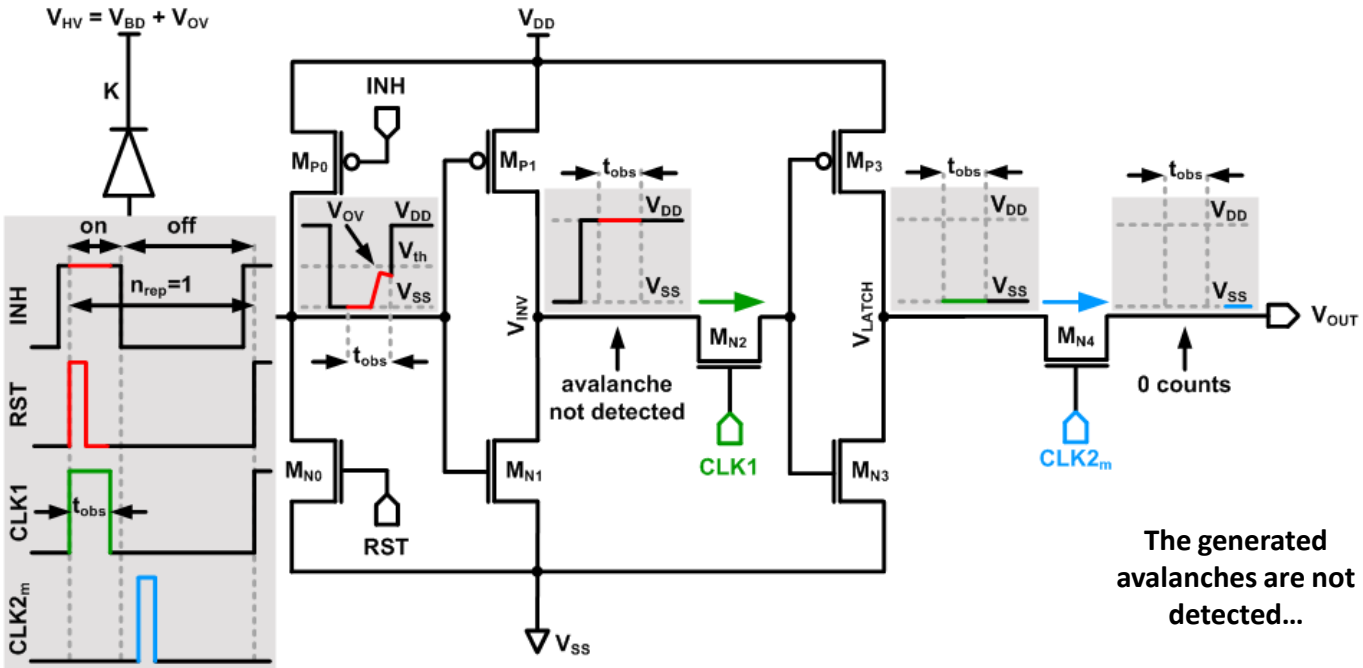
- Long enough gate-off periods the suppress the afterpulsing probability
- Short gate-on periods to reduce the DC probability
- Very short gate-on periods to eliminate the electrical crosstalk probability

- $C_{photodiode}$ = 540.19 fF at 1 V of V_{OV}
- C_P = 15 fF

E. Vilella et al., A gated single-photon avalanche diode array fabricated in a conventional CMOS process for triggered applications, Sens. Actuators A: Phys 186, 2012.

Time-gated GAPD pixel with low V_{OV}. Design.

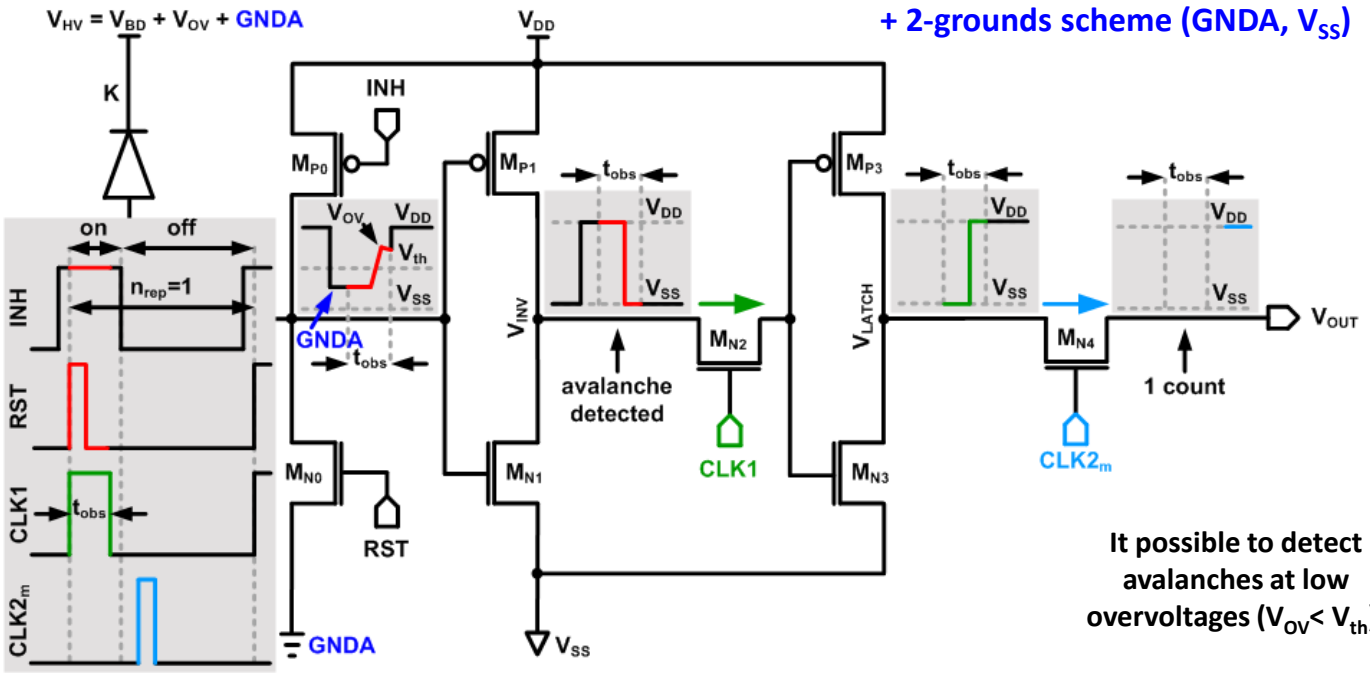
- Target → Voltage-mode readout circuit to operate the sensor at low V_{OV} and reduce the DCR + with low area occupation
- Problem → Difficult to implement in HV-AMS 0.35 µm
- Example readout circuit
  - 1 voltage discriminator **(CMOS inverter with $V_{th}=V_{DD}/2$, $V_{DD}=3.3$ V)**
  - 1-bit memory cell (time-gated synchronously with the sensor)
  - 1 pass gate to activate the pixel readout



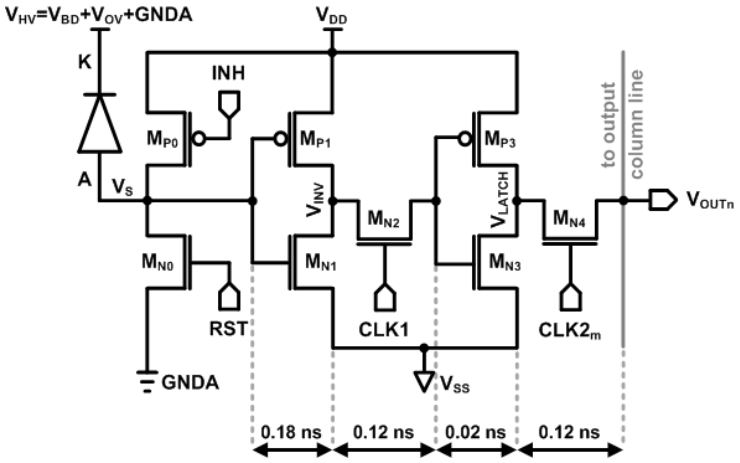
The generated avalanches are not detected…

Time-gated GAPD pixel with low V_{OV}. Design.

- Target → Voltage-mode readout circuit to operate the sensor at low V_{OV} and reduce the DCR + with low area occupation
- Problem → Difficult to implement in HV-AMS 0.35 µm
- Implemented readout circuit - 1 voltage discriminator **(CMOS inverter with $V_{th}=V_{DD}/2$, $V_{DD}=3.3$ V)**
  - 1-bit memory cell (time-gated synchronously with the sensor)
  - 1 pass gate to activate the pixel readout



Time-gated GAPD pixel array. Design.

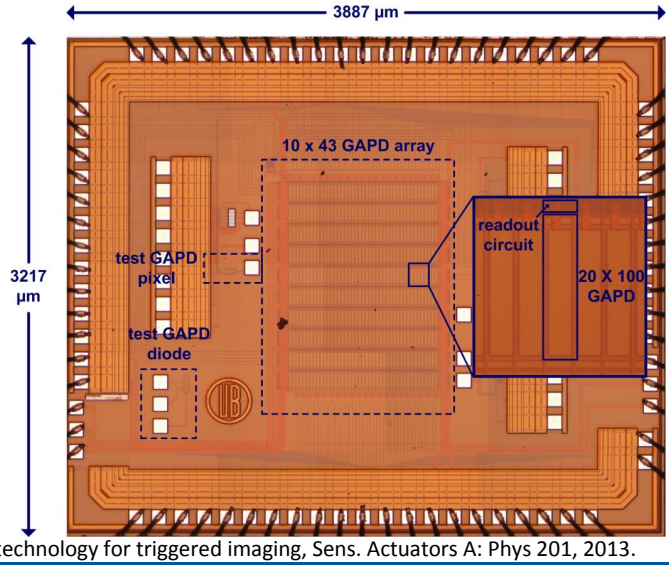


Features

- Monolithically integrated with the 0.35 µm HV-AMS standard CMOS technology
- 10 rows x 43 columns
- Total sensitive area of 1 mm^2 (to facilitate particle observation at beam-test)
- Sensors placed in the same well to increase the fill-factor (FF=67%)
- Readout circuits placed between two consecutive rows of sensors, pixel pitch = 22.9 µm x 138.1 µm
- Radiation effects mitigation techniques and on-chip data processing are not included

Chip

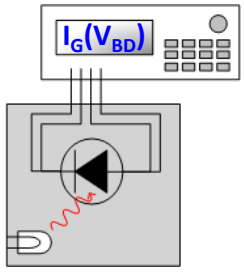
- Sequential readout by rows during gated-off periods
- Sequentially activating C_{LK2m}, with m=[1,10]
- Each output column connected to output buffer and output pad
- No multipliexers nor selection decoders
- 43 output pads + 13 control signal pads (RST, INH, CLK1 and the ten CLK2) + power supply pads
- Δt (from V_S to V_{LATCH}) = 0.32 ns
- Δt (from V_{LATCH} to outside the chip) = 1.33 ns (0.12 ns of C_{LK2m} + 0.26 ns of output buffer + 0.95 of output pad)



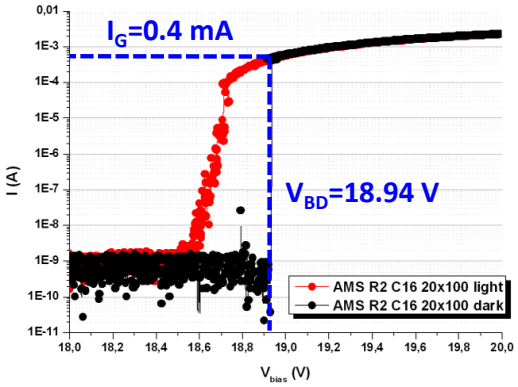
E. Vilella et al., A low-noise time-gated single-photon detector in a HV-CMOS technology for triggered imaging, Sens. Actuators A: Phys 201, 2013.

Time-gated GAPD pixel array. Characterization.

- **Current-voltage curve** (at room temperature)



4-wire method

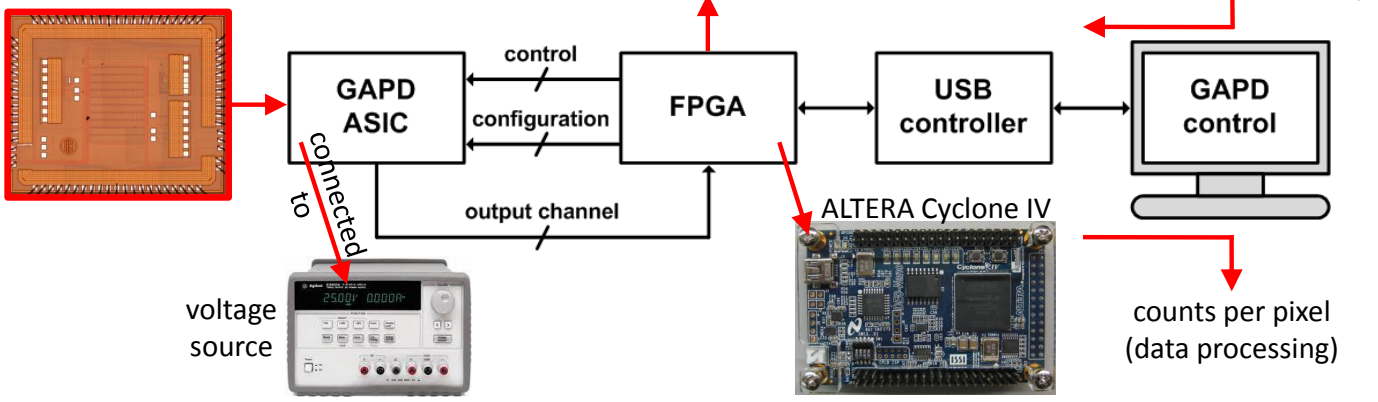


- **Noise and signal**

Testing board

- generate the control signals (t_{obs}, t_{off}, readout)
- count off-chip the number of pulses per pixel
- manage the communication with a PC

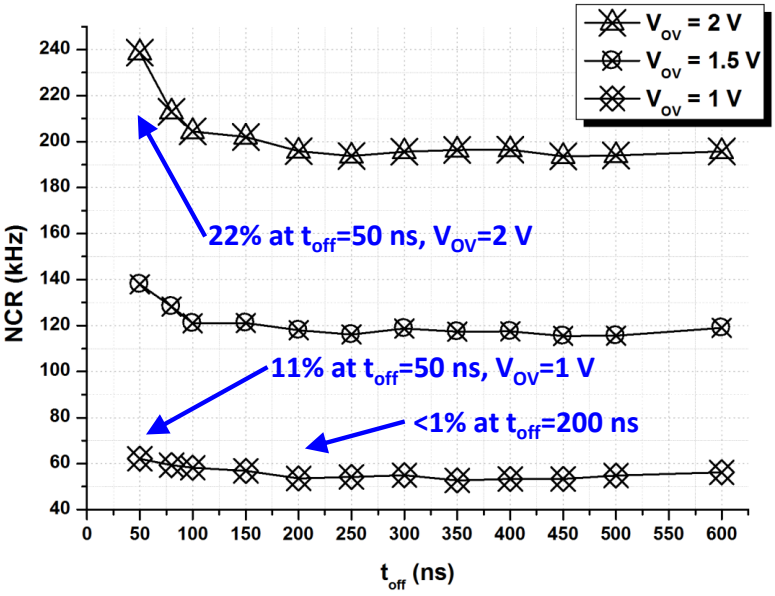
- t_{obs}, t_{off}
- num. repetitions (n_{rep})



Single pixels with voltage-mode readout circuit. Characterization.

- **Afterpulsing probability (in darkness, room T)**

  - t_{obs}=12 ns, $n_{rep}=10^5$
  - Measured at different t_{off}
  - $\text{NCR} = \frac{\text{noise counts}}{t_{obs} \text{ x } n_{rep}}$



- DCR is high; DCR ↓ as V_{OV} ↓

- Long enough gate-off periods suppress the afterpulsing probability

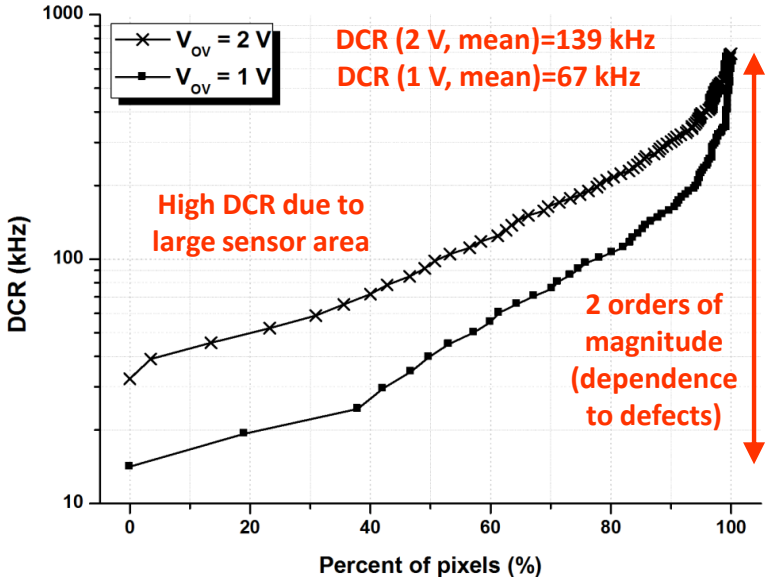
Time-gated GAPD pixel array. Characterization.

- **Dark count rate (in darkness, room T)**

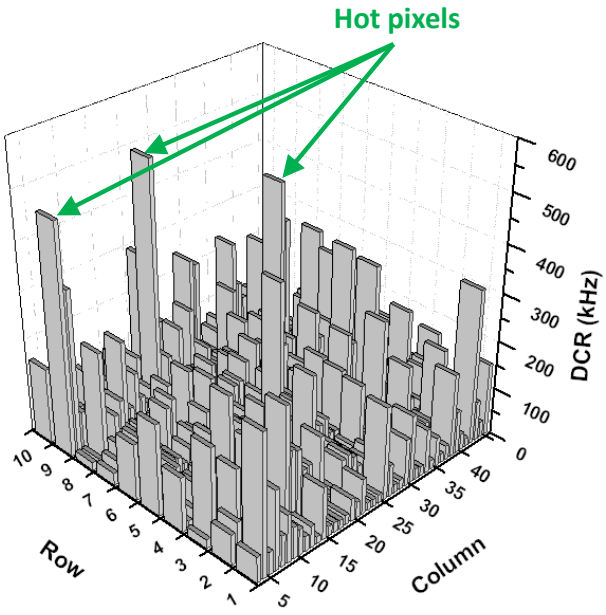
  - V_{OV}=1 V, 2 V (V_{BD}=18.9 V)
  - t_{obs}=1274 ns, t_{off}=1 μs (for data transmission to PC)
  - $\mathrm{DCR} = \frac{\text{noise counts}}{t_{obs} \times n_{rep}}$, no afterpulses but crosstalk

Cumulative plot

- Cumulative percent of pixels ≤ a certain DCR



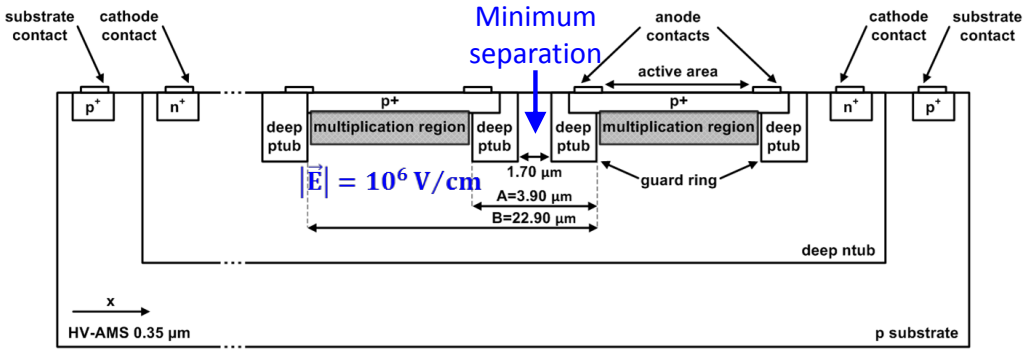
Spatial map (V_{OV}=1 V)



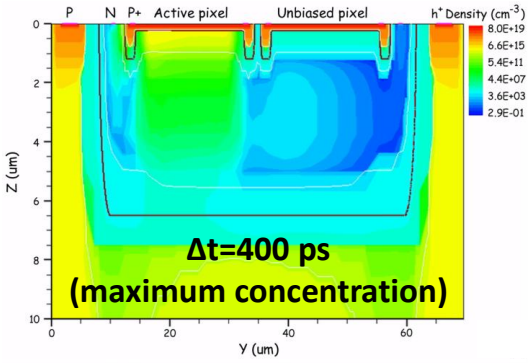
- With the **time-gated mode** → **DCP=10^{-4}** (t_{obs}=1274 ns) → **DCP=10^{-2}** (t_{obs}=4 ns) **[$\mathrm{DCP} = \mathrm{DCR} \times t_{obs}$]**

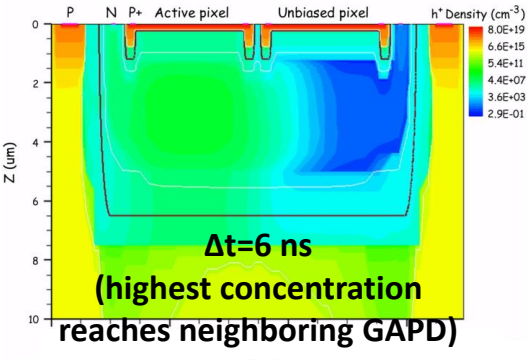
Time-gated GAPD pixel array. Characterization.

- **Electrical crosstalk**
- The GAPDs are placed in the same well to reduce the dead area and increase the fill-factor (FF=67%)



Simulations with ISE-TCAD



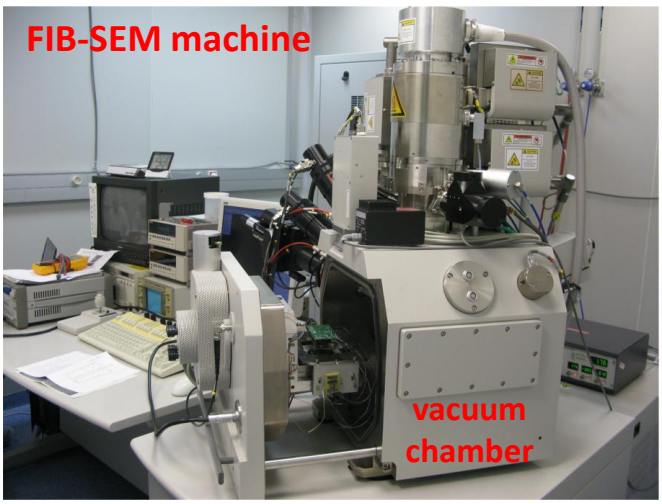


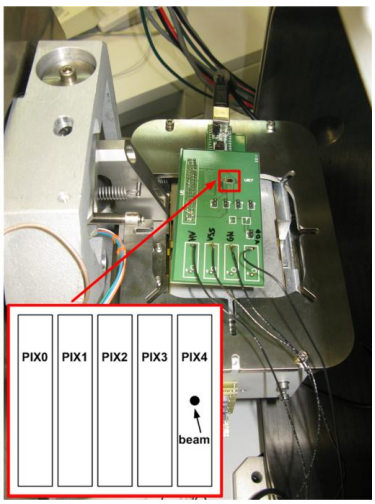
- Presence of **electrical crosstalk?**
- Maximum concentration per avalanche → $C=1\cdot10^{13}$ holes/cm^3
- Concentration to trigger a new avalanche → $C'=1\cdot10^{5}$ holes/cm^3
  - From Fick's 1st and 2nd laws:
  - $\Delta t=164$ ps → C' is at $\Delta x = 3.90$ µm
  - $\Delta t=6.23$ ns → C' is at $\Delta x = 22.90$ µm
- Electrical crosstalk should take place between 164 ps and 6.23 ns
- Good agreement between theoretical and simulated results
- Possibility to reduce the electrical crosstalk with $t_{obs}<6.23$ ns?

A. Vilà, E. Vilella et al., A crosstalk-free single photon avalanche photodiode located in a shared well, IEEE Electron. Device Lett. 35, 2014.

Time-gated GAPD pixel array. Characterization.

- **Characterization of the electrical crosstalk as a function of t_{obs}**
- **<u>Set-up # 1</u>:**





- Electron beam
- Beam energy = 1 keV
- Beam size = 1 nm

- PCB with chip + FPGA placed in the vacuum chamber during the measurements
- Control and display system placed outside the machine

- V_{OV} =2 V
- t_{obs}=100 ns (maximum crosstalk)
- t_{off}=1 µs (no afterpulses)
- n_{rep}=1·10^6

- Problems related to the set-up: Progressive oxide charging due to electron beam (change of V_{BD})
- Not possible to completely characterize

	GAPD array				
	PIX0	**PIX1**	**PIX2**	**PIX3**	**PIX4**
Noise counts in the dark	0.36 k	7.15 k	0.54 k	5.40 k	4.21 k
Net counts after beam	-	-	-	0.15 k	6.70 k

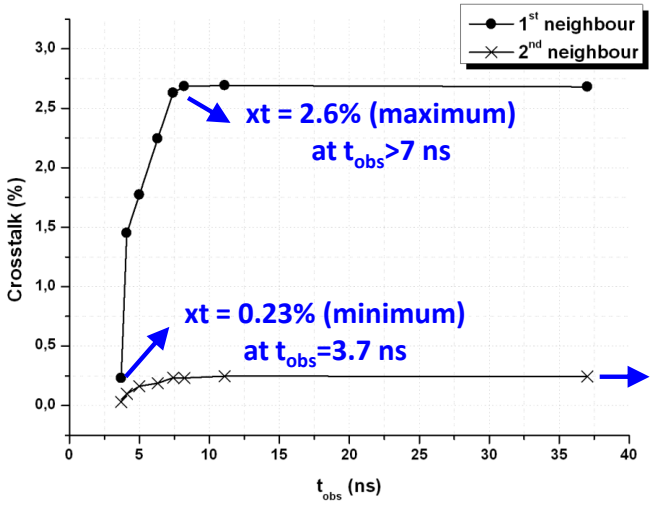
Negligible crosstalk (2nd neighbor and beyond)

2.2% → Maximum electrical crosstalk (1st neighbor)

Time-gated GAPD pixel array. Characterization.

- **Characterization of the electrical crosstalk as a function of t_{obs}**
- **<u>Set-up # 2</u>:**

t_{obs} (ns)	t_m (µs)	PIX0 (2.28 kHz)	PIX1 (42.84 kHz)	PIX2 (3.33 kHz)	PIX1 (32.55 kHz)	PIX4 (25.57 kHz)
3.7	9.6	6 xt (**0.23%**), 0.02 dc	2618	6 xt (**0.23%**), 0.03 dc	0 xt (**0.23%**), 0.03 dc	0
5	17.0	51 xt (**1.50%**), 0.03 dc	3407	66 xt (**1.93%**), 0.05 dc	5 xt (**0.15%**), 0.55 dc	0
7.4	38.0	119 xt (**2.33%**), 0.09 dc	5136	148 xt (**2.88%**), 0.13 dc	13 xt (**0.25%**), 1.23 dc	1
11.1	85.8	189 xt (**2.45%**), 0.19 dc	7732	266 xt (**2.93%**) 0.28 dc	20 xt (**0.25%**), 2.79 dc	1



- Noise counts generated by the sensor in the dark
- V_{OV}=1 V
- t_{obs}=3.7 ns (limited by control system) → 37 ns
- t_{off}=1 µs (no afterpulses)
- # coincidences>20 k
- $\mathrm{xt} = \frac{\text{coincidence counts neighbor}}{\text{noise counts emitter}} \cdot 100$

xt = 0.25%
Random coincidences
+ optical crosstalk (?)

- Good agreement between
  - Theoretical calculations
  - ISE-TCAD simulations
  - Experimental measurements with set-up # 1 and # 2

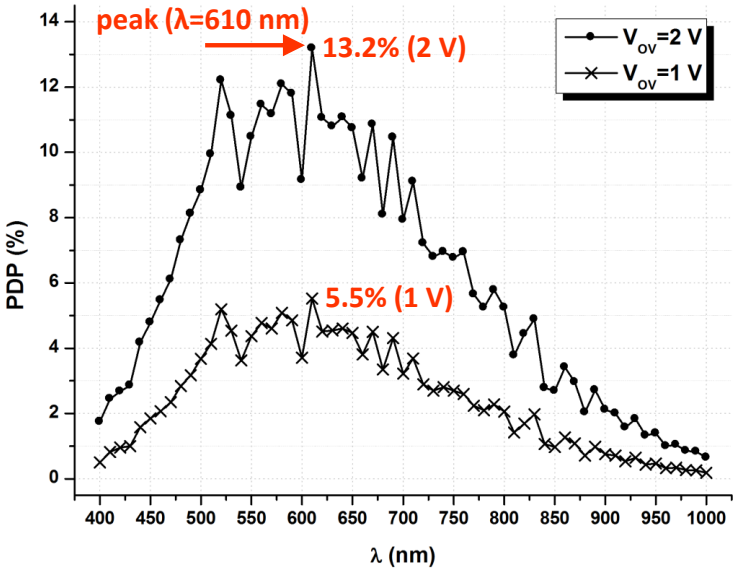
Time-gated GAPD pixel array. Characterization.

- **Photon detection probability**

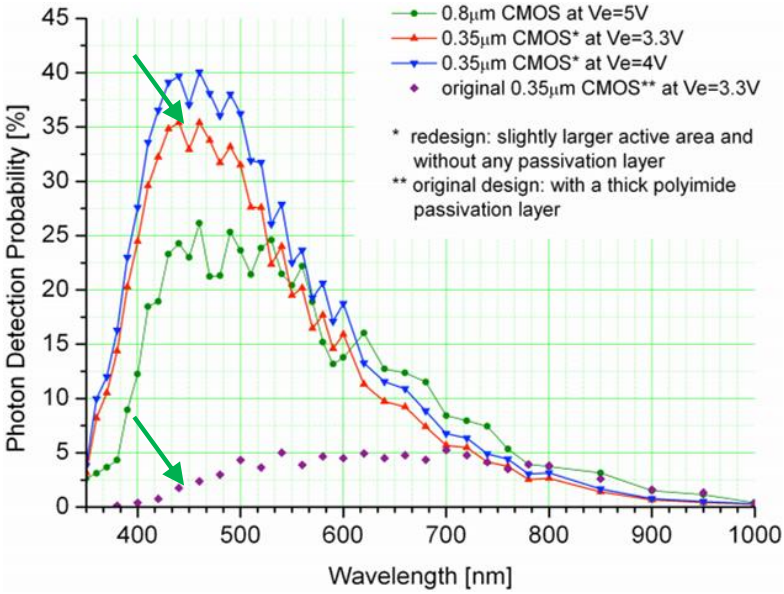
  - V_{OV}=1 V, 2 V
  - t_{obs}=14 ns, t_{off}=1 µs, t_m=1 s (n_{rep}=71 Mframes)
  - Tested with a UV-VIS spectrophotometer and calibrated reference detector

UB mesurements (average value)

- Results are below expectations due to passivation layer



C. Niclass et al, Proc. SPIE, 2006



- Calculated as → $\mathrm{PDP} = \frac{\text{total counts} - \text{noise counts}}{\text{incident photons}}$ (corrected for the detector FF)

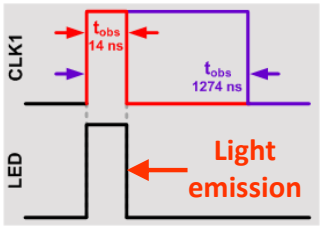
Time-gated GAPD pixel array. Characterization.

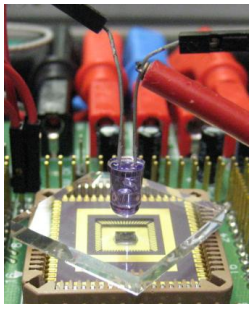
- **Dynamic range**

  - Defined as → $\mathrm{DR} = \log_2\left(\frac{I_{sat}}{I_{th}}\right)$
  - I_{th} → minimum detectable intensity (SNR≈1)
  - I_{sat}→ maximum detectable intensity (saturation of the readout circuit)
  - In imaging applications, it determines the contrast of the generated images

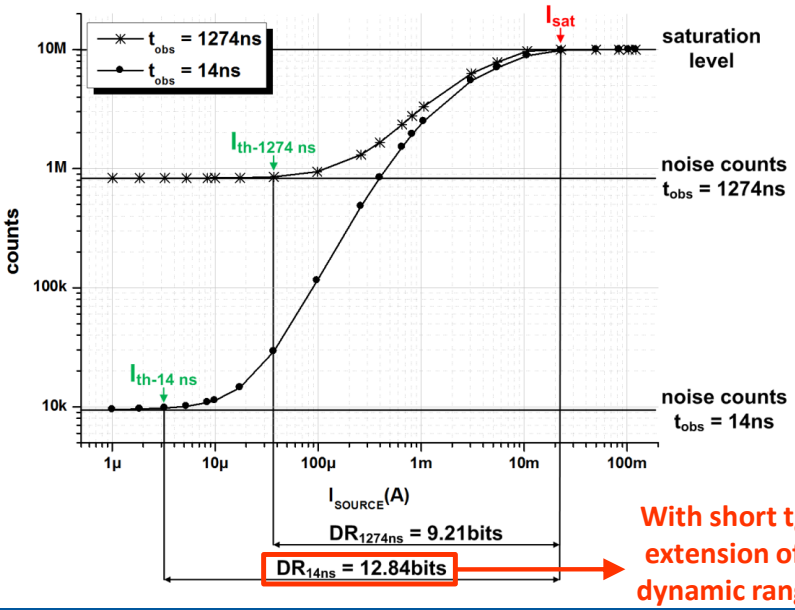
Set-up

- Pulsed light source
- Variable light intensity (λ=880 nm)
- V_{OV}=1 V
- t_{obs}=1274 ns, 14 ns
- t_{off}=1 µs
- n_{rep}=10 Mframes (counter capacity)





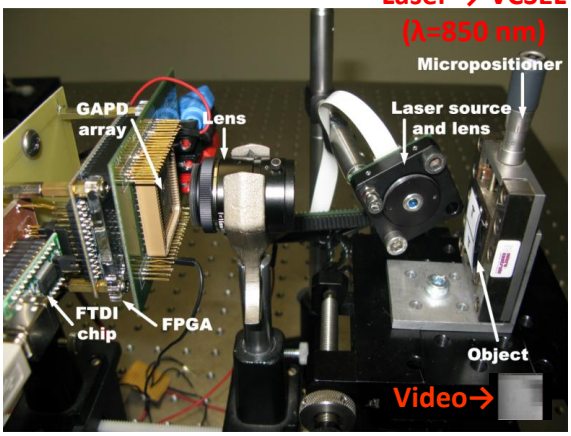
Result (average value)

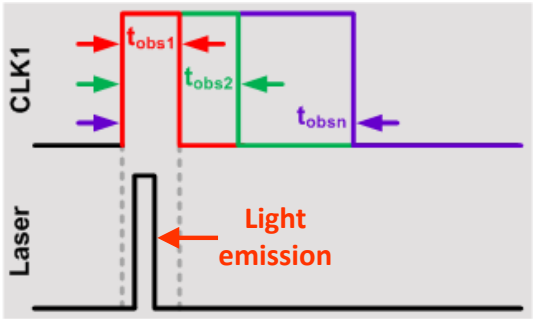


Time-gated GAPD pixel array. Characterization.

- **2D imaging**

Laser → VCSEL (λ=850 nm)





GAPD array

- V_{OV}=1 V
- t_{obs}=1274 ns → 34 ns
- t_{off}=1 µs
- n_{rep}=10 Mframes

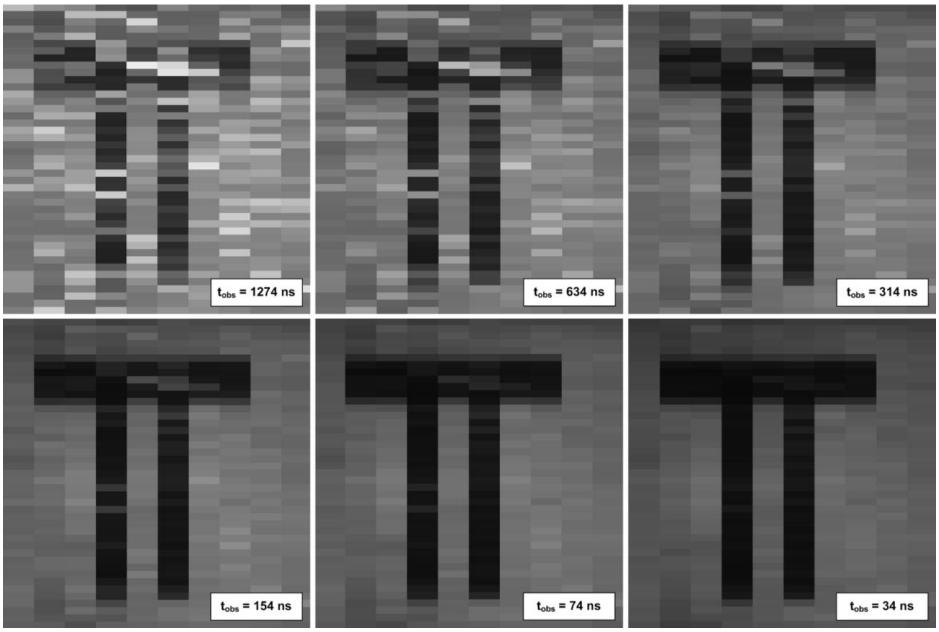
Laser

- t_{on}=22 ns

DCP

- t_{obs}=1274 ns → 0.085 nc/frame
- t_{obs}=34 ns → 0.0023 nc/frame

Reduction of the counter occupancy !!!

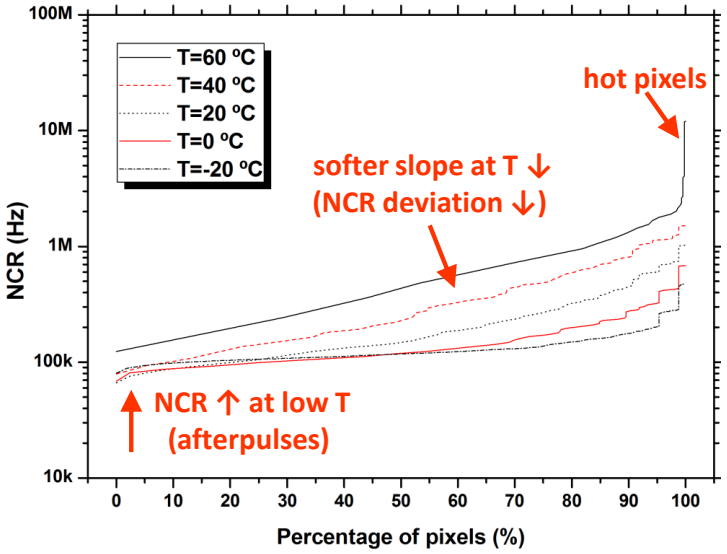


Time-gated GAPD pixel array. Characterization.

- **Thermal effects**

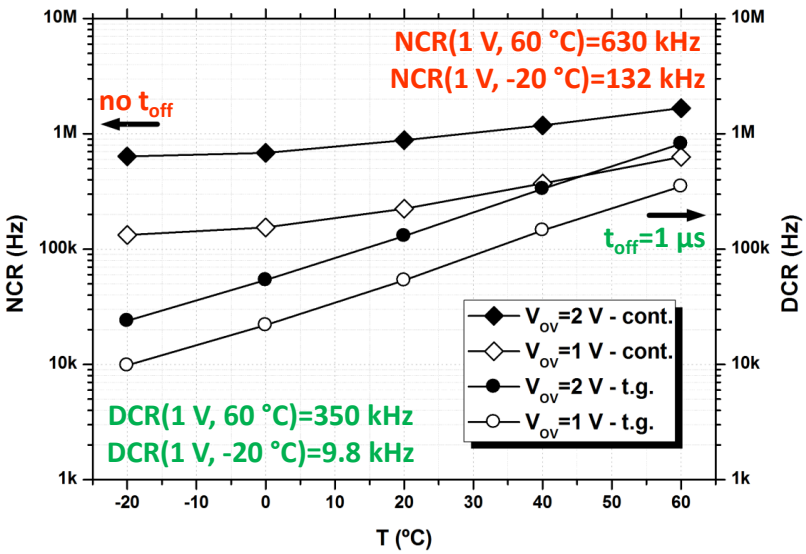
  - Measured in a climatic chamber within the range -20 °C<T<60 °C
  - **V_{BD}** drops with T → $dV_{BD}/dT|_{0.4mA}$=20 mV/°C (weaker ionization coefficients)
  - **DCR** rises with T → roughly multiplied by two every 10 °C (higher SRH generation)
  - **Afterpulsing (NCR)** rises at low T starting at 0 °C (longer trapping lifetimes)

Cumulative plot (NCR)



- NCR → dc + afterpulses + xt
- V_{OV}=1 V
- t_m=14 ms, t_{off}=0 s (continuous mode)

Average value (NCR, DCR)



- DCR → dc + xt (minimum t_{off}=200 ns)
- V_{OV}=1 V, 2 V
- t_{obs}=14 ns, t_{off}=1 µs, n_{rep}=1 Mframes, t_m=14 ms

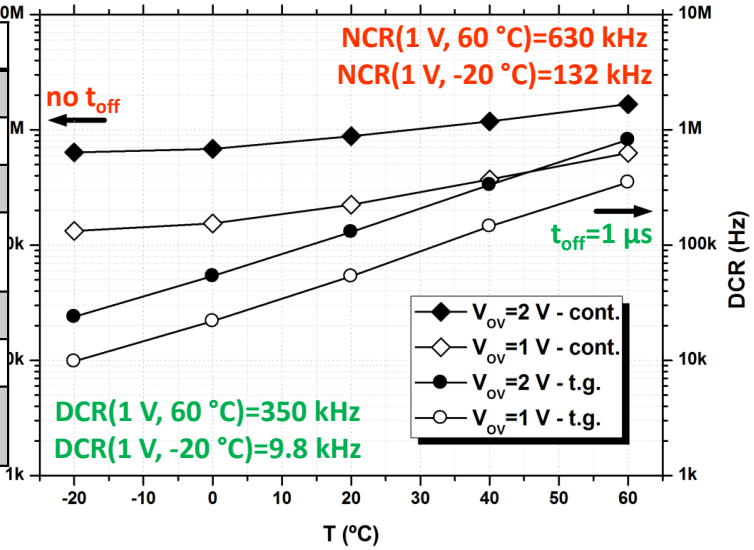
Time-gated GAPD pixel array. Characterization.

- **Thermal effects**

  - Measured in a climatic chamber within the range -20 °C<T<60 °C
  - V_{BD} drops with T → $dV_{BD}/dT|_{0.4mA}$=20 mV/°C (weaker ionization coefficients)
  - **DCR** rises with T → roughly multiplied by two every 10 °C (higher SRH generation)
  - **Afterpulsing (NCR)** rises at low T starting at 0 °C (longer trapping lifetimes)

T (°C)	Noise rate (kHz)	Expected noise counts	
		ILC (2820 BX, 337 ns)	CLIC (312 BX, 0.5 ns)
60	630 (NCR)	1 nc/1.5 µs	
		598 nc/GAPD/train	0.1 nc/GAPD/train
	350 (DCR)	10^{-3} nc/GAPD/BX (t_{obs}=10 ns) 10^{-4} nc/GAPD/BX (t_{obs}=1 ns)	10^{-2} nc/GAPD/train
-20	132 (NCR)	1 nc/7.5 µs	
		125 nc/GAPD/train	0.02 nc/GAPD/train
	9.8 (DCR)	10^{-5} nc/GAPD/BX (t_{obs}=10 ns) 10^{-6} nc/GAPD/BX (t_{obs}=1 ns)	10^{-3} nc/GAPD/train

Average value (NCR, DCR)



- NCR → dc + afterpulses + xt
- DCR → dc + xt

E. Vilella et al., BITE, 2013.

Better conditions for low noise

- a nanosecond time-gating scale
- low working temperature

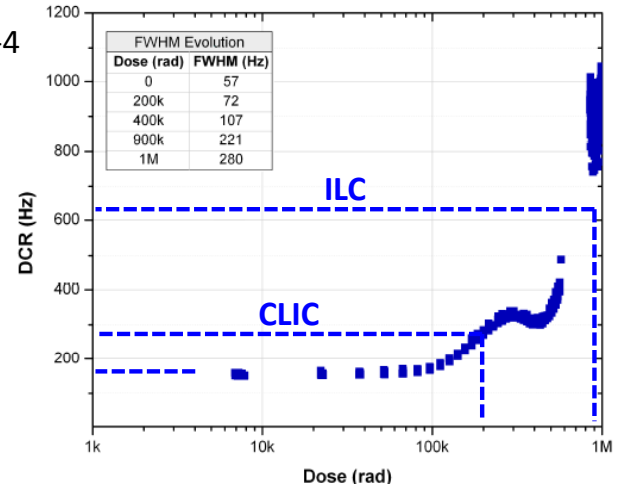
Time-gated GAPD pixel array. Characterization.

- **Radiation effects**

  - A few publications in the literature with irradiated GAPDs in the 0.35 µm HV-AMS technology
  - Publication with γ rays and protons (fluence $8.3 \cdot 10^7$ p/cm2/s, flux of 11 MeV, dose of 40 krad)

  - In ILC/CLIC presence of e^+-e^- pairs and neutrons
  - ILC → 1 kGy/year (TID) + 10^{11} n_{eq}/cm^2/year (NIEL) (x 10 years of operation)
  - CLIC → 200 Gy/year (TID) + 10^{10} n_{eq}/cm^2/year (NIEL) (x 10 years of operation)

  - According to the publication:
  - **ILC** → DCR(10 kGy=1 Mrad, γ ray) increased by a factor 3-4
    DCR(1 V, -20 °C)=9.8 kHz → 36.45 kHz
    DCP(1 V, -20 °C)=10^{-4} → $3 \cdot 10^{-4}$
    (long t_{off}, readout after each BX)
  - **CLIC** → DCR(2 kGy=200 krad, γ ray) increased by a factor 2
    DCR(1 V, -20 °C)=9.8 kHz → 19.6 kHz
    DCP(1 V, -20 °C)=10^{-3} → $3 \cdot 10^{-3}$
    (long t_{off}, readout after each train)



L. Carrara et al., IEEE Intl. Solid-State Circuits Conference, 2009.

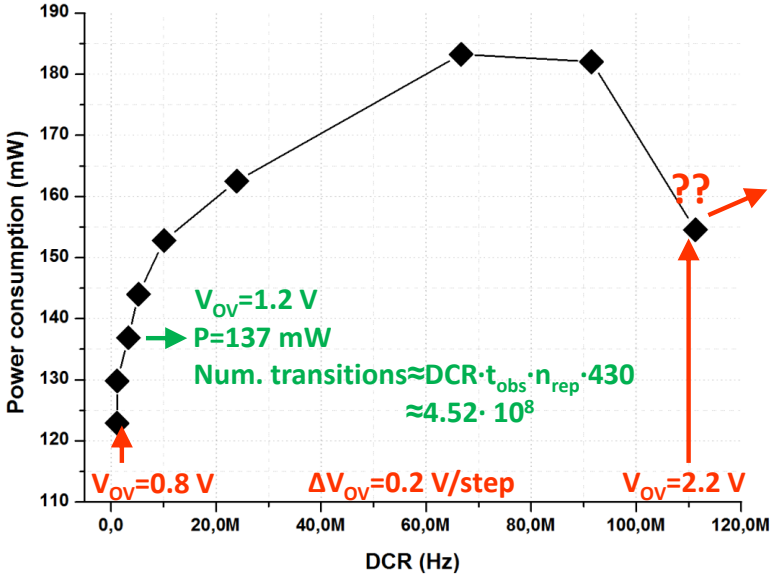
Time-gated GAPD pixel array. Characterization.

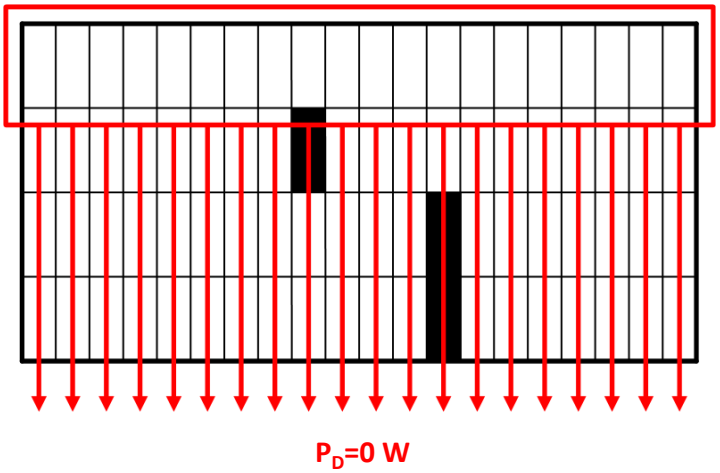
- **Power consumption**

  - P_S is due to non-idealitites → P_S=0 W in HV-AMS 0.35 µm
  - P_D is due to a change of state → $P_D = C_L \cdot V_{DD}^2 \cdot f$
  - P_D is caused by the readout circuits and the output pads of the chip

  P(DCR), the DCR indicates the frequency of operation **GAPD array biased at V_{OV}**

  - t_{obs}=4 ns, t_{off}=1 µs, n_{rep}=100 Mframes (t_m=0.4 s)





$$P_{D,measured} \approx DCR \cdot t_{obs} \cdot n_{rep} \cdot 430 \cdot (P_{D,circ} + P_{D,pad})$$

- $P_{D,pad}$=295 µW/MHz (datasheet foundry)
- $P_{D,cir}$=8 µW/MHz (calculated), 10 µW/HMz (simulated)
- $P_{D,TOTAL}$(1.2 V)=4 mW (circuits) + 133 mW (pads) → **LVDS pad**

Time-gated GAPD pixel array. Characterization.

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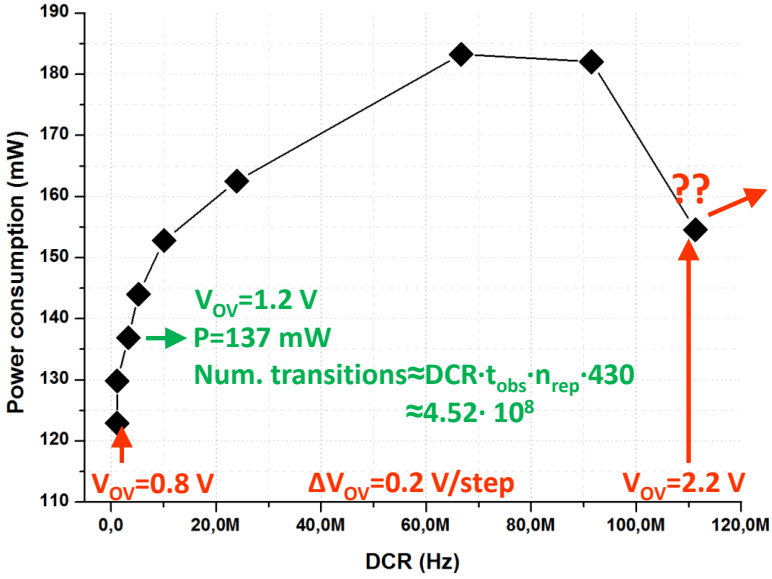

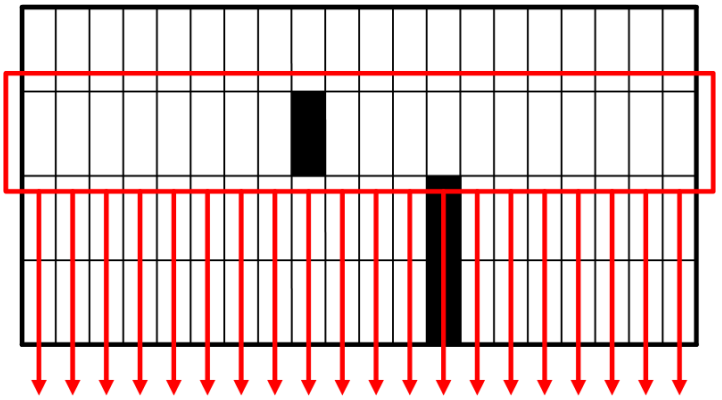

$P_D = P_{D,circ} + P_{D,pad}$ ('0' → '1' for 1 column)

$$P_{D,measured} \approx DCR \cdot t_{obs} \cdot n_{rep} \cdot 430 \cdot (P_{D,circ} + P_{D,pad})$$

- $P_{D,pad}$=295 µW/MHz (datasheet foundry)
- $P_{D,cir}$=8 µW/MHz (calculated), 10 µW/MHz (simulated)
- $P_{D,TOTAL}$(1.2 V)=4 mW (circuits) + 133 mW (pads) → **LVDS pad**

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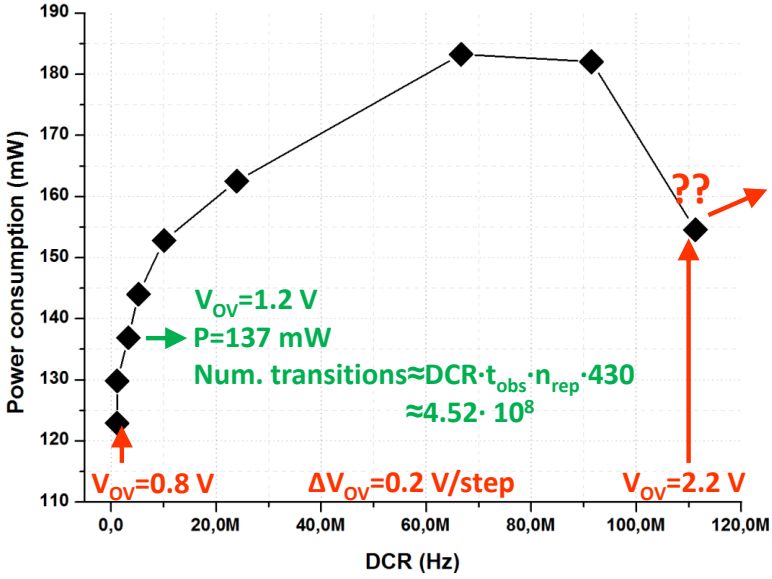
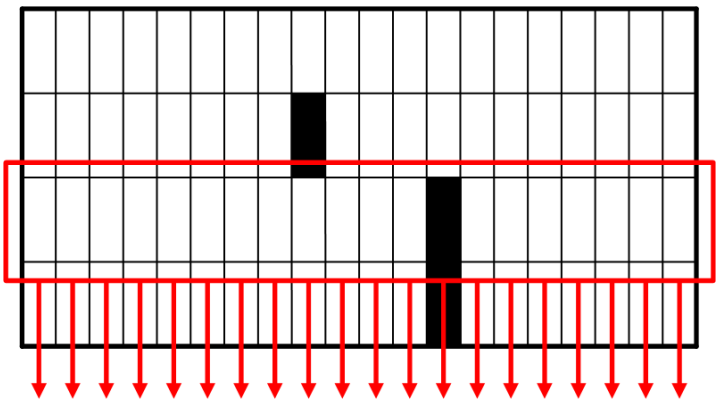
  - t_{obs}=4 ns, t_{off}=1 µs, n_{rep}=100 Mframes (t_m=0.4 s)





$P_D = P_{D,circ} + P_{D,pad}$ ('0' → '1' for 1 column)

$$P_{D,measured} \approx DCR \cdot t_{obs} \cdot n_{rep} \cdot 430 \cdot (P_{D,circ} + P_{D,pad})$$

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- $P_{D,cir}$=8 µW/MHz (calculated), 10 µW/MHz (simulated)
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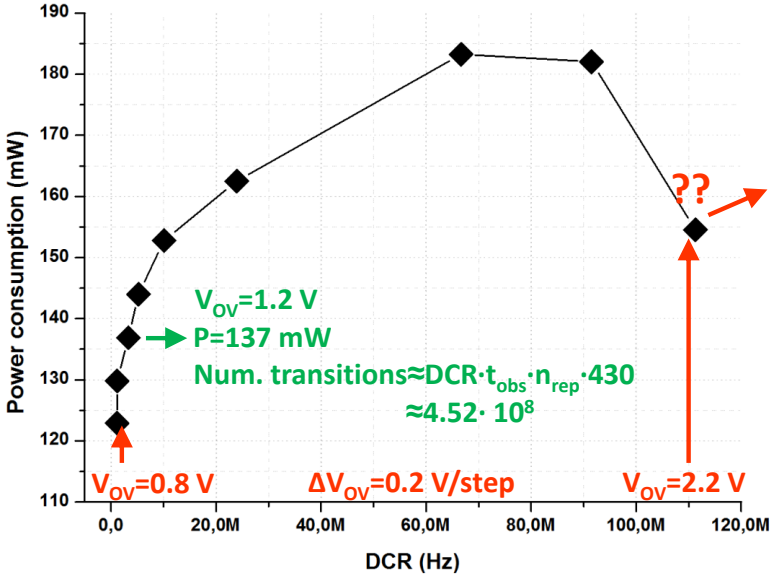
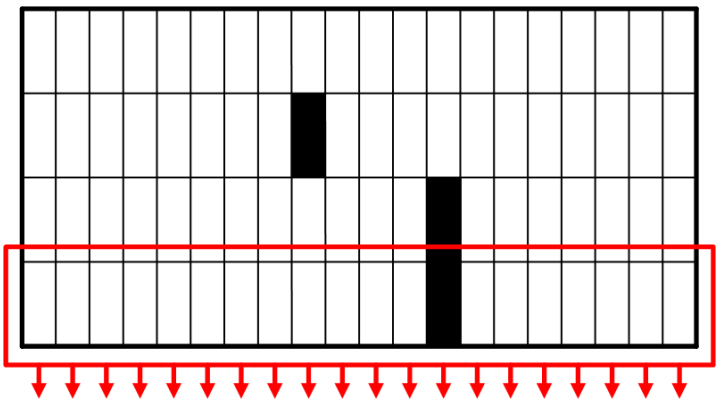
  - t_{obs}=4 ns, t_{off}=1 µs, n_{rep}=100 Mframes (t_m=0.4 s)



$$P_{D,measured} \approx DCR \cdot t_{obs} \cdot n_{rep} \cdot 430 \cdot (P_{D,circ} + P_{D,pad})$$



$P_D = P_{D,circ} + P_{D,pad}$ ('1' → '1' for 1 column)

$P_{D,TOTAL}$

- $P_{D,pad}$=295 µW/MHz (datasheet foundry)
- $P_{D,cir}$=8 µW/MHz (calculated), 10 µW/MHz (simulated)
- $P_{D,TOTAL}$(1.2 V)=4 mW (circuits) + 133 mW (pads) → **LVDS pad**

Time-gated GAPD pixel array. Characterization.

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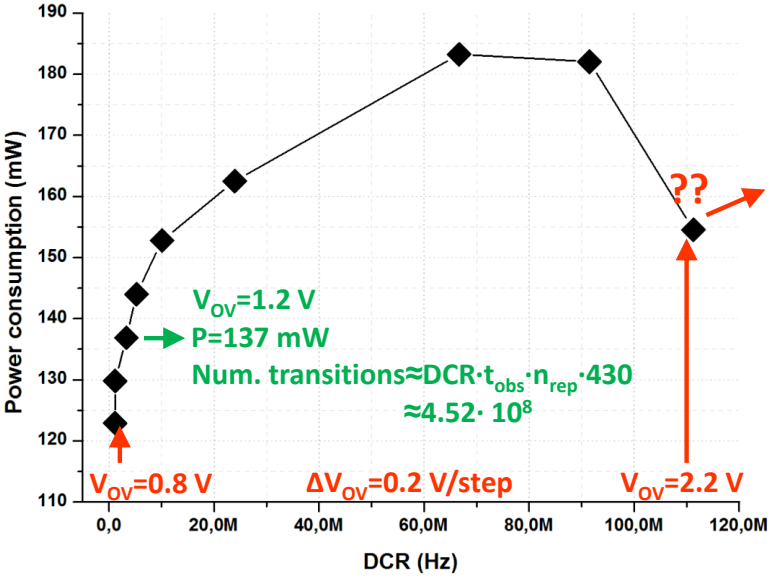
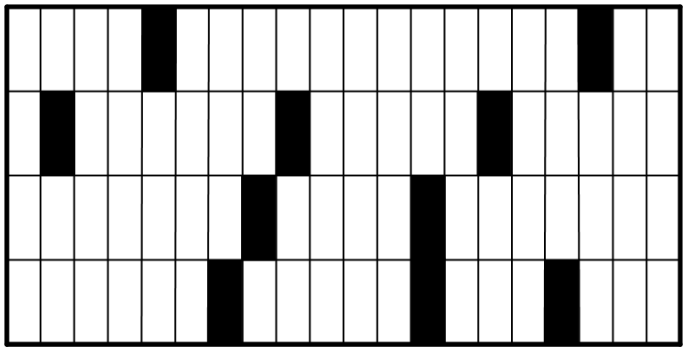
  - P_D is caused by the readout circuits and the output pads of the chip

  P(DCR), the DCR indicates the frequency of operation **GAPD array biased at V_{OV} ↑**

  - t_{obs}=4 ns, t_{off}=1 µs, n_{rep}=100 Mframes (t_m=0.4 s)





$$P_{D,measured} \approx DCR \cdot t_{obs} \cdot n_{rep} \cdot 430 \cdot (P_{D,circ} + P_{D,pad})$$

P_D=$P_{D,circ}$ ↑ + $P_{D,pad}$ ↑ (more dc → more transitions)

$P_{D,TOTAL}$ ↑

- $P_{D,pad}$=295 µW/MHz (datasheet foundry)
- $P_{D,cir}$=8 µW/MHz (calculated), 10 µW/MHz (simulated)
- $P_{D,TOTAL}$(1.2 V)=4 mW (circuits) + 133 mW (pads) → **LVDS pad**

Time-gated GAPD pixel array. Characterization.

- **Power consumption**

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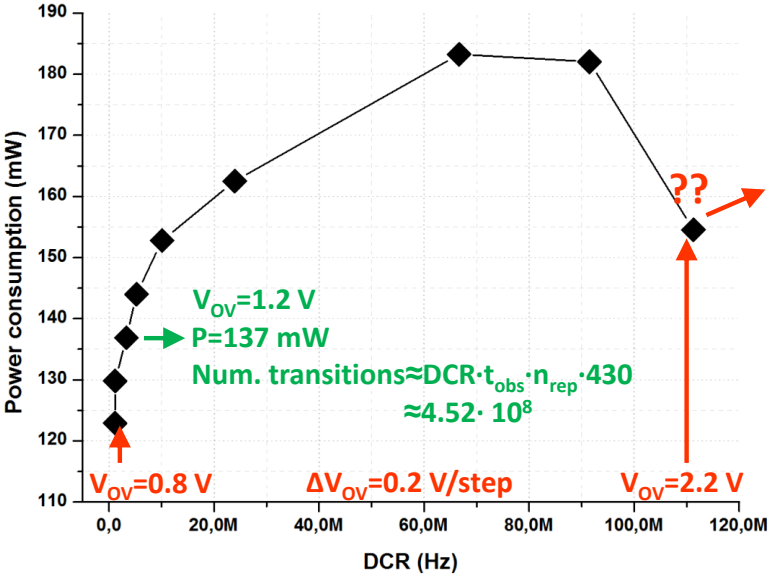
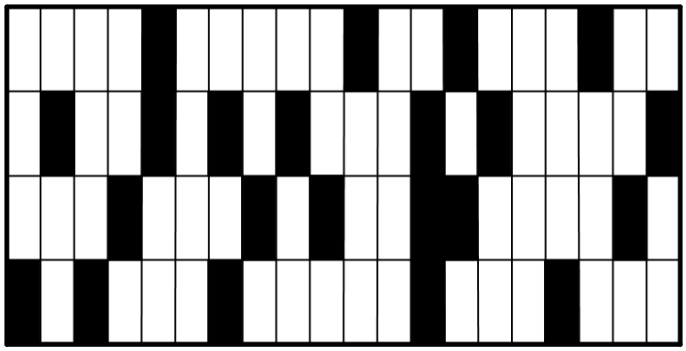
  - P_D is due to a change of state → $P_D = C_L \cdot V_{DD}^2 \cdot f$
  - P_D is caused by the readout circuits and the output pads of the chip

  P(DCR), the DCR indicates the frequency of operation

  GAPD array biased at V_{OV} ↑↑

  - t_{obs}=4 ns, t_{off}=1 µs, n_{rep}=100 Mframes (t_m=0.4 s)





$$P_{D,measured} \approx DCR \cdot t_{obs} \cdot n_{rep} \cdot 430 \cdot (P_{D,circ} + P_{D,pad})$$

P_D=$P_{D,circ}$ ↑↑ + $P_{D,pad}$ ↑↑ (more dc → more transitions)

$P_{D,TOTAL}$ ↑↑

- $P_{D,pad}$=295 µW/MHz (datasheet foundry)
- $P_{D,cir}$=8 µW/MHz (calculated), 10 µW/MHz (simulated)
- $P_{D,TOTAL}$(1.2 V)=4 mW (circuits) + 133 mW (pads) → **LVDS pad**

Time-gated GAPD pixel array. Characterization.

- **Power consumption**

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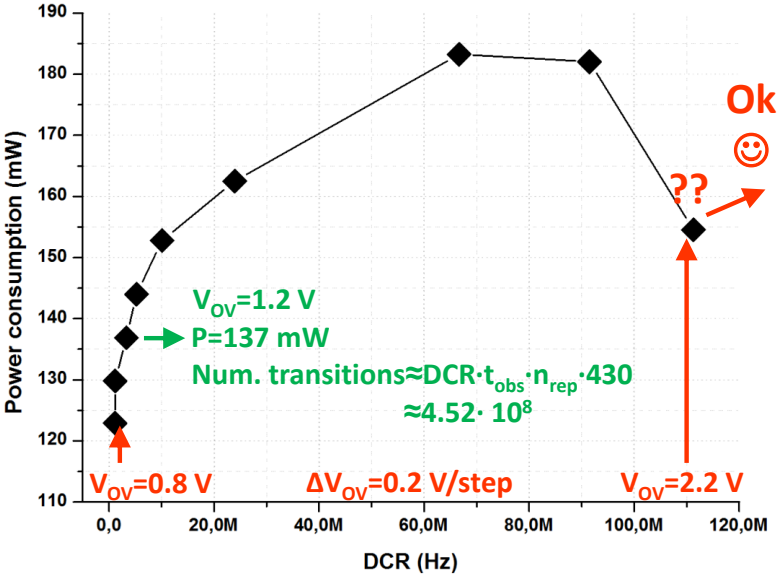
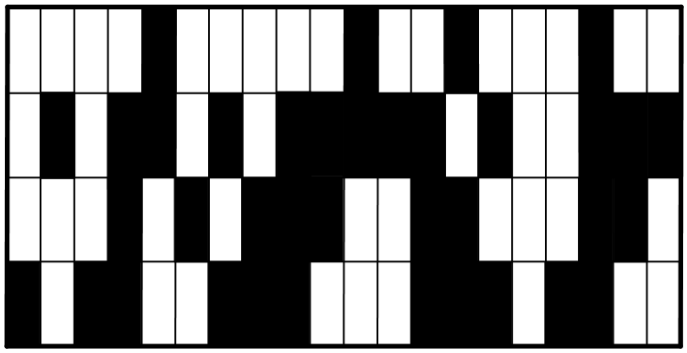
  - P_D is caused by the readout circuits and the output pads of the chip

  P(DCR), the DCR indicates the frequency of operation **GAPD array biased at V_{OV} ↑↑↑↑**

  - t_{obs}=4 ns, t_{off}=1 µs, n_{rep}=100 Mframes (t_m=0.4 s)



$$P_{D,measured} \approx DCR \cdot t_{obs} \cdot n_{rep} \cdot 430 \cdot (P_{D,circ} + P_{D,pad})$$



$P_D = P_{D,circ}$ ↑↑ + $P_{D,pad}$ ↓↓ (more dc → less transitions)

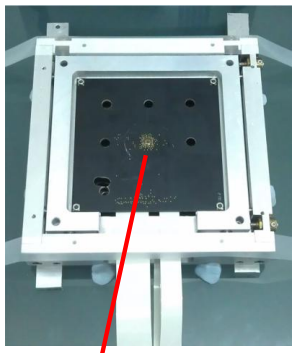
$P_{D,TOTAL}$ ↓↓

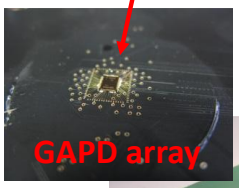
- $P_{D,pad}$=295 µW/MHz (datasheet foundry)
- $P_{D,cir}$=8 µW/MHz (calculated), 10 µW/MHz (simulated)
- $P_{D,TOTAL}$(1.2 V)=4 mW (circuits) + 133 mW (pads) → **LVDS pad**

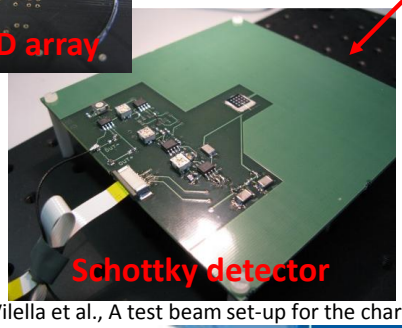
Time-gated GAPD pixel array. Characterization.

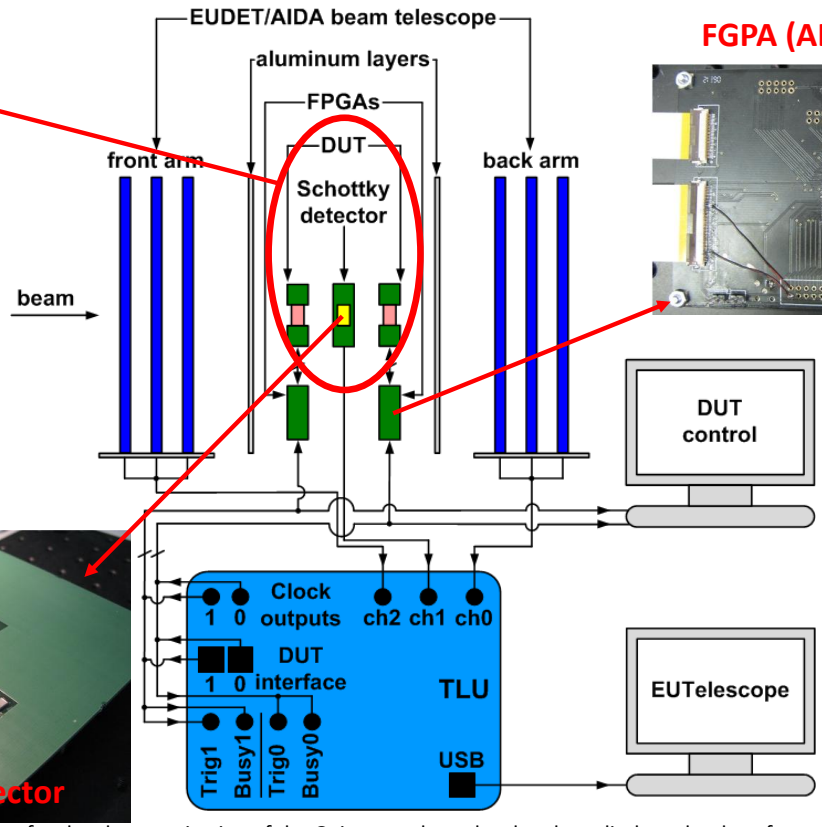
- **Series of beam-tests at CERN with a 120 GeV pion beam**

The mechanics

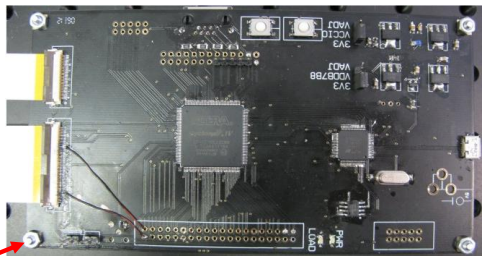








FGPA (ALTERA Cyclone IV)



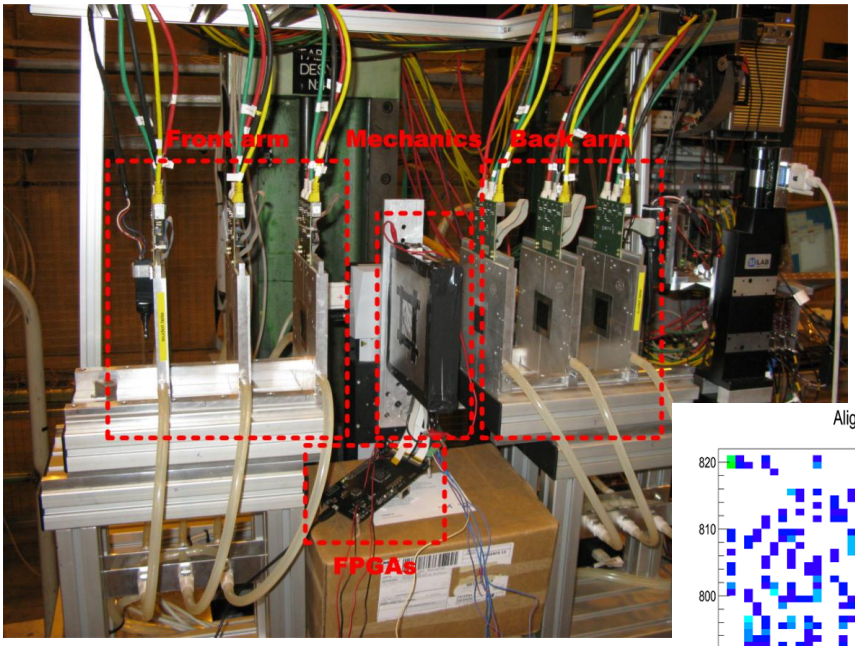
Special features to <u>avoid multiscattering</u>:

- Wafer of 250 µm
- No chip package
- PCB drilled under chip

E. Vilella et al., A test beam set-up for the characterization of the Geiger-mode avalanche photodiode technology for particle tracking, NIM A 694, 2012.

Time-gated GAPD pixel array. Characterization.

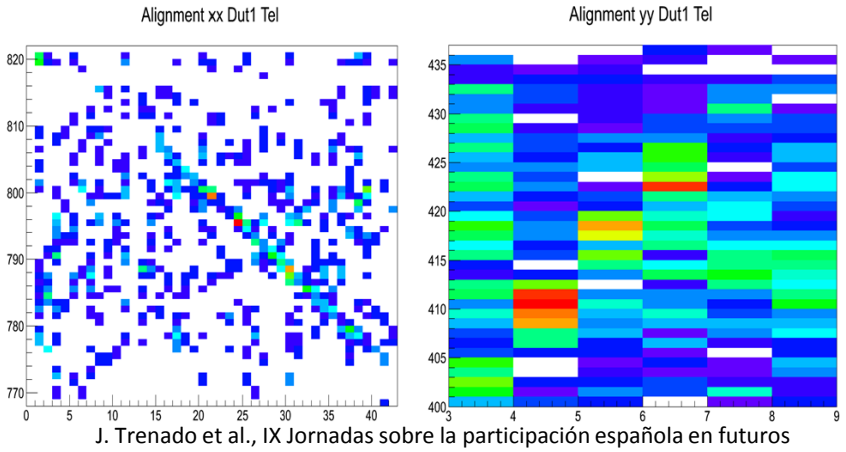
- **Series of beam-tests at CERN with a 120 GeV pion beam**



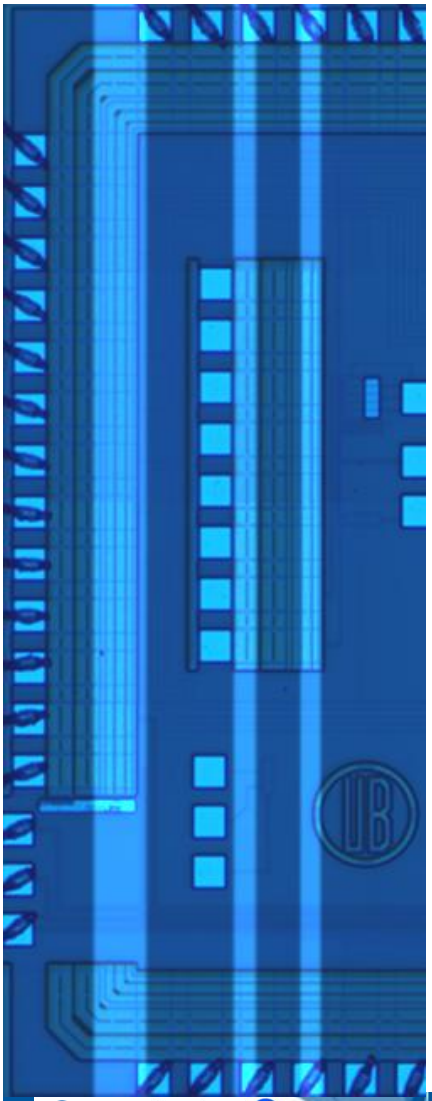
GAPD array

- V_{OV}=1.2 V
- t_{obs}=30 ns
- t_{off}=1.75 µs

Correlation between the GAPD detector array and the EUDET/AIDA beam telescope



J. Trenado et al., IX Jornadas sobre la participación española en futuros aceleradores lineales, 2012.



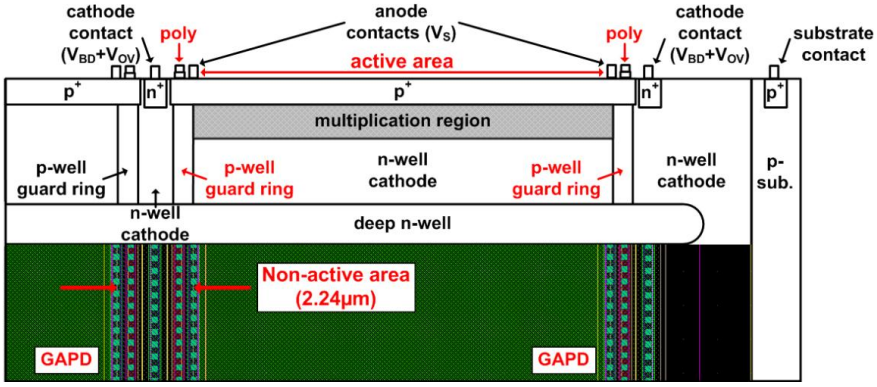
➢Outline

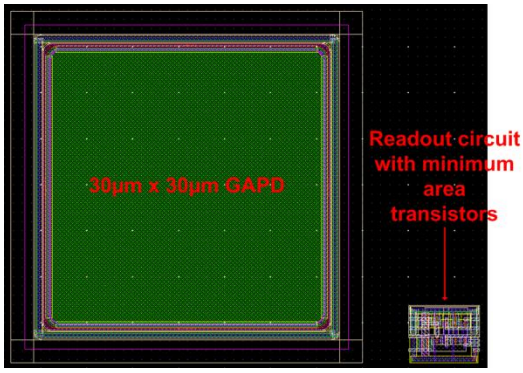
1. Potential applications
   - Future linear lepton colliders
   - Detector systems in ILC/CLIC
2. GAPDs in CMOS technologies
   - Principle of operation and figures of merit
   - State-of-the-art
   - Front-end electronics
3. Large arrays in a HV-CMOS process
   - Design and characterization
4. **Large arrays in a 3D process**
   - Design

Conclusion

Time-gated GAPD array in a 3D process. Design.

- A 100% FF is required by ILC/CLIC on detector systems
- GAPD detectors present dead areas due to
  - Guard-ring to prevent the premature edge breakdown
  - Additional masks to block the STI (technologies <0.250 µm)
  - Monolithically integrated readout circuit



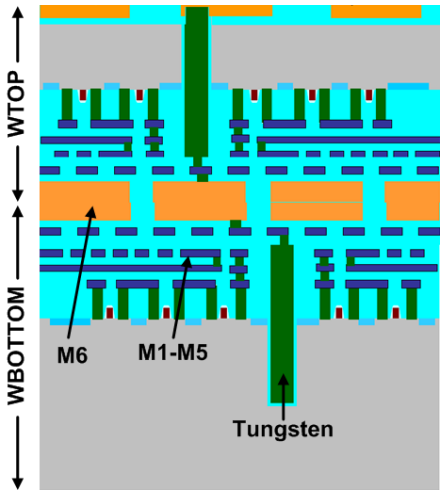


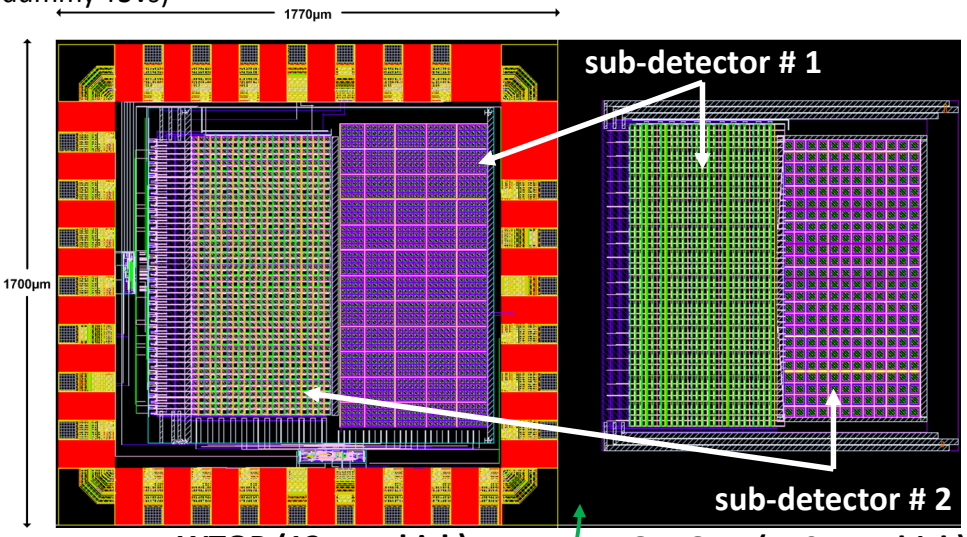
- As a result, GAPD detectors present a low FF (<10% in many cases!!)
- Time-gated GAPD pixel array (0.35 µm HV-AMS CMOS) → FF = 67%
  - Reduced number of in-pixel transistors
  - Sensors placed in the same n-well (minimum separation between pixels of 1.7 µm)
- 3D-IC technologies (Global Foundries 130 nm/Tezzaron 3D) are explored as a solution to overcome this limitation

Time-gated GAPD array in a 3D process. Design.

- **<u>3D vertical integration</u>:**
  - Fabricated by Global Foundries 130 nm and vertically integrated by Tezzaron
  - 2-layer stack of logic dies (no-DRAM option)
  - The 2 dies are bonded face-to-face (the designs need to be mirrored)
  - I/O pads are on the back side of WTOP
  - Via-first TSVs for connection between the logic circuitry and the I/O pads
  - Recommended TSV pitch → 100 µm (dummy TSVs)

- **<u>Main features of our design</u>:**
  - 48 rows x 48 columns
  - 2-different sub-detectors with the same pixel (different sensor area) but different implementations
    - Sub-detector # 1 (48 rows x 24 columns, **FF=66%**)
    - Sub-detector # 2 (48 rows x 24 columns, **FF=92%**)
  - Total area of 1770 µm x 1770 µm





Time-gated GAPD array in a 3D process. Design.

- **<u>Sub-detector # 1</u>:**

  - Cluster of 1 pixel. For each cluster:
    - WBOTTOM (T1) → readout electronics
    - WTOP (T2) → sensors (18 µm x 18 µm)
  - Interconnection between layers → from each GAPD to its readout circuit
  - **FF=66%**

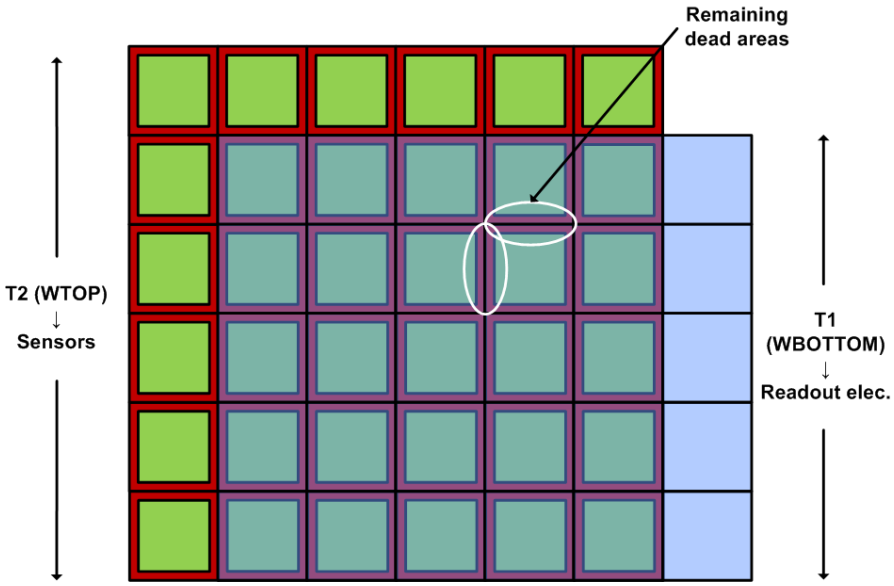
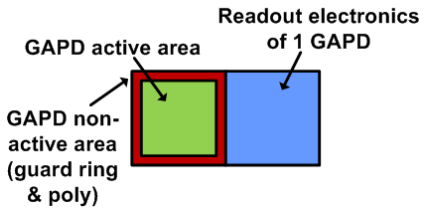
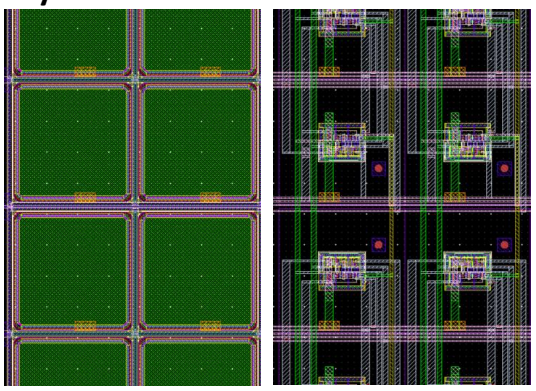


Figure legend:



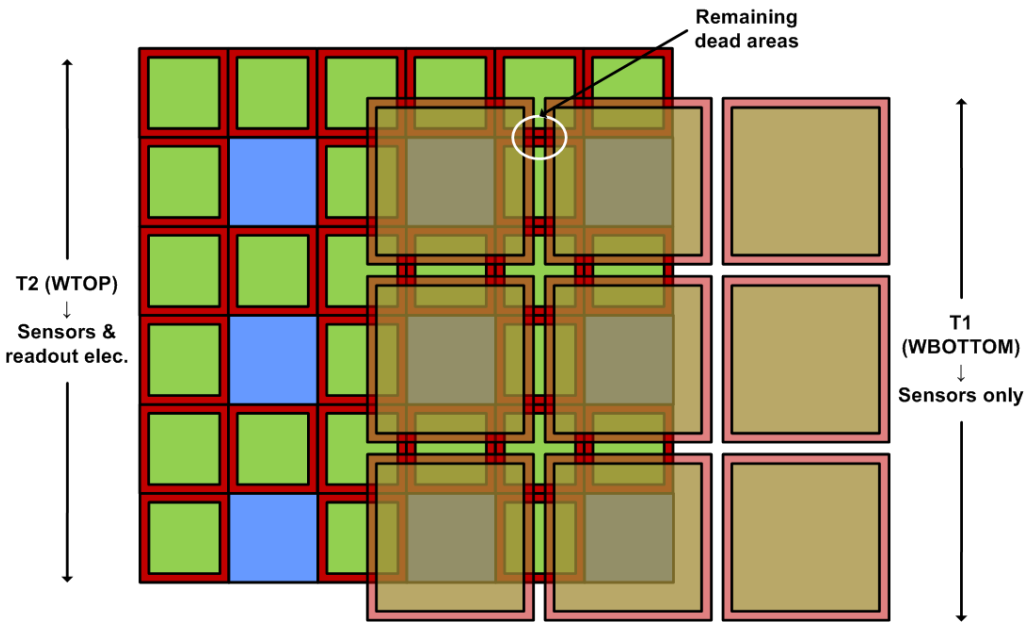
Layout zoom

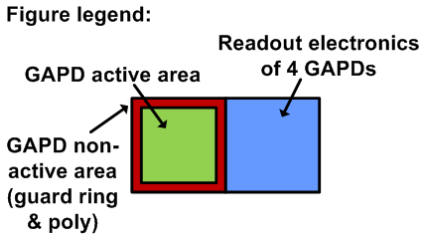


WTOP (T2) **WBOTTOM (T1)**

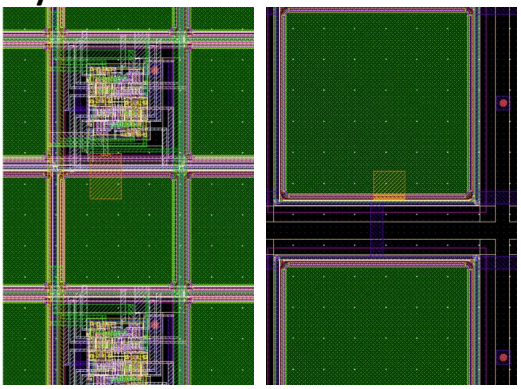
Time-gated GAPD array in a 3D process. Design.

- **<u>Sub-detector # 2</u>:**
  - Cluster of 4 pixels. For each cluster:
    - WBOTTOM (T1) → 1 sensor (30 µm x 30 µm)
    - WTOP (T2) → 3 sensors (18 µm x 18 µm) and readout electronics of the 4 pixels
  - Interconnection between layers → from the 30 µm x 30 µm to its readout electronics
  - **FF=92%**



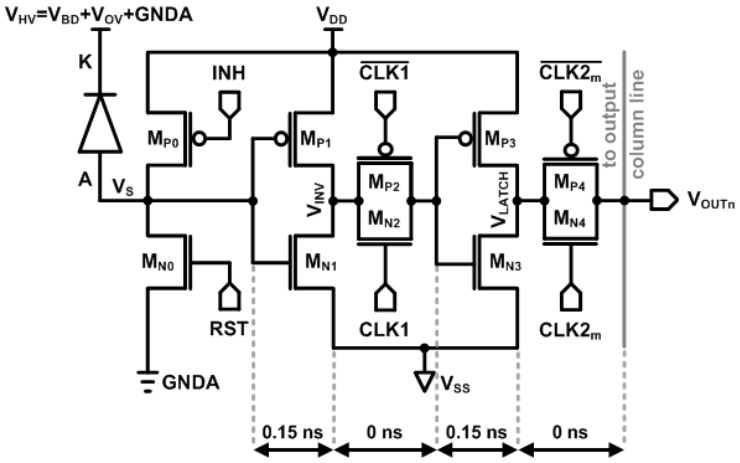


Layout zoom



WTOP (T2) **WBOTTOM (T1)**

Time-gated GAPD array in a 3D process. Design.



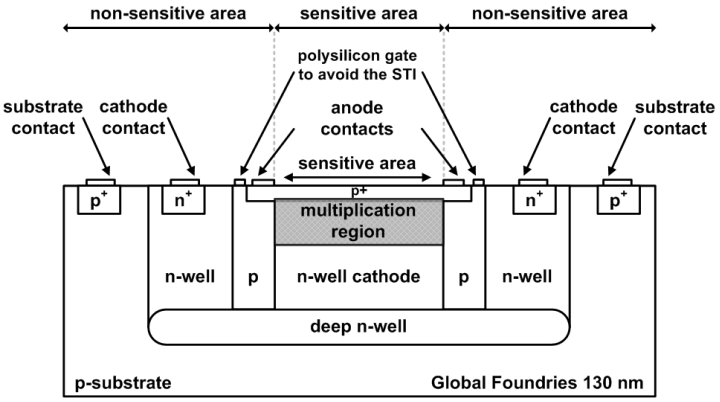
Pixel schematic

- GAPD + active INH and RST + 2G approach readout circuit
  - inverter with $V_{th}=V_{DD}/2$, V_{DD} =1.2 V
  - low V_{OV} to reduce the DCR
  - dynamic latch (1-bit memory cell) controlled by CLK1 to reduce the DCP
  - transmission-gate for sequential readout
  - digital output

- Δt (from V_S to V_{LATCH}) = 0.30 ns

GAPD design in a 130 nm process

- p^+ anode in an n-well cathode
- Surrounded by a low-doped p-well guard ring
- Deep n-well for full isolation with the p-substrate
- Polysilicon gate around the p^+ anode to avoid contact between the STI and the multiplication region for an acceptable DCR
- The separation between two consecutive GAPDs is filled with n-well (minimum separation → 2.24 µm)
- Based on C. Niclass et al., IEEE J. Sel. Top. Quantum Electron., 2007



Time-gated GAPD array in a 3D process. Design.

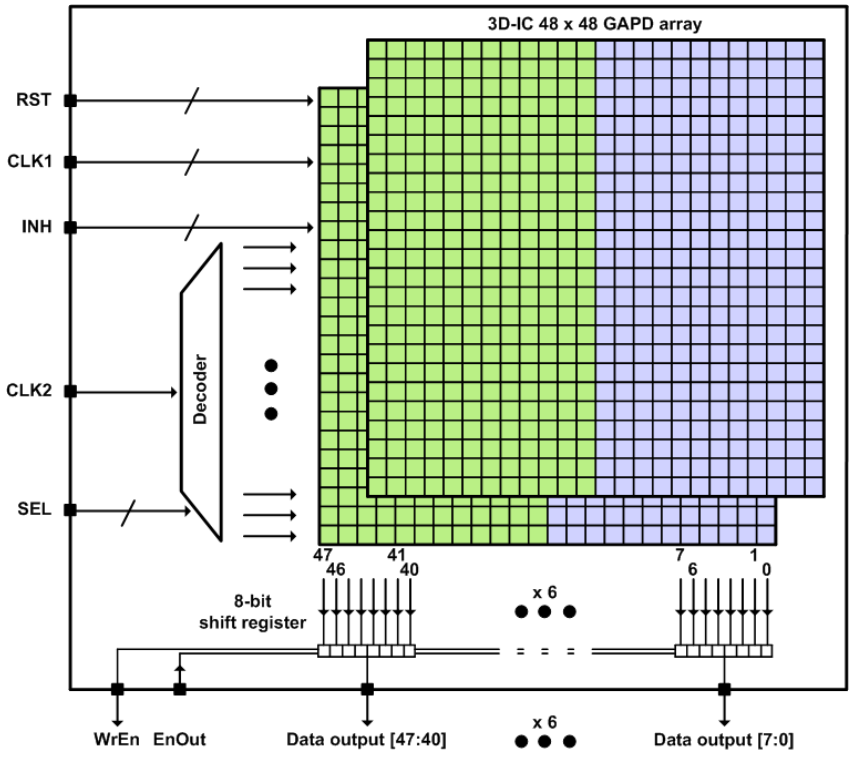
- **Chip:**

  - Pixel control signals:
  - INH, RST (time-gated sensor)
  - CLK1 (time-gated readout circuit)
  - $CLK2_m$ (readout)

  - Readout:
  - Sequential by rows during gated-off periods
  - Sequentially activating $CLK2_m$, with m=[1,48]
  - $CLK2_m$ → 1 input pin + 1 decoder (SEL) with 48 outputs

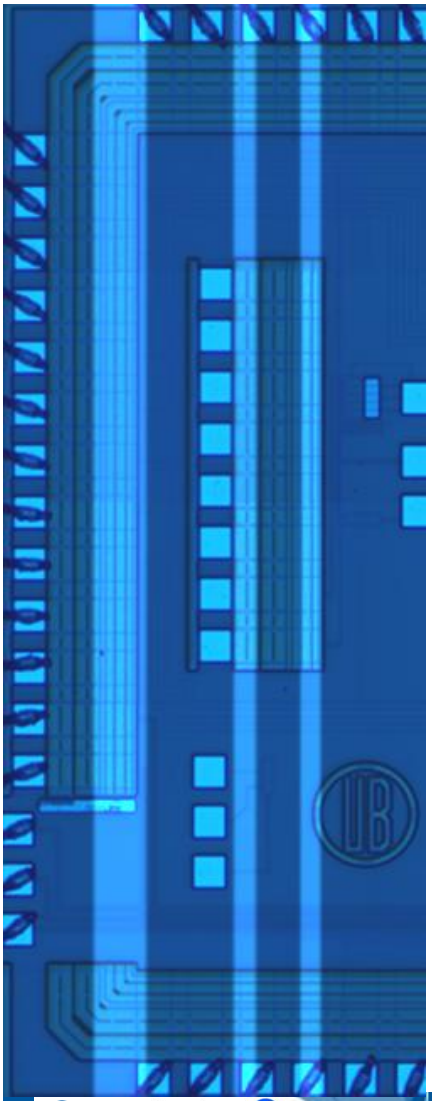
  - Pads:
  - 6 output pads + 5 control signal pads (RST, INH, CLK1, CLK2) + SEL + WrEn + EnOut + power supply pads
  - 6 8-bit shift-registers

  - Δt to read the whole detector ≈ 400 ns



- The detector has not been submitted for fabrication due to the delays in the MPW runs of this technology

E. Vilella et al., 3D integration of Geiger-mode avalanche photodiodes aimed to very high fill-factor pixels for future linear colliders", NIM A 731, 2013.



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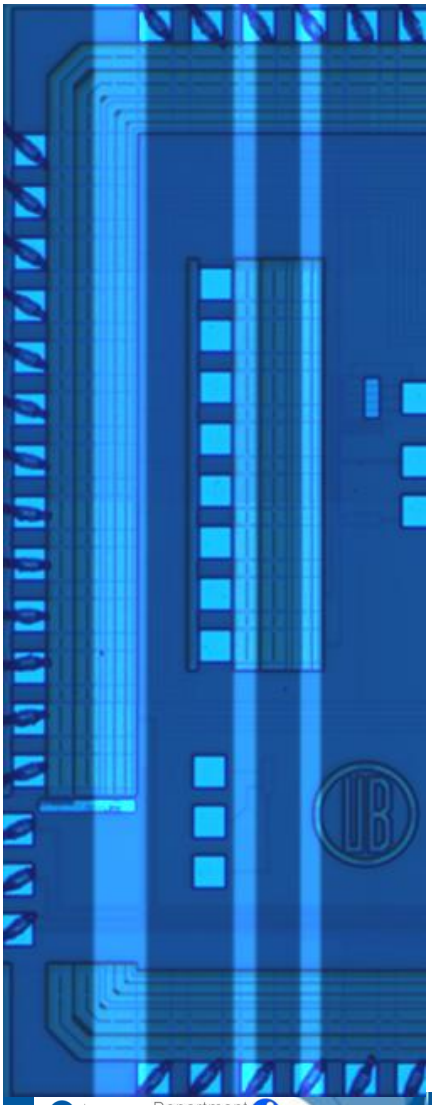
Conclusion

Summary

Category	Required	Achieved by GAPDs	Possible improvement
σ_{point} (pixel size)	<5 µm (17 µm)	5.77 µm (20 µm)	–
Material budget	0.15% X_0 (ILD) 0.30% X_0 (SiD)	0.25% X_0	–
Granularity	High	20 µm x 100 µm	–
Timing	Single BX resolution	Single BX resolution (ILC) Time integration (CLIC)	– Time stamping (CLIC)
Occupancy	<1 %, the noise counts (nc) generated by GAPDs should be below the background hits (bh)	$9 \cdot 10^{-7}$ bh/GAPD/BX (L2, FTD), 10^{-6} nc/GAPD/BX (ILC) $6 \cdot 10^{-6}$ bh/GAPD/train, $1{,}5 \cdot 10^{-3}$ nc/GAPD/train (CLIC)	– 2-input logic AND
Radiation tolerance	TID=1 kGy/year, NIEL=10^{11} n_{eq}/cm^2/year (ILC) TID=200 Gy/year, NIEL=10^{10} n_{eq}/cm^2/year (CLIC)	$9 \cdot 10^{-7}$ bh/GAPD/BX (L2, FTD), $4 \cdot 10^{-6}$ nc/GAPD/BX (ILC) $6 \cdot 10^{-6}$ bh/GAPD/train, $3 \cdot 10^{-3}$ nc/GAPD/train (CLIC)	– 2-input logic AND
Power	<a few mW/cm^2	High	LVDS pad
Fill-factor	100%	67% (90%)	3D technologies (to ≈100%)
EMI	Immunity	Yes	–
Cost	Affordable	Yes (MPW runs)	–

Conclusion

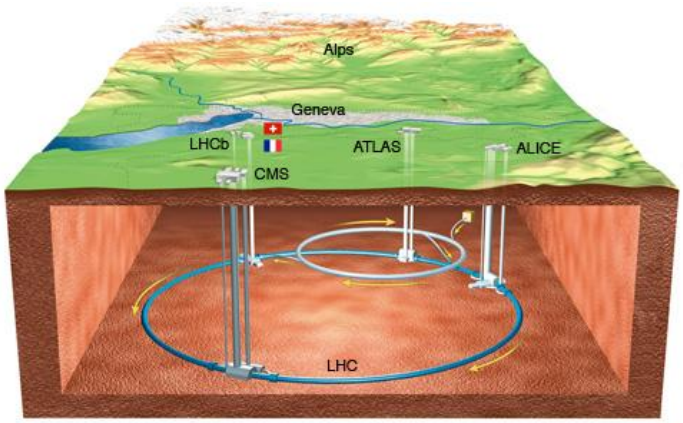
- To complement the discoveries made at LHC, a future linear lepton collider (ILC/CLIC) will be built
- Future linear colliders impose very extreme requirements on detector systems
- A prototype GAPD pixel detector aimed mostly at particle tracking at future linear colliders has been developed
- The two most ambitious requirements are the occupancy and the fill-factor:
- **Occupancy** → GAPD detector operated in a time-gated mode and at low V_{OV}
  - Design and characterization of 2 chips in a standard CMOS technology (0.35 µm HV-AMS)
  - APDs chip (Run 3) → Pixel array prototype with 10 x 43 pixels (67% FF)
  - Characterization →
    - reduction of the DCP (time-gated operation + low V_{OV} + low T)
    - avoidance of afterpulses
    - reduction of crosstalk
    - sensitivity to MIPs at beam-test
    - sensitivity to photons (400 nm - 1000 nm)
- **Fill-factor** → 3D technologies (vertical stacking of two layers of logic dies)
  - 3D APDs chip → Design of a GAPD prototype with a FF=92%

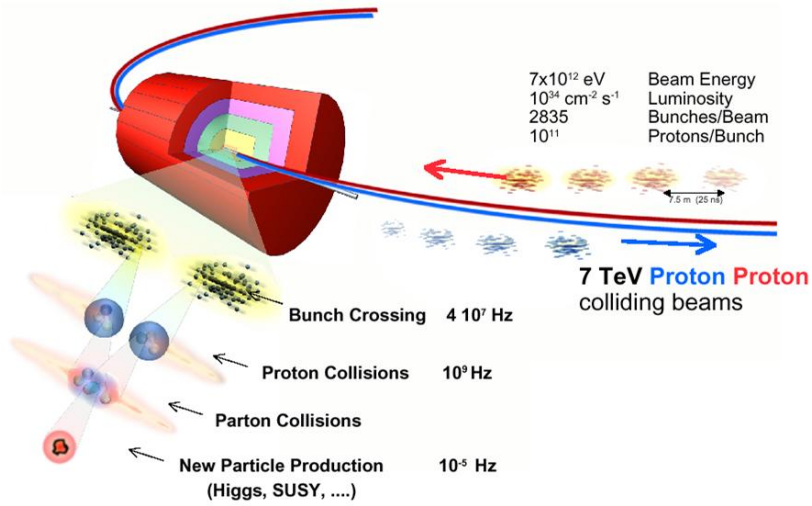


Back-up slides

HEP experiments. The present.

LHC (Large Hadron Collider)

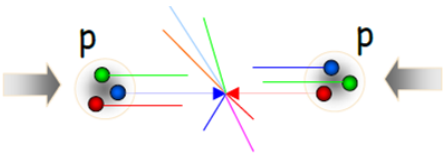




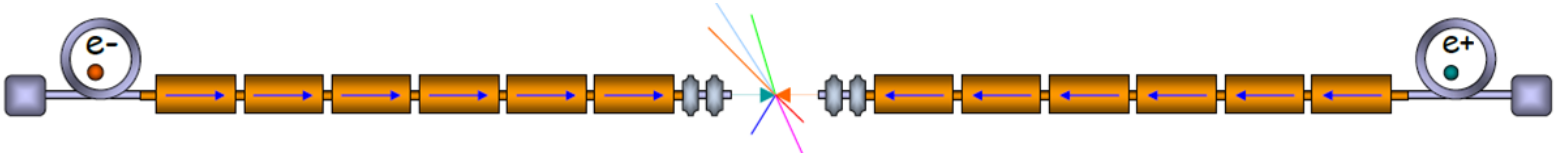
- Synchrotron hadron-hadron collider
- 27 km ring buried underground
- Two beams of hadrons are accelerated in opposite directions
- Energy → 7 TeV per beam (maximum)
- The two beams are made to collide at the detector area (ATLAS, CMS, ALICE and LHCb)
- Luminosity → $1 \cdot 10^{34}$ $cm^{-2}s^{-1}$
- Main discovery → Existence confirmation of the Higgs boson (2012)

HEP experiments. The future.

- Need to study the new particle in great detail
- This is not possible at LHC
  - Hadron-hadron collision (non-fundamental particles)
  - Broadband initial state

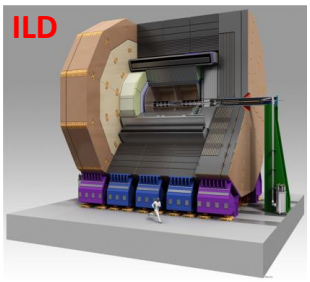


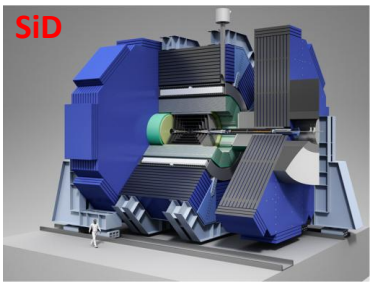
- **Post-LHC era**
- Lepton collider
  - Electron-positron collision (fundamental particles)
  - The energy of each particle is known → Precision measurements are possible
- A circular positron-electron collider is not an option
  - Energy losses due to synchrotron radiation → $\Delta E_{syn}[GeV] = \frac{K}{radius[km]} \cdot \left(\frac{E[GeV]}{m_0[GeV/c^2]}\right)^4$
  - Implies high energy compensations (not feasible)
  - Or severly increasing the radius of the ring (not feasible either)
- Next accelerator → Linear positron-electron collider



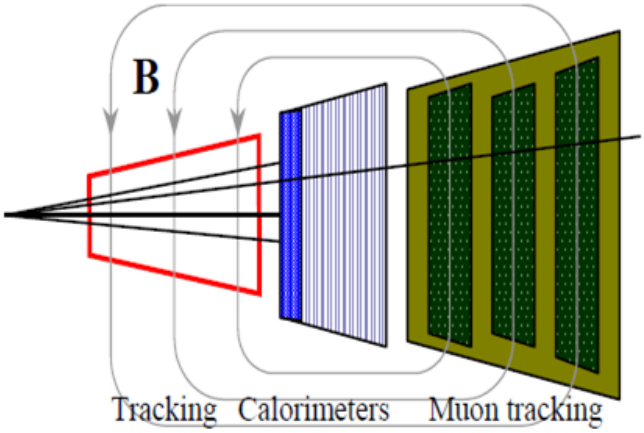
HEP experiments. Detector systems in ILC/CLIC.

- Detectors → To reconstruct the events generated right after the collisions
- Two validated detector proposals → (adopted by ILC and CLIC)





- **<u>General purpose detector</u>:**
  - To measure at several points the position of the particles generated, their momentum and energy



Disks to track down to small angles

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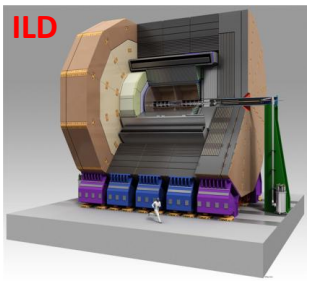
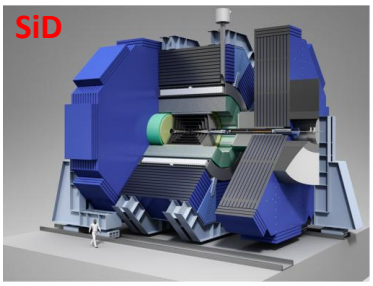




- **Subdetector arrangement (SiD):**

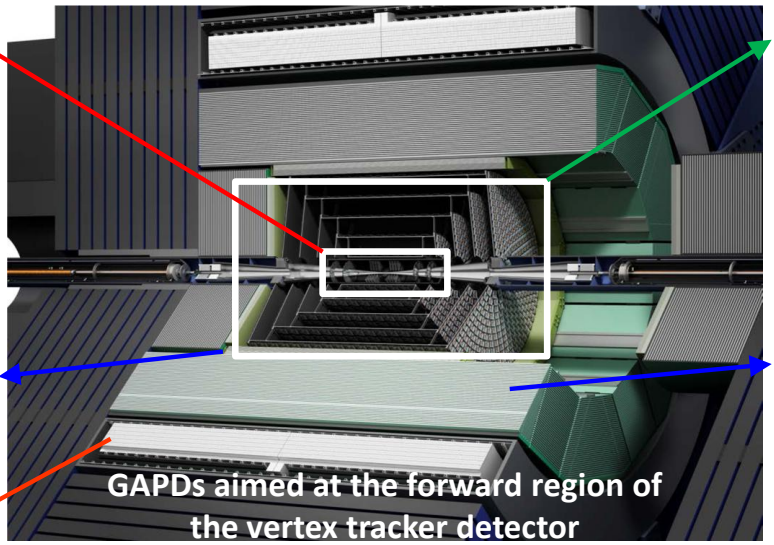
Vertex detector

- Multilayer barrel section **(5)**
- FW and BW disks **(4)**
- Disks **(3)**
- Si pixels
- To measure space points where particles are produced

Electromagnetic calorimetry

- Si pixels – W
- To measure particles energy

Solenoid – Magnet system (5T)



Tracker detector

- Barrel layers **(5)**
- Disks **(4)**
- Si strips [SiD]
- TPC + Si strips + Si pixels [ILD]
- To measure track curvature of charged particles and obtain their momentum

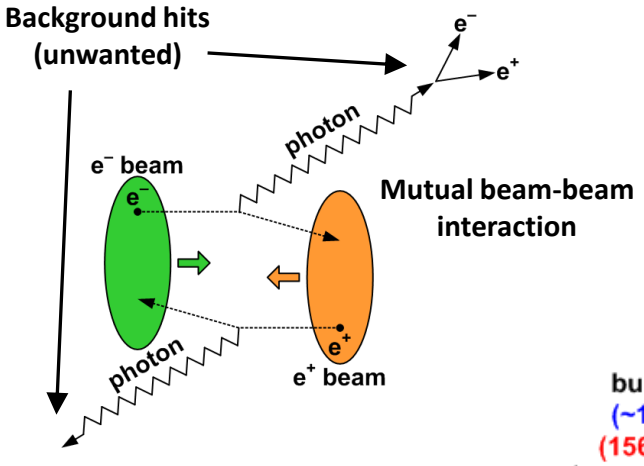
Hadronic calorimetry

- RPC steel
- To measure particles energy

Muon system – To identify isolated muons

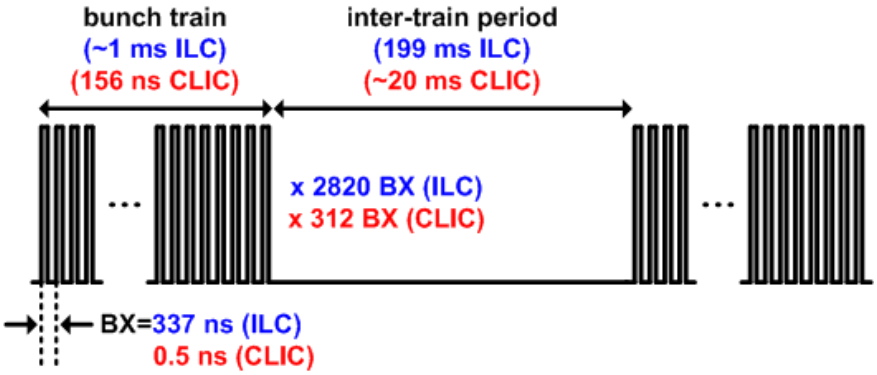
HEP experiments. Future linear lepton colliders.

- **Luminosity →** $L = n_b \cdot f_{rep} \cdot \frac{N^2}{4\pi\sigma_x\sigma_y} \cdot H_D$
- **H_D (enhancement factor)** → Beamstrahlung process



Beam parameter	ILC	CLIC
Energy (TeV)	1	3
L → Luminosity ($\cdot 10^{34}$ cm^{-2}s^{-1})	2.70	5.90
n_b → # Bunches/train	2820	312
f_{rep} → Train repetition rate (Hz)	5	50
Bunch separation (ns)	337	0.5
N^2 → # Particles/bunch ($\cdot 10^9$)	7.50	3.72
σ_x/σ_y → Beam size (nm/nm)	640/5.7	40/1

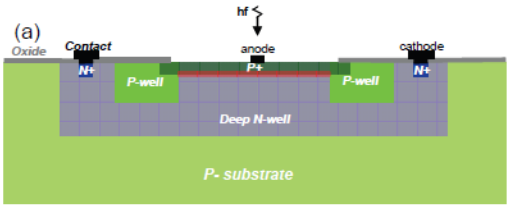
- **ILC/CLIC beam structure** → (drives timing requirements for detectors)



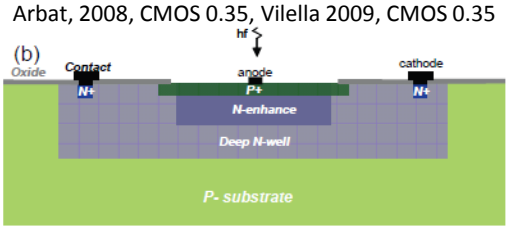
HEP experiments. Pair induced background hits in the subdetectors.

Technical Design Report, Volume 4 – Detectors (p. 282)

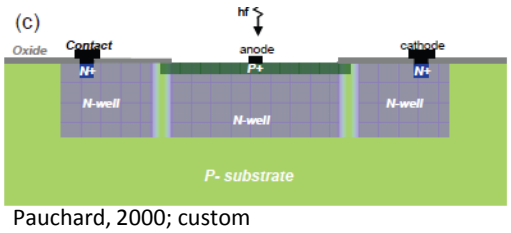
Sub-detector	Units	Layer	500 GeV	1000 GeV
VTX-DL	hits/cm^2/BX	1	6.320 ± 1.763	11.774 ± 0.992
		2	4.009 ± 1.176	7.479 ± 0.747
		3	0.250 ± 0.109	0.431 ± 0.128
		4	0.212 ± 0.094	0.360 ± 0.108
		5	0.048 ± 0.031	0.091 ± 0.044
		6	0.041 ± 0.026	0.082 ± 0.042
SIT	hits/cm^2/BX	1	0.0009 ± 0.0013	0.0016 ± 0.0016
		2	0.0002 ± 0.0003	0.0004 ± 0.0005
FTD	hits/cm^2/BX	1	0.072 ± 0.024	0.145 ± 0.024
		2	0.046 ± 0.017	0.102 ± 0.016
		3	0.025 ± 0.009	0.070 ± 0.009
		4	0.016 ± 0.005	0.046 ± 0.007
		5	0.011 ± 0.004	0.034 ± 0.005
		6	0.007 ± 0.004	0.024 ± 0.006
		7	0.006 ± 0.003	0.022 ± 0.006
SET	hits/BX	1	0.196 ± 0.924	0.588 ± 2.406
		2	0.239 ± 1.036	0.670 ± 2.616
TPC	hits/BX	-	216 ± 302	465 ± 356
ECAL	hits/BX	-	444 ± 118	1487 ± 166
HCAL	hits/BX	-	18049 ± 729	54507 ± 923



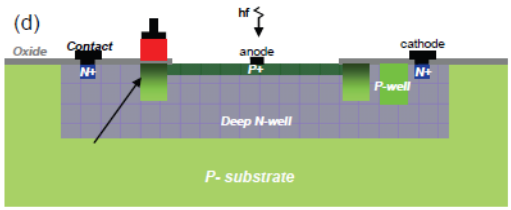
Goetzberger, 1963; Cova,1981; Kindt, 1994; custom
Rochas, 2002, CMOS 0.8; Niclass, 2007, CMOS 0.13;
Arbat, 2008, CMOS 0.35, Vilella 2009, CMOS 0.35



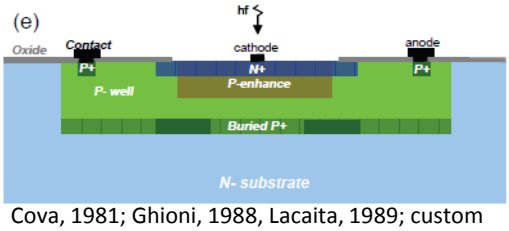
Petrillo, 1984; Ghioni, 1988, Lacaita, 1989, custom
Pancheri, 2007 CMOS 0.7



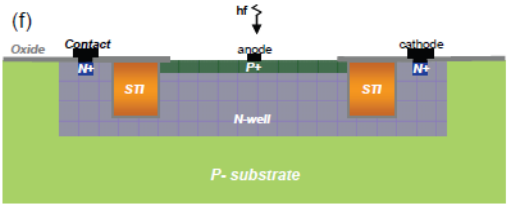
Pauchard, 2000; custom
Rochas, 2001, CMOS 0.8



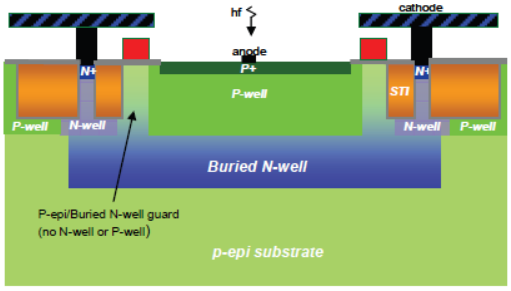
Rochas, 2003, CMOS 0.8; Xiao, 2007, CMOS 0.35



Cova, 1981; Ghioni, 1988, Lacaita, 1989; custom



Finkelstein , 2006,CMOS 0.18; Hsu, 2009, CMOS 0.18;
Niclass, 2007, CMOS 0.13; Gersback, 2008, CMOS 0.13,
Arbat, 2008, CMOS 0.13

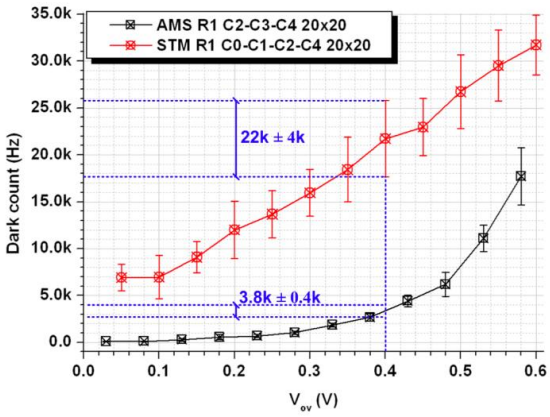


Richardson, 2009, CMOS 0.13, Webster, 2012, CMOS 0.09

G.F.Dalla Betta, “Avalanches in Photodiodes” Ed., InTech Pub. (2011)

First steps in GAPDs at the University of Barcelona.

- First steps in GAPDs at the Department of Electronics by *Dr. A. Arbat ("Towards a forward tracker detector based on Geiger mode avalanche photodiodes for future linear colliders", PhD, 2010)*.
- In the thesis of Dr. Arbat, 2 standard CMOS technologies for GAPDs aimed to particle tracking are explored:
  - 130 nm STMicroelectronics
  - 0.35 µm High Voltage AustriaMicroSystems
- Conclusion of Dr. Arbat's work:



0.35 µm HV-AMS presents a lower DCR due to its lower trap concentration

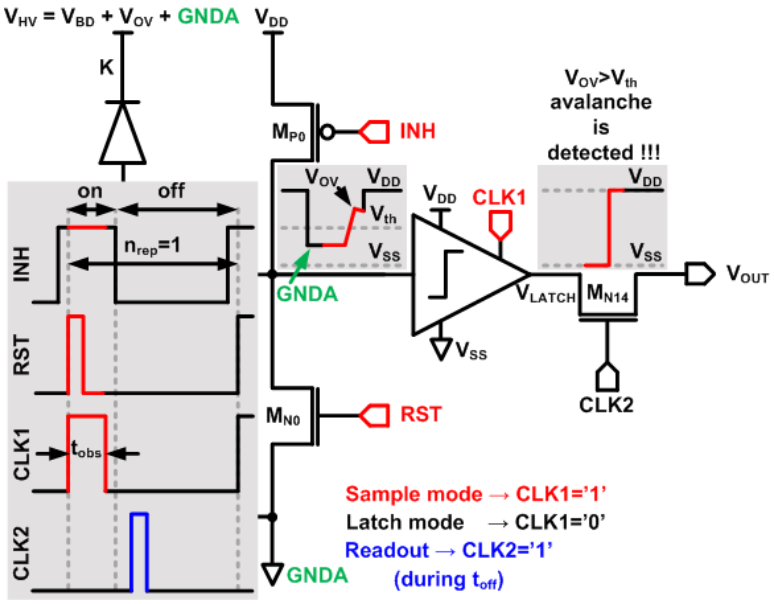
↓

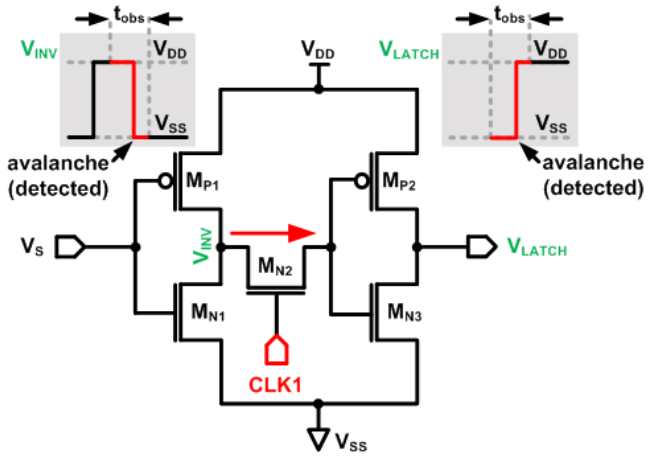
This technology was selected to develop a GAPD detector for particle tracking

- To continue the working line of Dr. Arbat, in E. Vilella's thesis:
  - Technology → 0.35 µm High Voltage AustriaMicroSystems
  - Sensor size → 20 µm x 100 µm
  - Sensor design → p^+ in an n-well (wafer is a p-substrate)

Single pixels with voltage-mode readout circuit. Design.

- Target → Voltage-mode readout circuit to operate the sensor at low V_{OV} and reduce the DCR
- Problem → Difficult to detect low V_{OV} with a small area readout circuit in HV-AMS 0.35 µm
- Decision → **Design of 3 pixels with a different readout circuit that overcomes this issue**
- All the pixels consist of - 1 voltage discriminator **(with $V_{th}=V_{DD}/2$, $V_{DD}=3.3$ V)**
  - 1-bit memory cell (time-gated synchronously with the sensor)
  - 1 pass-gate to activate the pixel readout
- 1-bit memory cell → Samples during gate-on and holds value during gate-off





A) 2-grounds (2G)

- Voltage discriminator → CMOS inverter with $V_{th}=V_{DD}/2$
- $V_{DD}=3.3$ V in this technology

Single pixels with voltage-mode readout circuit. Design.

- Target → Voltage-mode readout circuit to operate the sensor at low V_{OV} and reduce the DCR
- Problem → Difficult to detect low V_{OV} with a small area readout circuit in HV-AMS 0.35 µm
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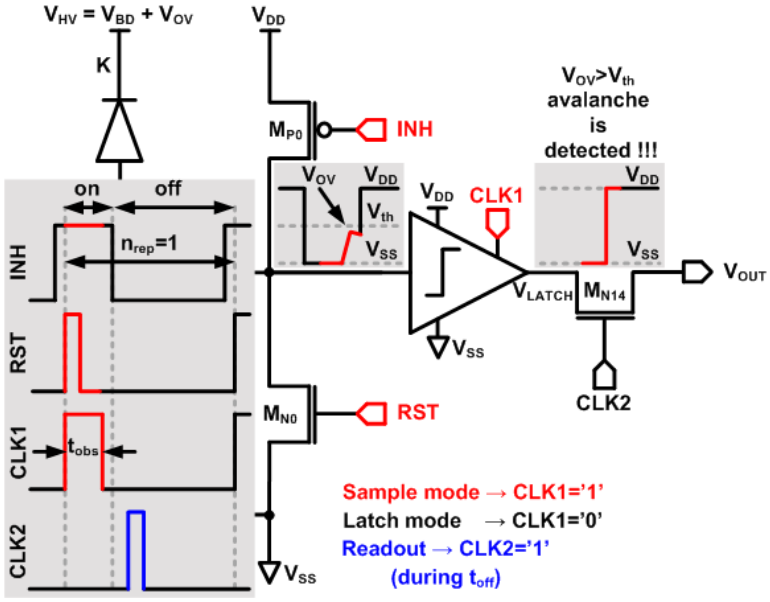
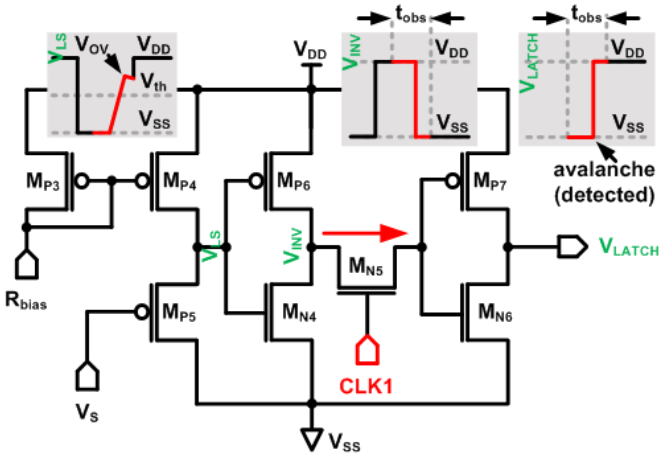
  - 1-bit memory cell (time-gated synchronously with the sensor)
  - 1 pass-gate to activate the pixel readout
- 1-bit memory cell → Samples during gate-on and holds value during gate-off



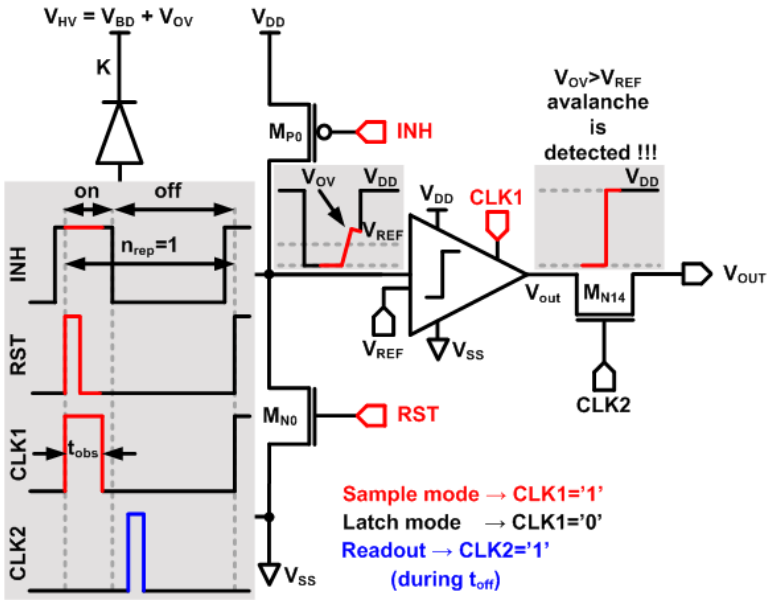


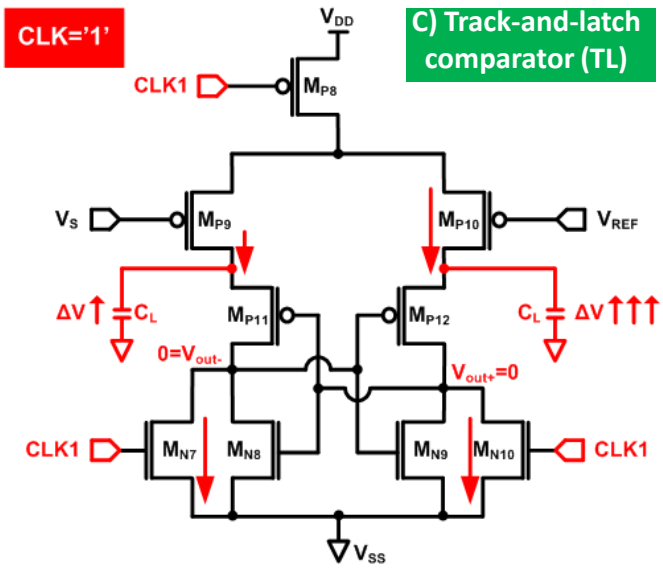
B) Level-shifter (LS)

- Voltage discriminator → CMOS inverter with $V_{th}=V_{DD}/2$
- $V_{DD}=3.3$ V in this technology

Single pixels with voltage-mode readout circuit. Design.

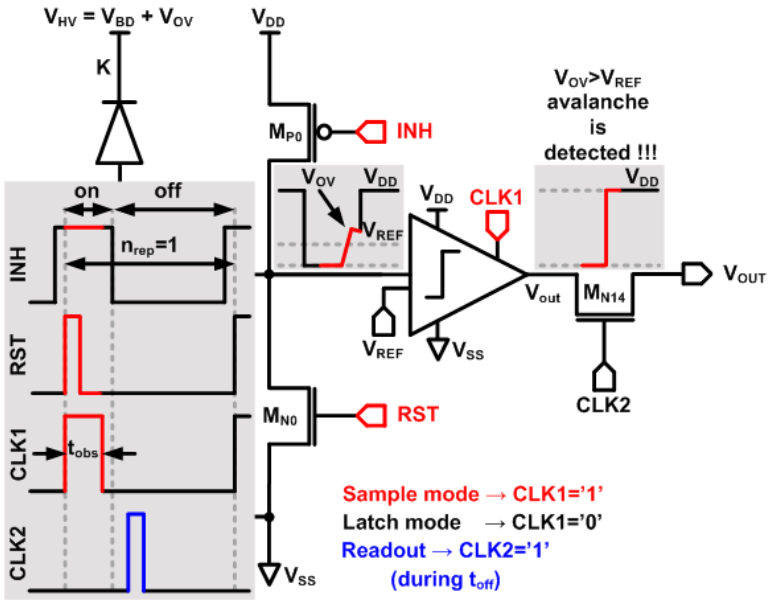
- Target → Voltage-mode readout circuit to operate the sensor at low V_{OV} and reduce the DCR
- Problem → Difficult to detect low V_{OV} with a small area readout circuit in HV-AMS 0.35 µm
- Decision → **Design of 3 pixels with a different readout circuit that overcomes this issue**
- All the pixels consist of - 1 voltage discriminator **(with V_{th} → V_{REF}, $0 \leq V_{REF} \leq 3.3$ V)**
  - 1-bit memory cell (time-gated synchronously with the sensor)
  - 1 pass-gate to activate the pixel readout
- 1-bit memory cell → Samples during gate-on and holds value during gate-off

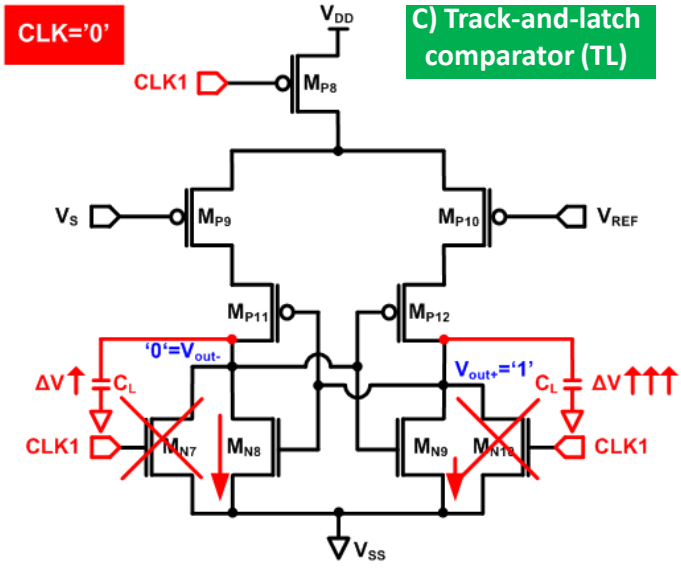




Single pixels with voltage-mode readout circuit. Design.

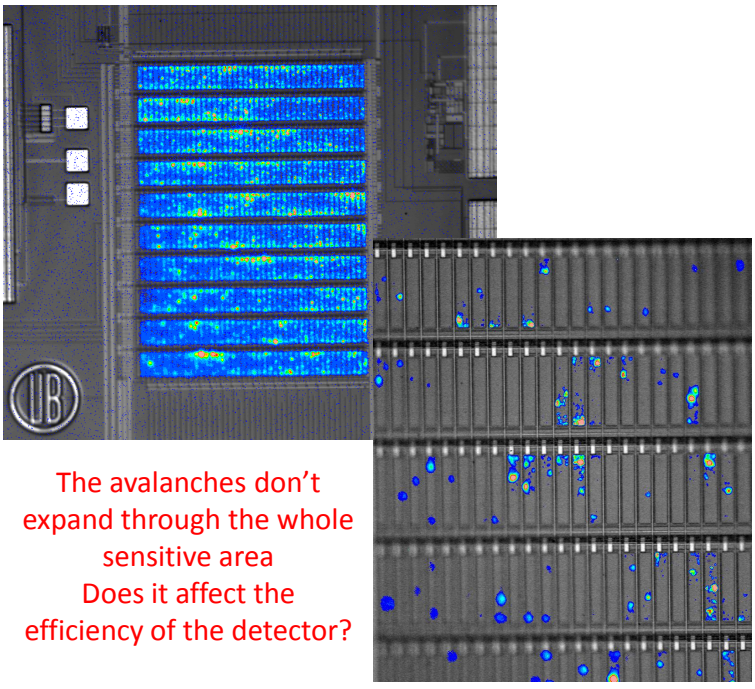
- Target → Voltage-mode readout circuit to operate the sensor at low V_{OV} and reduce the DCR
- Problem → Difficult to detect low V_{OV} with a small area readout circuit in HV-AMS 0.35 µm
- Decision → **Design of 3 pixels with a different readout circuit that overcomes this issue**
- All the pixels consist of - 1 voltage discriminator **(with V_{th} → V_{REF}, $0 \leq V_{REF} \leq 3.3$ V)**
  - 1-bit memory cell (time-gated synchronously with the sensor)
  - 1 pass-gate to activate the pixel readout
- 1-bit memory cell → Samples during gate-on and holds value during gate-off





Time-gated GAPD pixel array. Characterization.

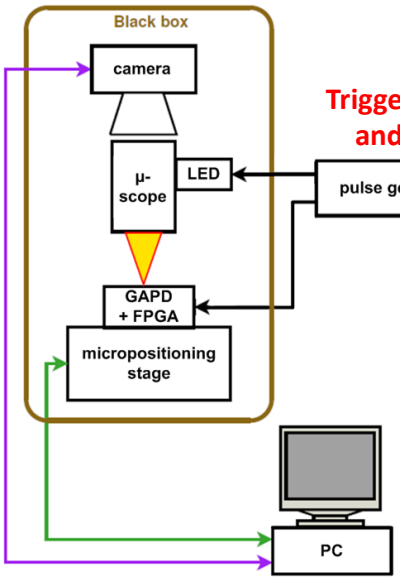
- **Photoemission**
  - An emission microscope (PHEMOS 1000) was used to localize the high field regions by detecting the emitted light during the avalanche process
  - Presence of non-uniformities across the array and also within single GAPDs



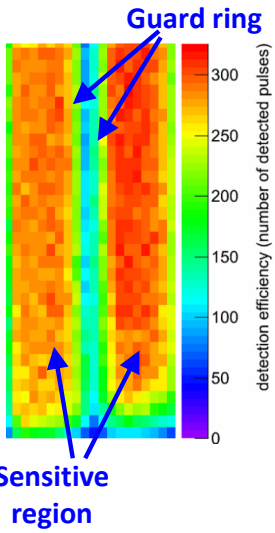
The avalanches don't expand through the whole sensitive area
Does it affect the efficiency of the detector?

- **Distribution of photon detection efficiency**
  - Set-up to scan a region of the array with a pulsed LED
  - LED resolution → 2 µm
  - LED λ → 625 nm
  - Shots per spot → 1 k
  - V_{OV}=3.1 V, t_{obs}=50 ns, t_{off}=5 ms (LED moves to next spot), n_{rep}=1 k

Set-up



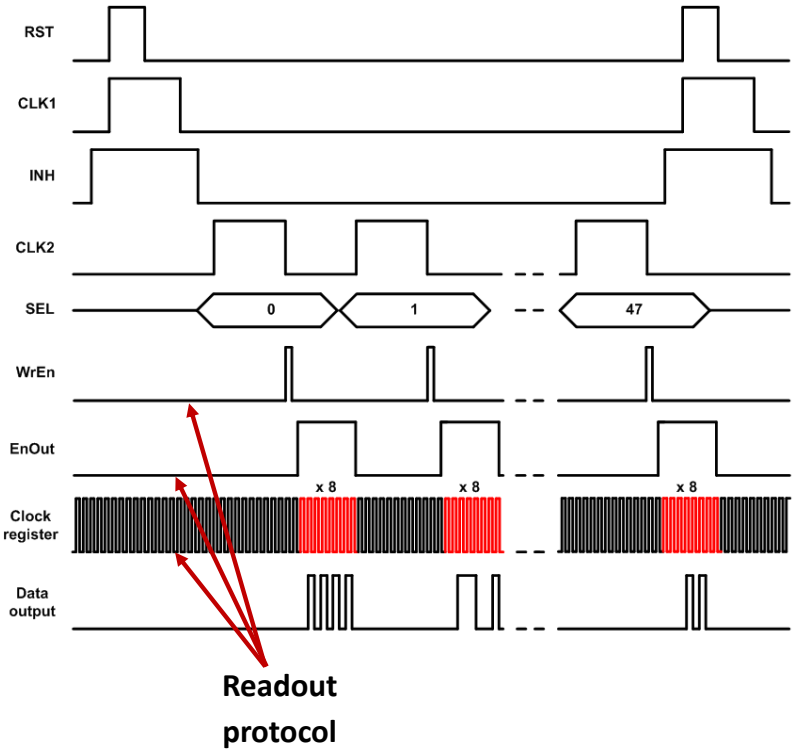
Result

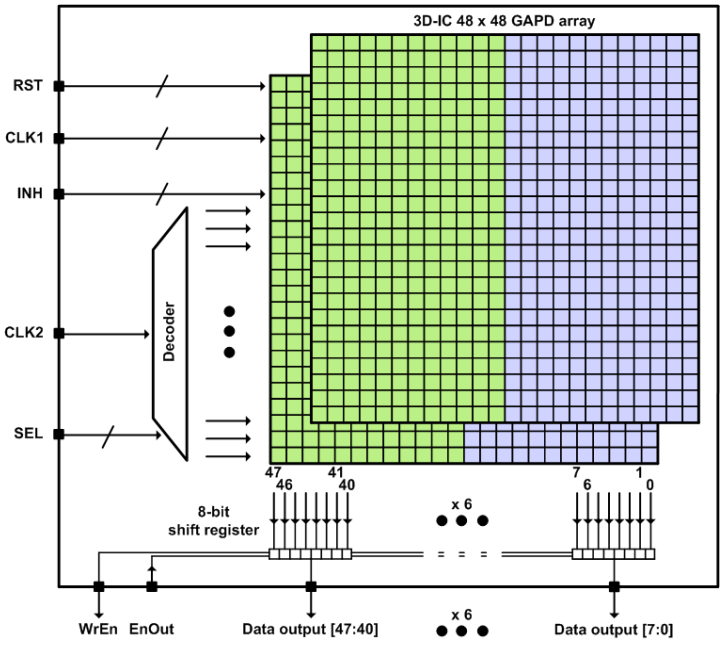


M. Tesař et al, Proc. Sci., 2012

Time-gated GAPD array in a 3D process. Design.

- **Sequential readout by rows during the gated-off periods**:

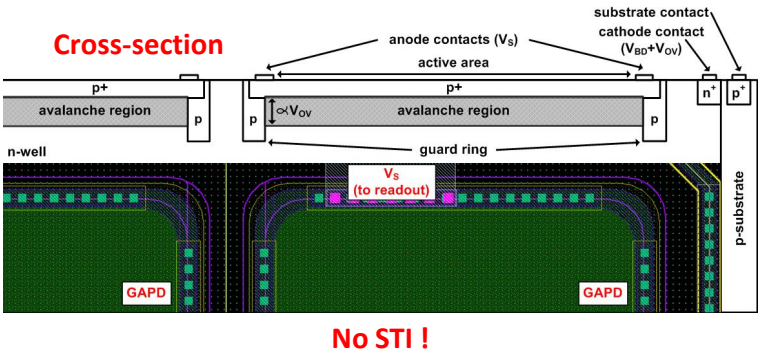




Alternative solutions.

- **Vertically integrated detector with 0.35 µm HV-AMS standard CMOS technology:**

In this particular technology, and with our structure, the guard ring is sensitive → ≈ 100% fill-factor seems feasible (*)



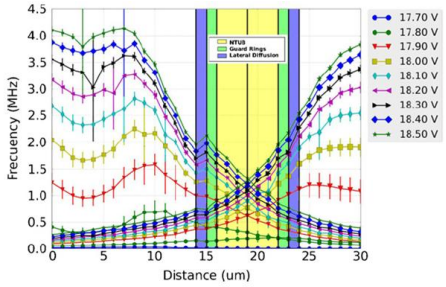
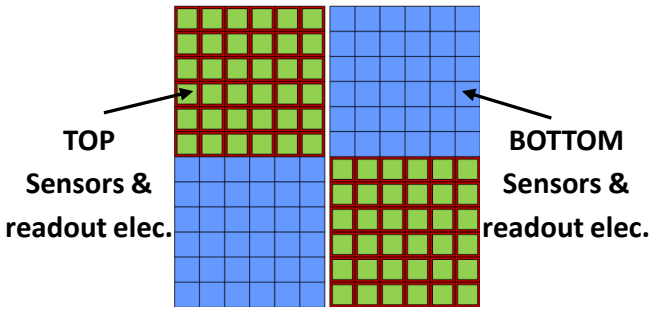
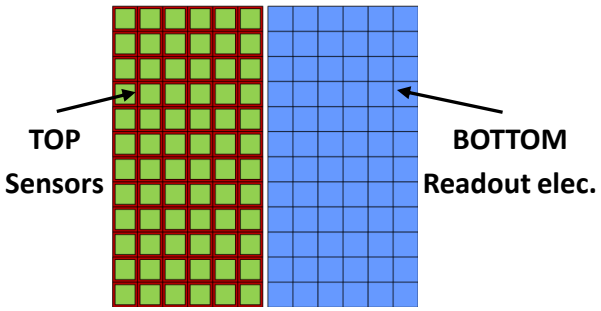


Fig. 16. Detection frequencies measured by scanning a 30 keV electron beam onto two neighbouring pixels in the array.



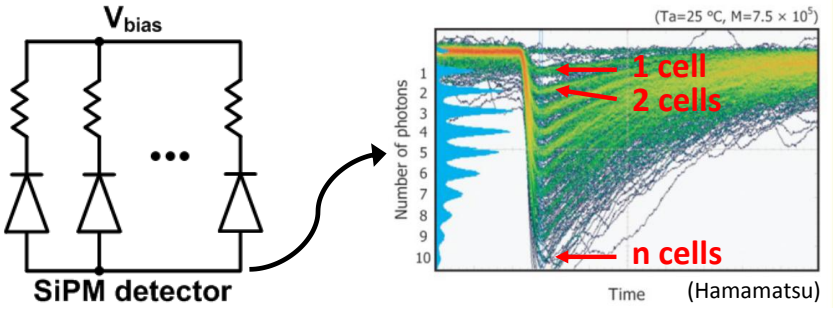


(*) A. Vilà, Characterization and simulation of avalanche photodiodes for next-generation colliders, Sens. Actuators A (2011).

Further improvements. Reduction of the threshold event in dSiPMs.

- The time-gated operation can be used to improve the performance of SiPMs
- **SiPM:**

An array of GAPD cells that are connected in parallel (each cell has binary output)



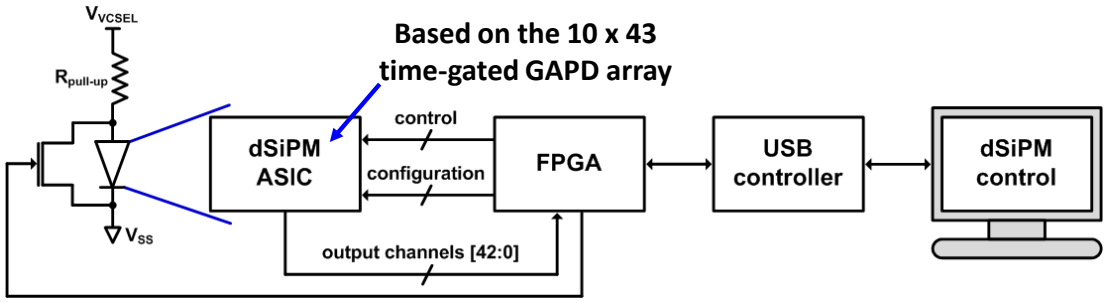
The output signal is the sum of the individual currents of the fired cells (analog output)

- GAPD based nature + analog output → high pattern noise with typical values from 10^5 to 10^6 Hz/mm^2
- The intensity of the impinging signal → by counting the number of cells fired
- High pattern noise → high threshold event → not possible to detect weak intensities

- **Typical solutions:**
- Work at cooled temperatures → pattern noise of 10^3 Hz/mm^2 at -20 °C (still high)
- Switch off those GAPD cells with an abnormal DCR (Philips) → FF ↓
  PDP ↓
  DR ↓
- Another possible solution is the time-gated operation with short gated-on periods…

Further improvements. Reduction of the threshold event in dSiPMs.

- **Experimental set-up**:



dSiPM

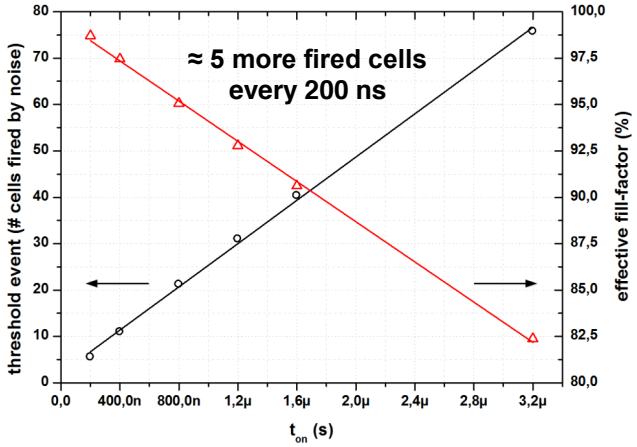
- V_{OV}=1 V
- t_{obs}=200 ns → 3.2 µs
- t_{off}=1 µs
- n_{rep}=10^5 frames

VCSEL

- V_{VCSEL}=5 V → 6 V
- t_{laser}=100 ns (within t_{obs})

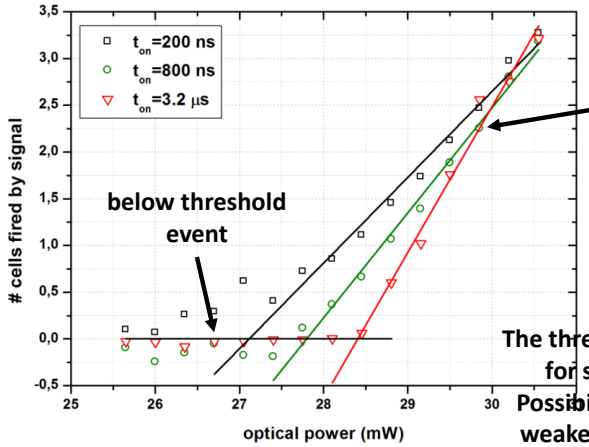
- **Results**:

1. In darkness → $\text{threshold event} = \frac{1}{n_{rep}} \sum_{n=0}^{429} \text{noise counts}_{\text{cell n}}$



2. With VCSEL →

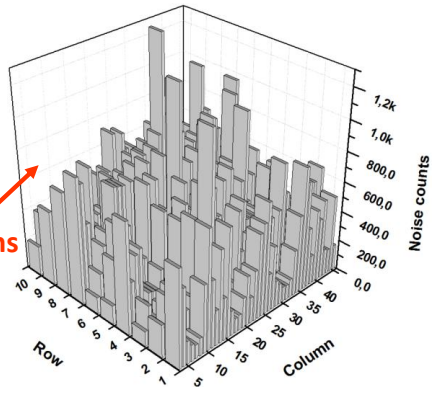
$\text{cells fired by signal} = \frac{1}{n_{rep}} \sum_{n=0}^{429} \text{counts}_{\text{cell n}}$ - threshold event



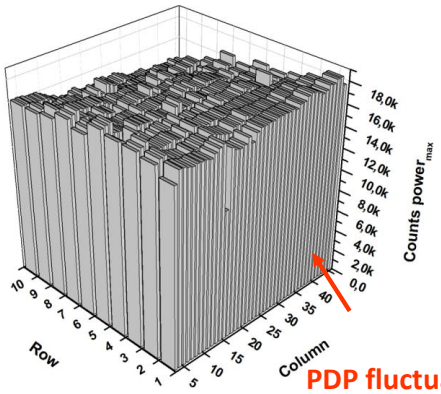
Further improvements. Non-uniformity correction system.

- During the fabrication process, doping profile fluctuations and lattice defects are unavoidably introduced

Consequences amongst the pixels of a GAPD array



DCR fluctuations



PDP fluctuations

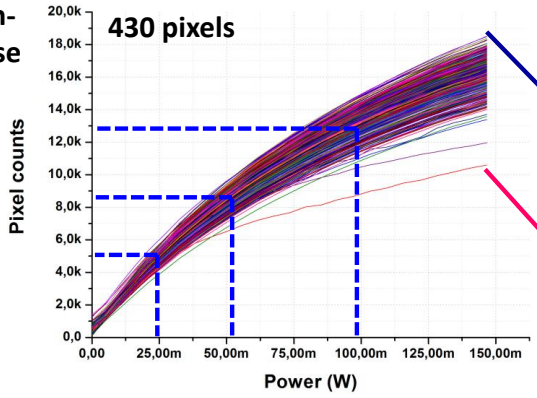
10 x 43 GAPD array

- V_{OV}=1 V
- t_{obs}=10 ns
- t_{off}=1 µs
- n_{rep}=10 Mframes

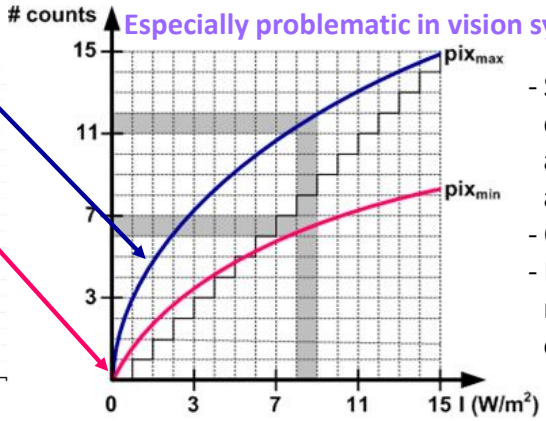
Light source

- 9 white LEDs

Also, GAPD pixels present a non-linear response



Especially problematic in vision systems:



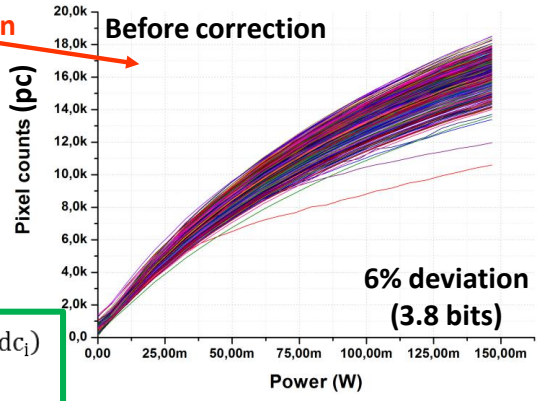
- Same irradiance → different # counts across the pixels of an array
- Overlapped areas
- Levels of representation (bits of contrast) are lost

Further improvements. Non-uniformity correction system.

- The problem can be reduced with correction techniques based on calibration algorithms (equation)

- With 1 eq. per pixel, linear correction:

High deviation

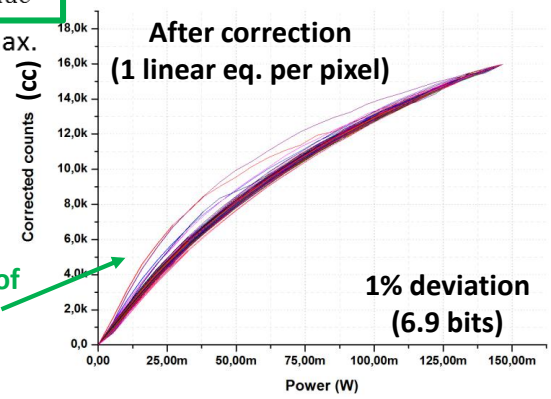


Calibration equation:

$$cc_i = k_i \cdot (pc_i - dc_i)$$

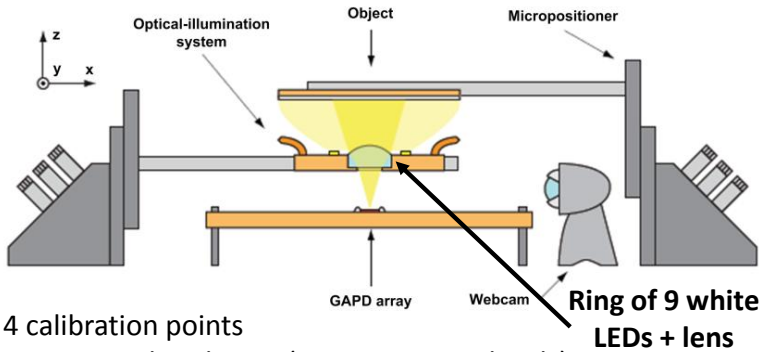
$$k_i = \frac{pc_i - dc_i}{\text{average value}}$$

(k_i is at the max. irradiance)



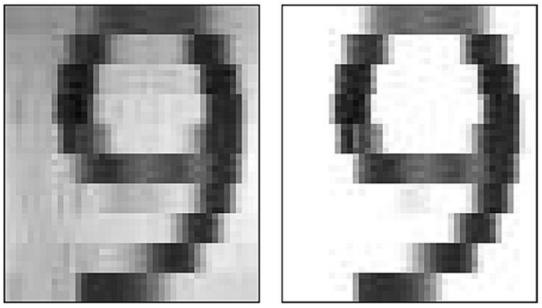
The response of the pixels is equalized!!

- With 1 B-spline per pixel, non-linear correction:



- 4 calibration points
- 256 interpolated pairs (representation levels)
- generated values saved in a LUT

- Results:



Linear correction **Non-linear correction**