Update on SLDO Calibration

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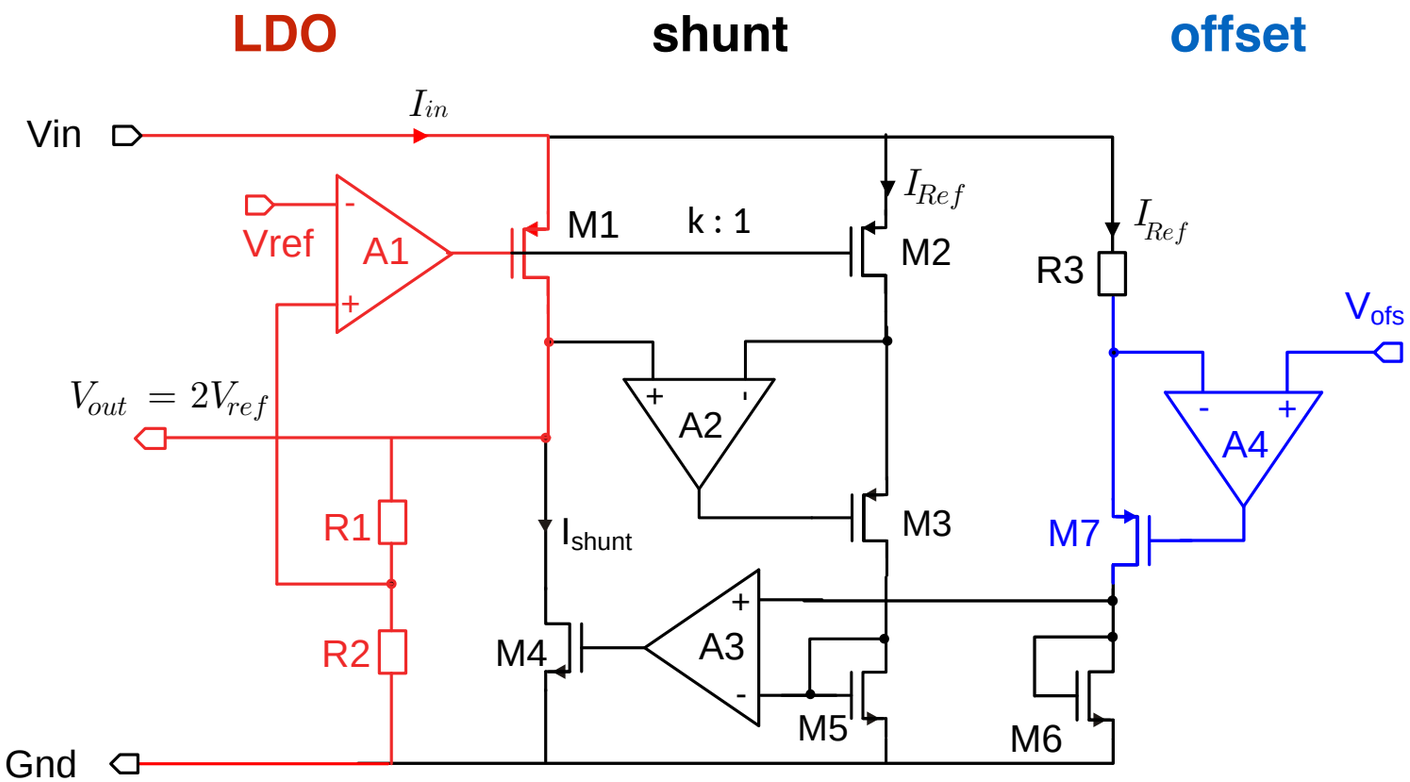
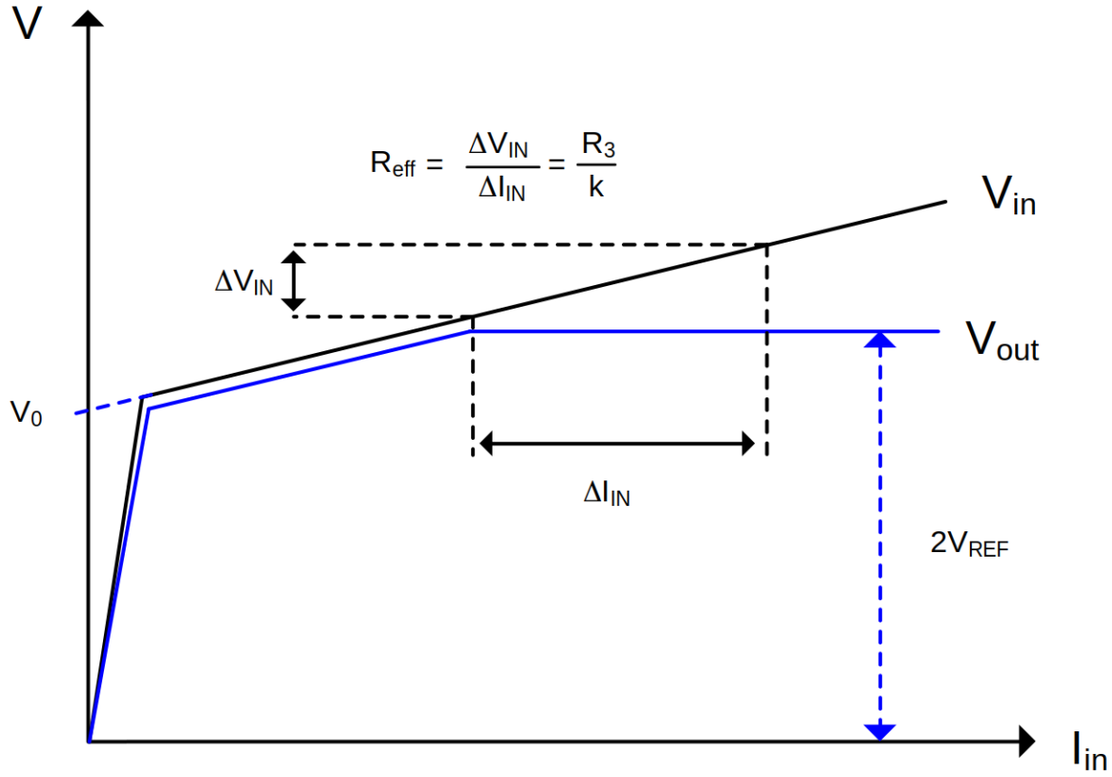
Introduction

- To set up serial power chain, need to understand operation in shunt mode
- Want to test the stability of shunt mode setting
  - Discuss IV curve results on SCCs and hybrid tested
  - Difficulty in measuring transients

Serial powering: shunt mode



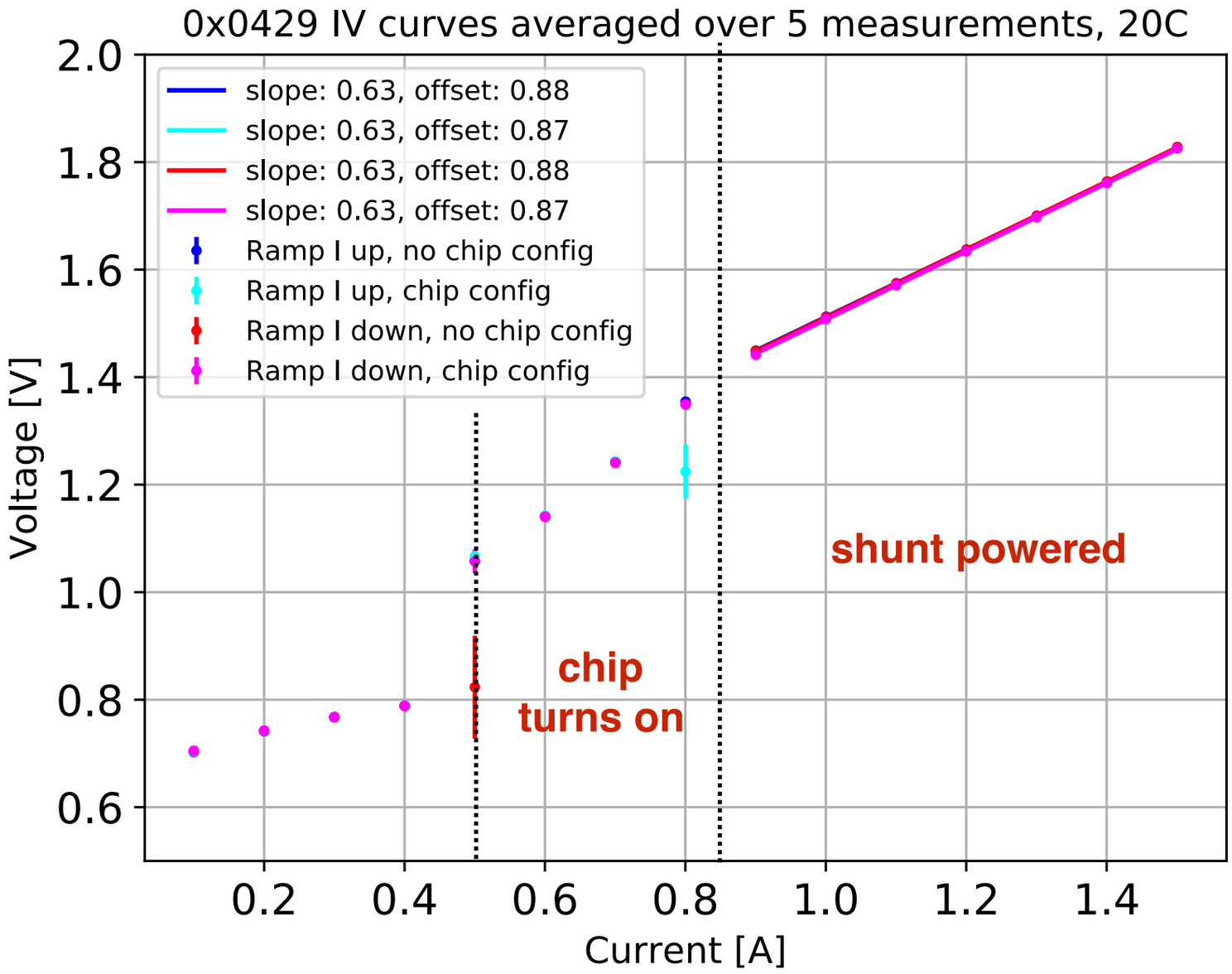


- Shunt current depends on Voffset and R3
- Want a small slope so don't consume too much current
  - Need to set offset and external resistors
  - Both of these are controlled by resistors on the SCC
- Measured to be:
  - RoffsA: 232k, RoffD: 226k
  - RextA: 1.15k, RextD: 1.07k

How to: I-V curves

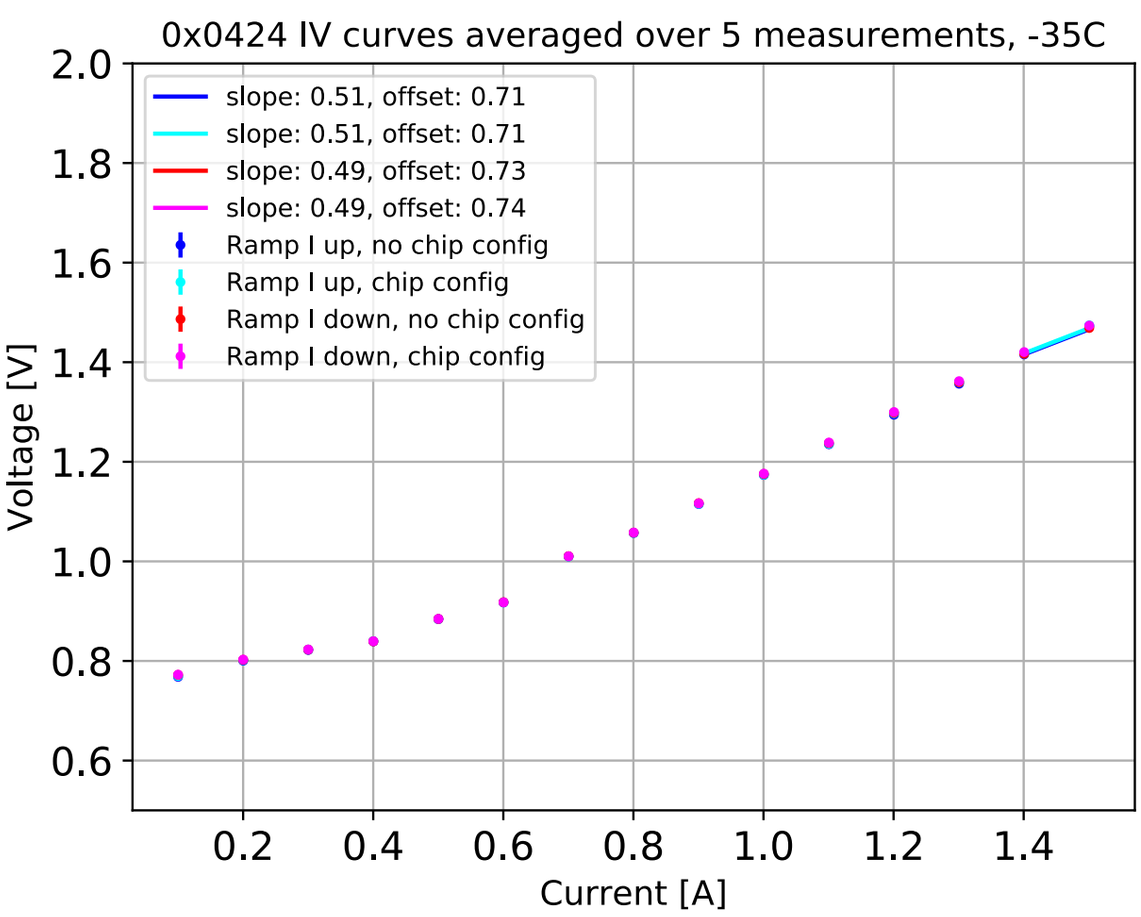
- In constant current mode, vary the current and measure the voltage
  - Do a power cycle between each change in current
- Tests conducted
    - Ramp current up and ramp current down
    - Room temperature (~20C) and at -35C
    - With chip configuration and without chip configuration
- 5 current ramps are taken for each configuration to increase statistics

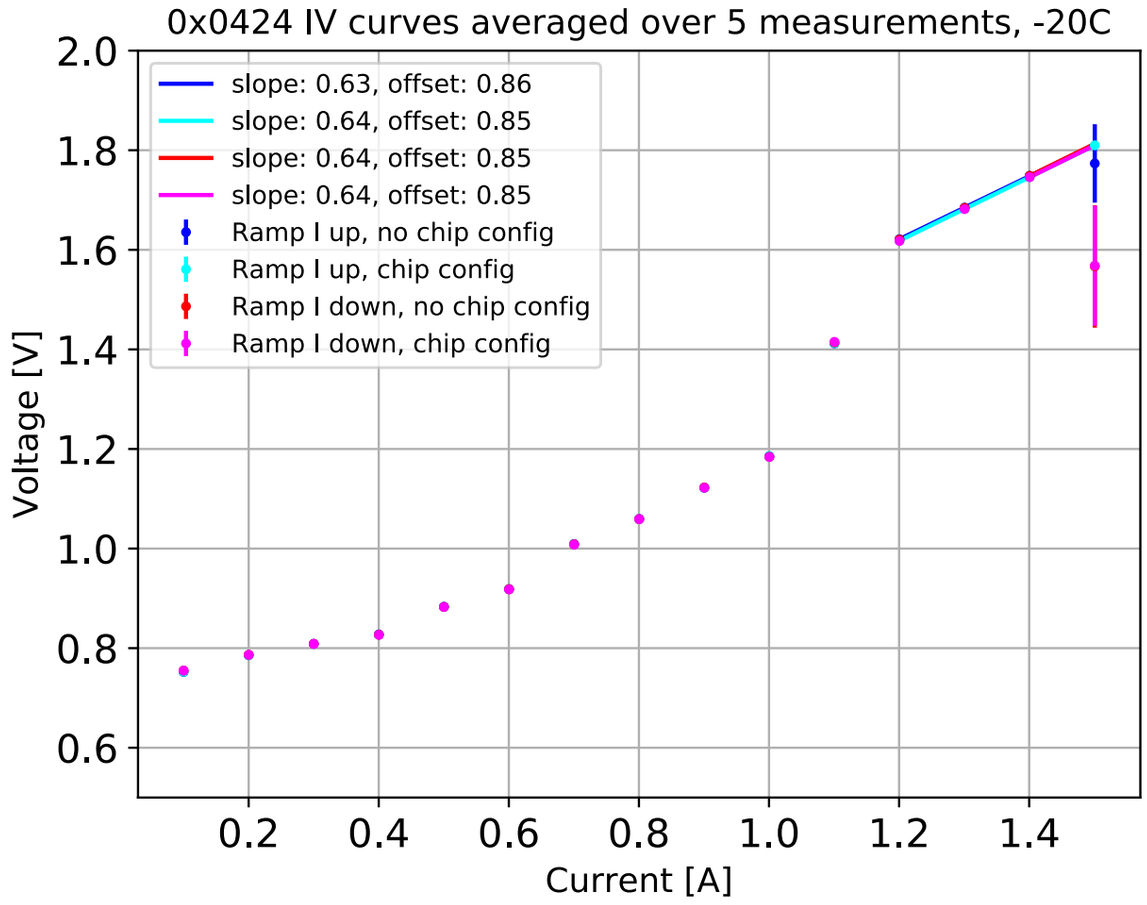
I-V curves for 0x0429



- Points are fit for voltages > 1.4 V
- Offset voltage close to 0.9 V (expected offset voltage)

Chip turn-on issues

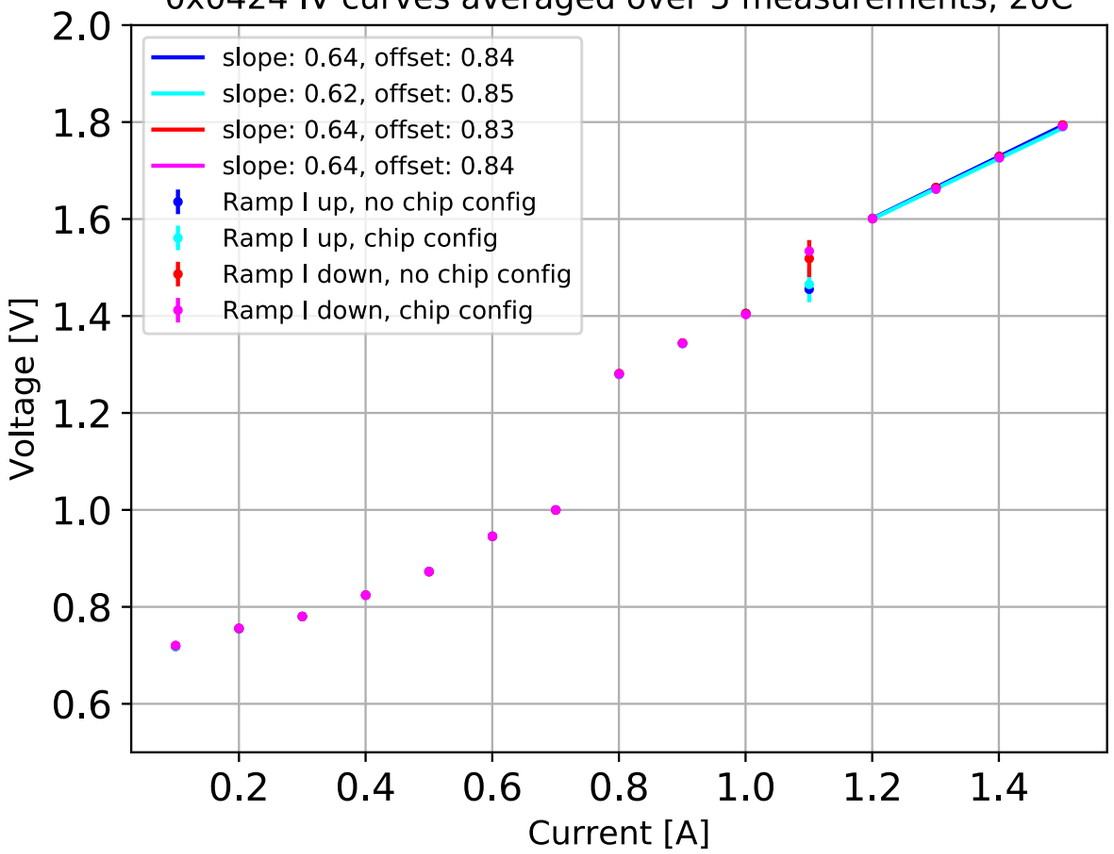




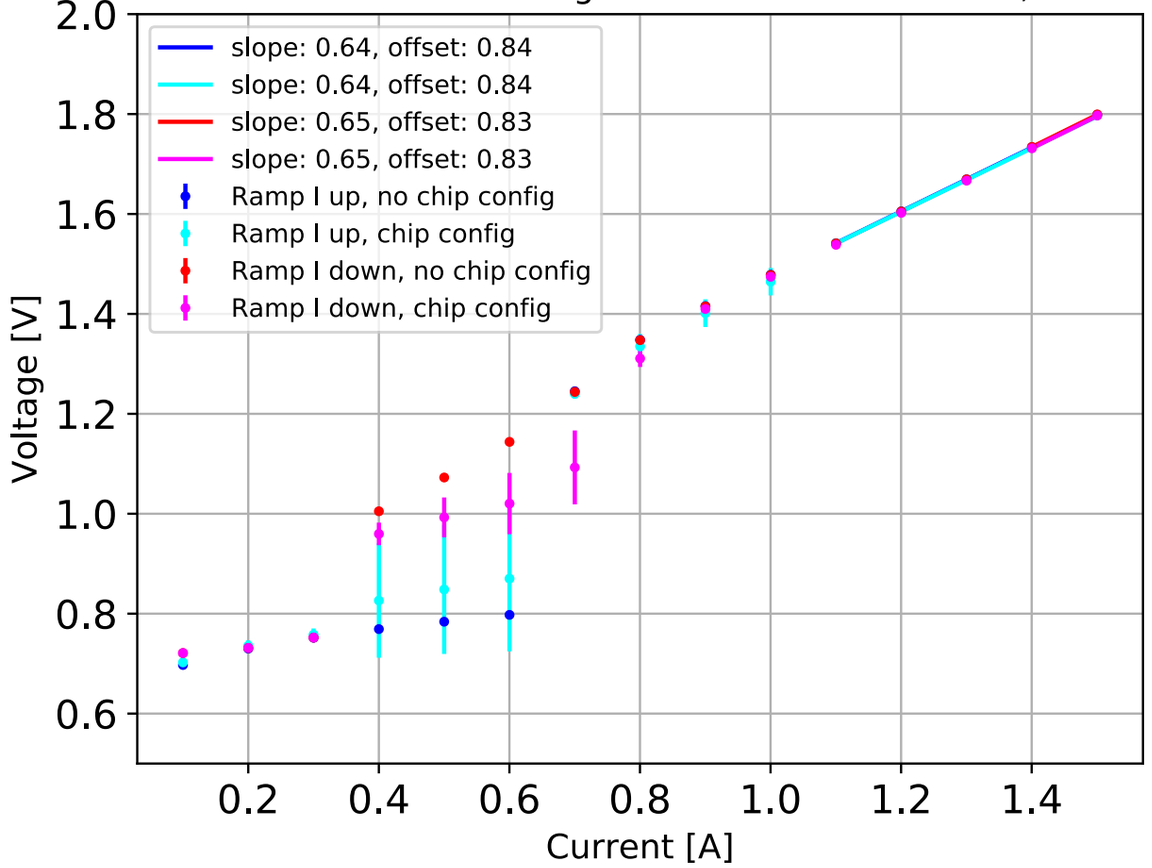
- 0x0424 does not start up at -35C, just like 0x796
- (see slide 18-20 for voltage measurements as a function of temperature)
- At -20C, chip starts up and offset is at 0.85, similar to when the chip is warm
  - Note: last point at 1.5 A not included in the fit
- To be able to run this chip at -35C, need to turn it on at -20C then lower the temperature, slide 21

Impact of power cycling

with power cycles



no power cycles



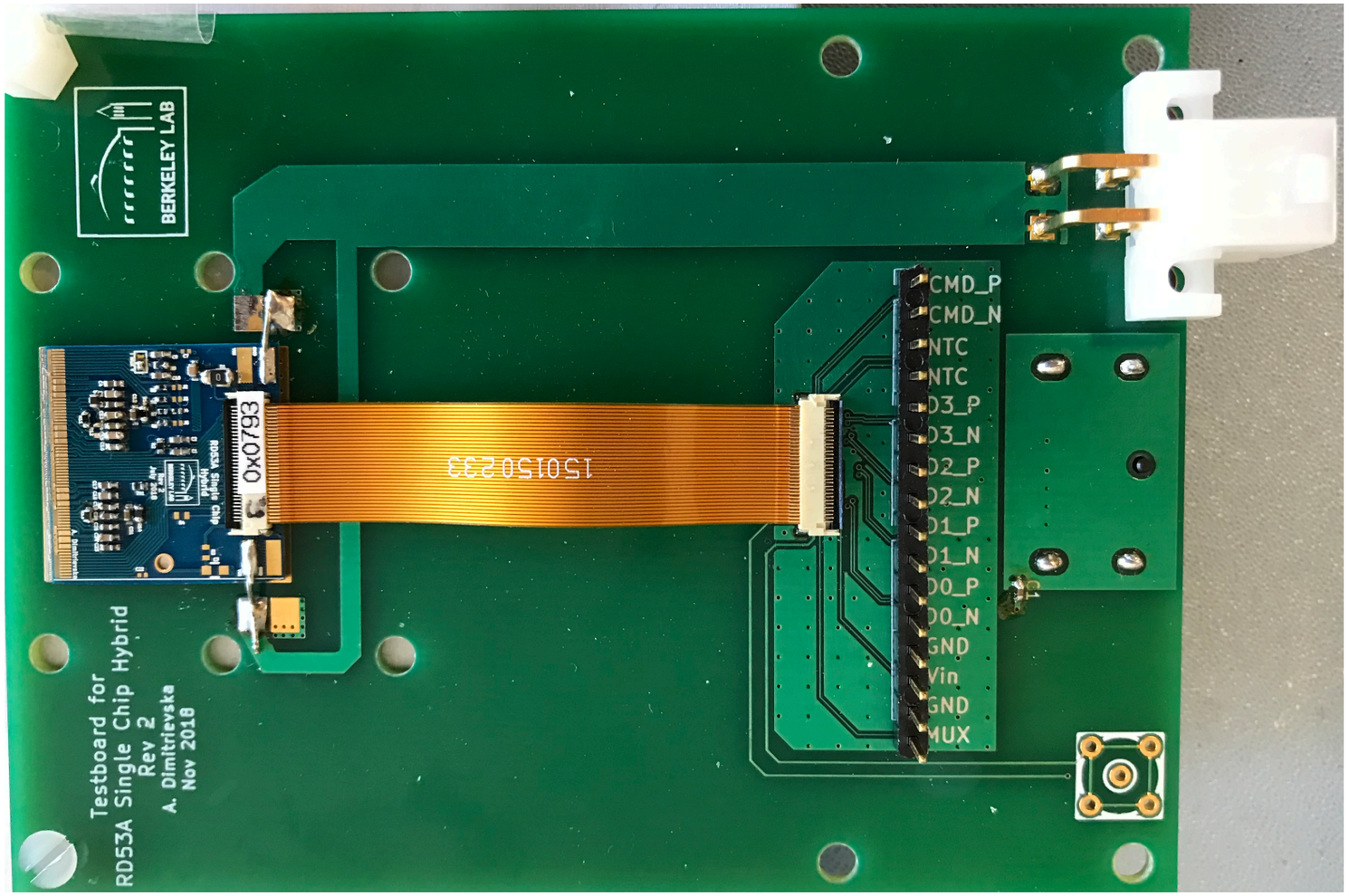
- With power cycles, do not see difference between ramping the current up or down at chip turn-on
- No power cycles: Ramping current down produces larger voltages than ramping current up
- For QC, might want to power cycle in between each measurement

Slope and offset depending on Iref

SCC	Iref settings	Trim settings	Temperature (C)	Offset [V]	Slope
424	7 (4.03 µA)	analog 22 digital 26	20	0.84	0.64
424	6 (3.91 µA)	analog 22 digital 26	20	0.84	0.65
424	8 (4.17 µA)	analog 22 digital 26	20	0.84	0.65
424	15 (5.00µA)	analog 22 digital 26	20		

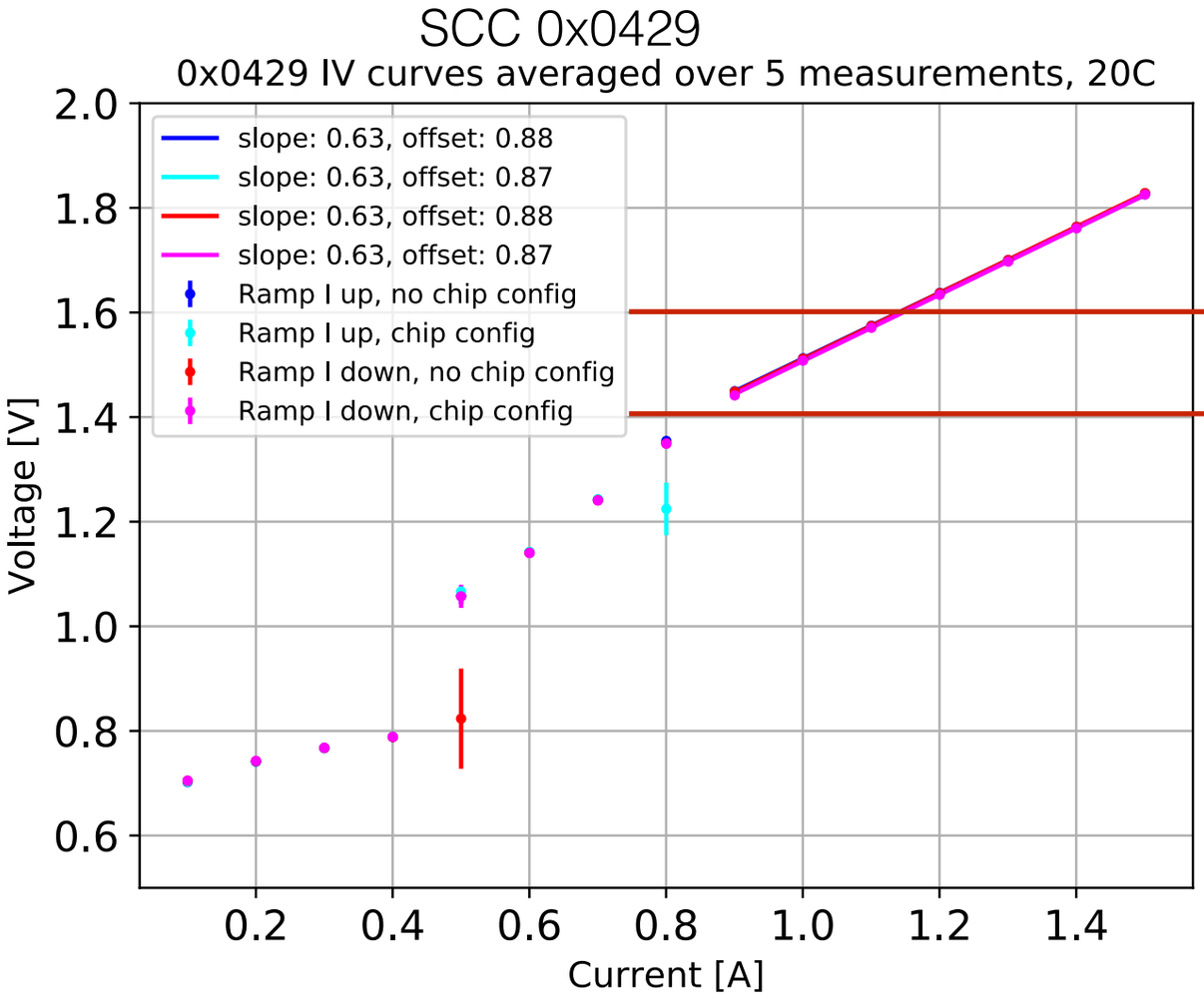
- IV curves are in the backup, slide 24
- No impact on the slope and offset when varying the Iref by ±1 setting

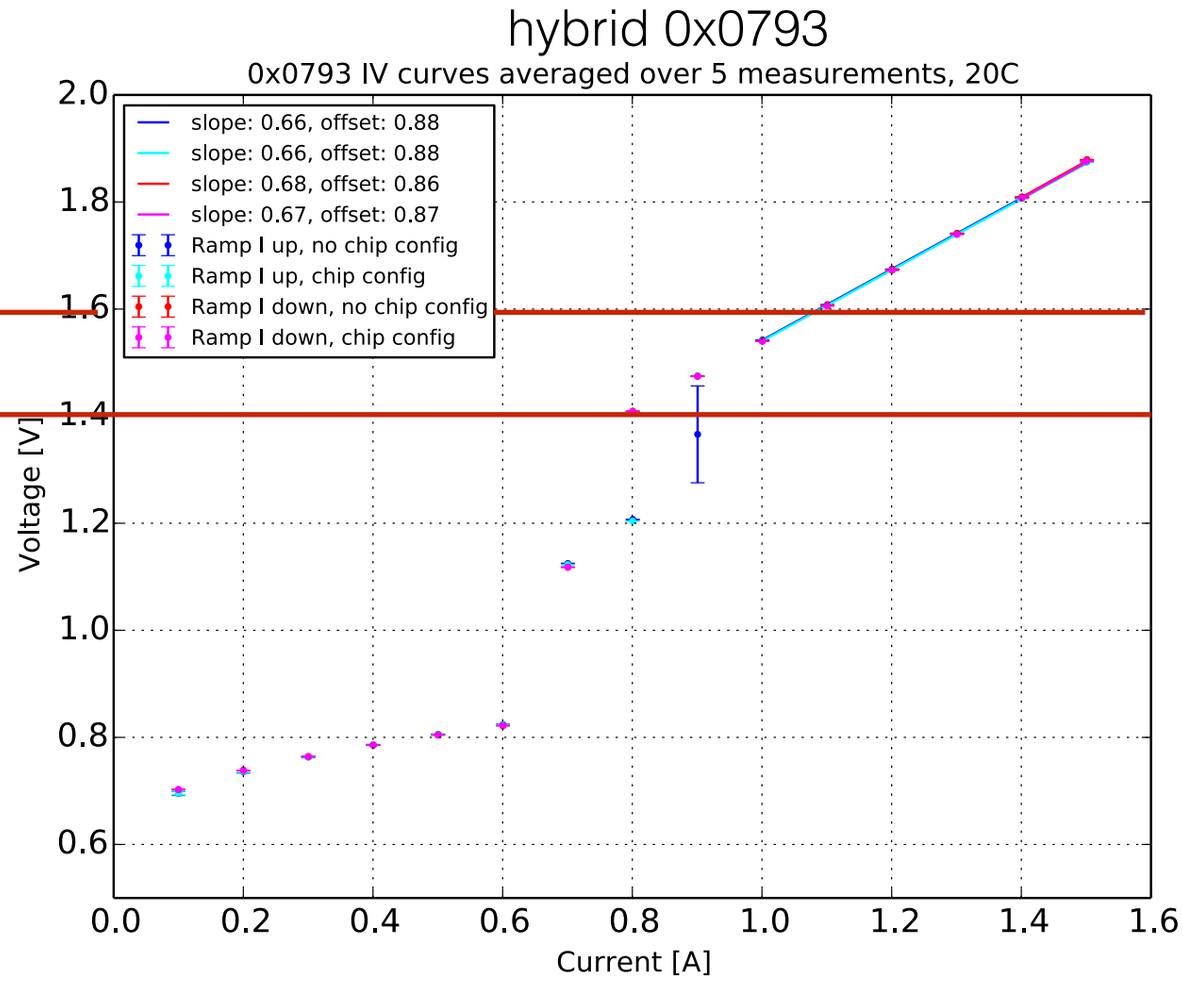
Hybrid testing



- Resistors with 0.1% tolerance used for external and offset resistors
- Note: could not measure Iref and trim voltages because MUX connection is not working

IV curve on hybrid





- Offset is about 0.88, slope is 0.67
  - Slope is steeper than for other chips
- Need to determine better procedure for turn
  - How low in current can we be at and still communicate with the chip?
- Seems that offset resistors are ~consistent across set of chips tested
- Would want to possible change the slope resistors

Summary of slope and offset measurements

SCC	Iref settings	Trim settings	Temperature (C)	RIofsD [kΩ]	RIofsA [kΩ]	RextA [kΩ]	RextD [kΩ]	Offset [V]	Slope
429	6 (3.99 µA)	analog 23 (1.219 V) digital 22 (1.190 V)	20	225.4	232.3	1.1562	1.079	0.88	0.63
429	6 (3.99 µA)	analog 19 digital 22	-35	225.4	232.3	1.1562	1.079	0.91	0.62
796	8 (4.04 µA)	analog 23 (1.193 V) digital 25 (1.202 V)	20	225.6	232.6	1.157	1.075	0.84	0.63
424	7 (4.03 µA)	analog 22 (1.204 V) digital 26 (1.202 V)	20	225.3	232.4	1.1555	1.076	0.84	0.64
424	7 (4.03 µA)	analog 19 digital 26	-20	225.3	232.4	1.1555	1.076	0.85	0.64
793	-	analog 28 digital 22	20	not measured 226	not measured 232	not measured 1.15	not measured 1.07	0.87	0.67
793	-	analog - digital 22	-35	not measured 226	not measured 232	not measured 1.15	not measured 1.07	0.87	0.68

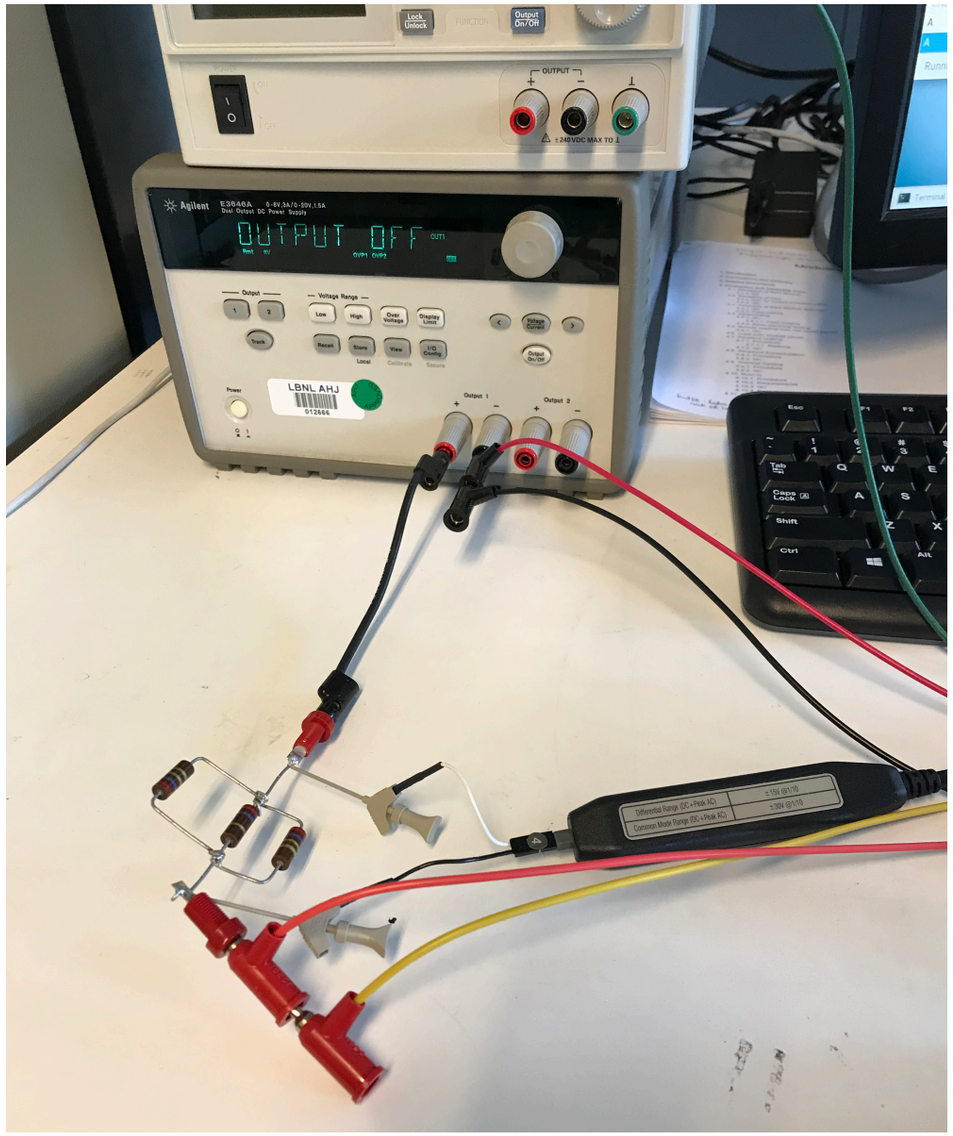
- Difference in offset and slope

Summary of voltages for 1.1A

SCC	Iref settings	Temperature (C)	Voltage [V]
429	6 (3.99 µA)	20	1.573 ± 0.001
796	8 (4.04 µA)	20	1.526 ± 0.002
424	7 (4.03 µA)	20	1.549 ± 0.002
424	6 (3.91 µA)	20	1.557 ± 0.002
424	8 (4.17 µA)	20	1.556 ± 0.003
793	-	20	1.609 ± 0.001
429	6 (3.99 µA)	-35	1.594 ± 0.001
424	7 (4.03 µA)	-20	1.413 ± 0.002
793	-	-35	1.546 ± 0.068

- Current value chosen from resistor tuning procedure
- At room temperature, voltages range from 1.53 V - 1.61 V
- At cold temperatures, range from 1.55 V - 1.59 V

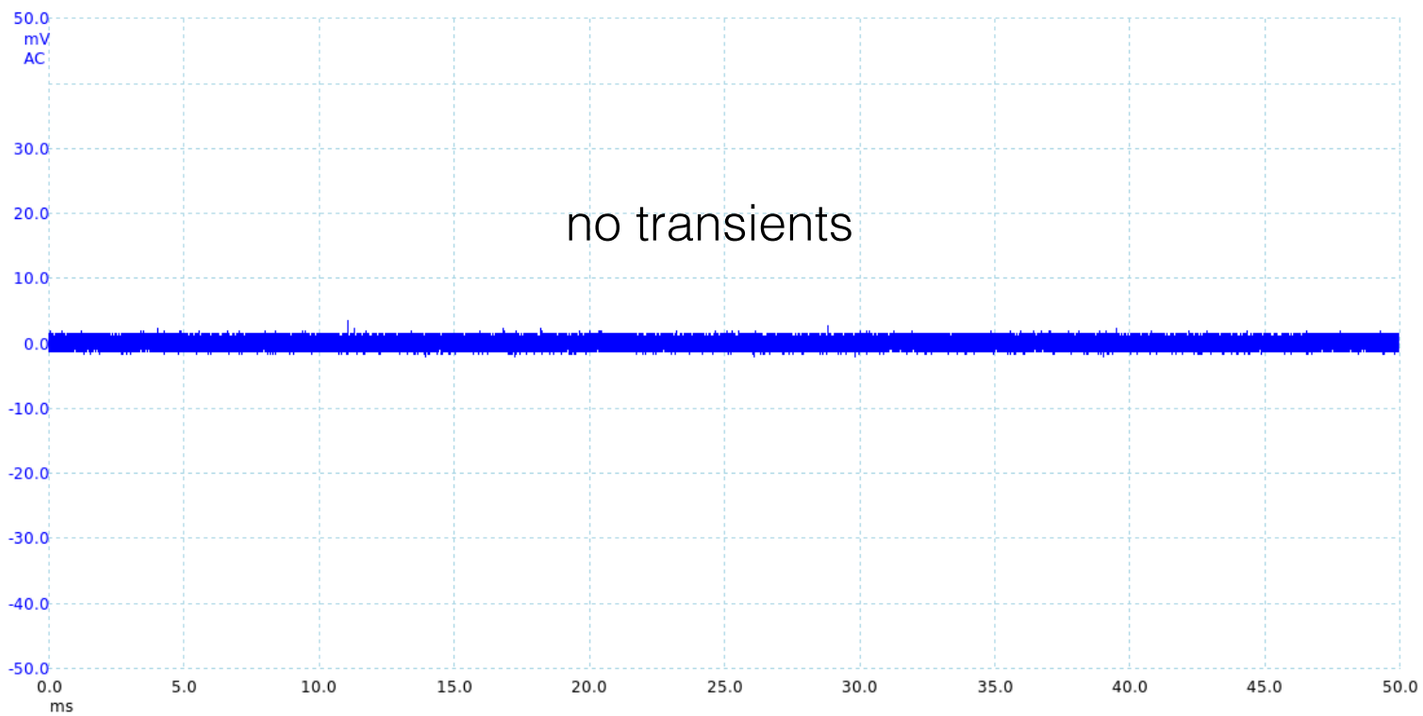
Transient measurements



- Put a 1 Ohm resistor in series with the SCC
  - Measure the resistance of the SCC
  - Adjust the voltage limit
  - Current setting should be the one for which the values were optmized: 1.1 A
- Take noise scans which consume a lot of current

Getting rid of the headroom

- Resistors were optimized for 20% headroom on both analog and digital voltages
- Need to get rid of headroom to see transients
- Reducing analog headroom by changing pre-amplifier values
  - M. Standke's slides about how current changes as function of preamp value
  - Differential: DiffPrmp, from 500 to 1000
  - Linear: LinPaInBias from 300 to 511
  - Synchronous: SyncIbiasp2 (120->500)
  - Voltage change after diff. and linear: -0.01, after sync pre-amp: -0.05V
- Reducing digital headroom: more difficult to do without changes Rext
  - Make DiffVth2 (50) > DiffVth1 (250)
  - Reduces Voltage by 0.3 V



Conclusion

- There is variance between the offsets and slopes
  - At 1.1A, see variance in current of 0.8 V
- Transients have been surprisingly difficult to try to measure
  - Need to switch out resistors to get rid of headroom?
- Next steps:
  - Keep doing IV curves to get more statistics
  - Need to determine if the resistor values are appropriate or not
  - Measure this on triplet to see impact of chips in parallel on IV curve
  - Automate the scripts for obtaining and plotting the IV curves for QC

Backup

Resistors stuffed for testing

SCC	Iref settings	Trim settings	RIofsD [kΩ]	RIofsA [kΩ]	RextA [kΩ]	RextD [kΩ]	Analog current [A]	Digital Current [A]	Plugged Together [A]
433	6 (3.99 μA)	analog 24 (1.238V) digital 19 (1.210V)	225.6	232.7	1.166	1.084	0.488	0.538	1.025
429	6 (3.99 μA)	analog 23 (1.219 V) digital 22 (1.190 V)	225.4	232.3	1.1562	1.079	0.530	0.621	1.143 (powered) 1.148 (config)
796	8 (4.04 μA)	analog 23 (1.193 V) digital 25 (1.202 V)	225.6	232.6	1.157	1.075	0.601	0.624	1.216 (powered) 1.220 (config)
424	7 (4.03 μA)	analog 22 (1.204 V) digital 26 (1.202 V)	225.3	232.4	1.1555	1.076	0.572	0.639	1.198 (powered) 1.205 (config)

- 1.60V set on power supply

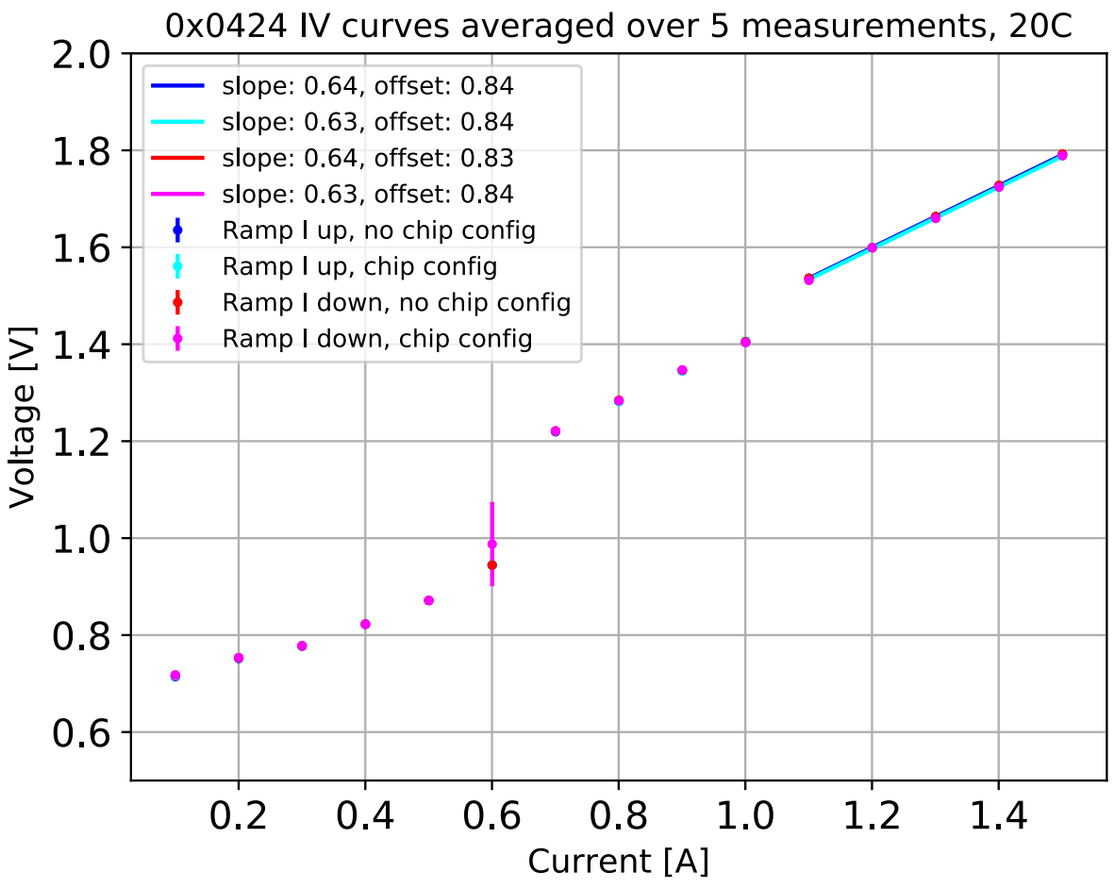
Iref as a function of temperature

Iref (μA)	Temperature (C)
4.04	20
4.026	10
4.020	0
4.011	-10
4.008	-20
3.998	-35

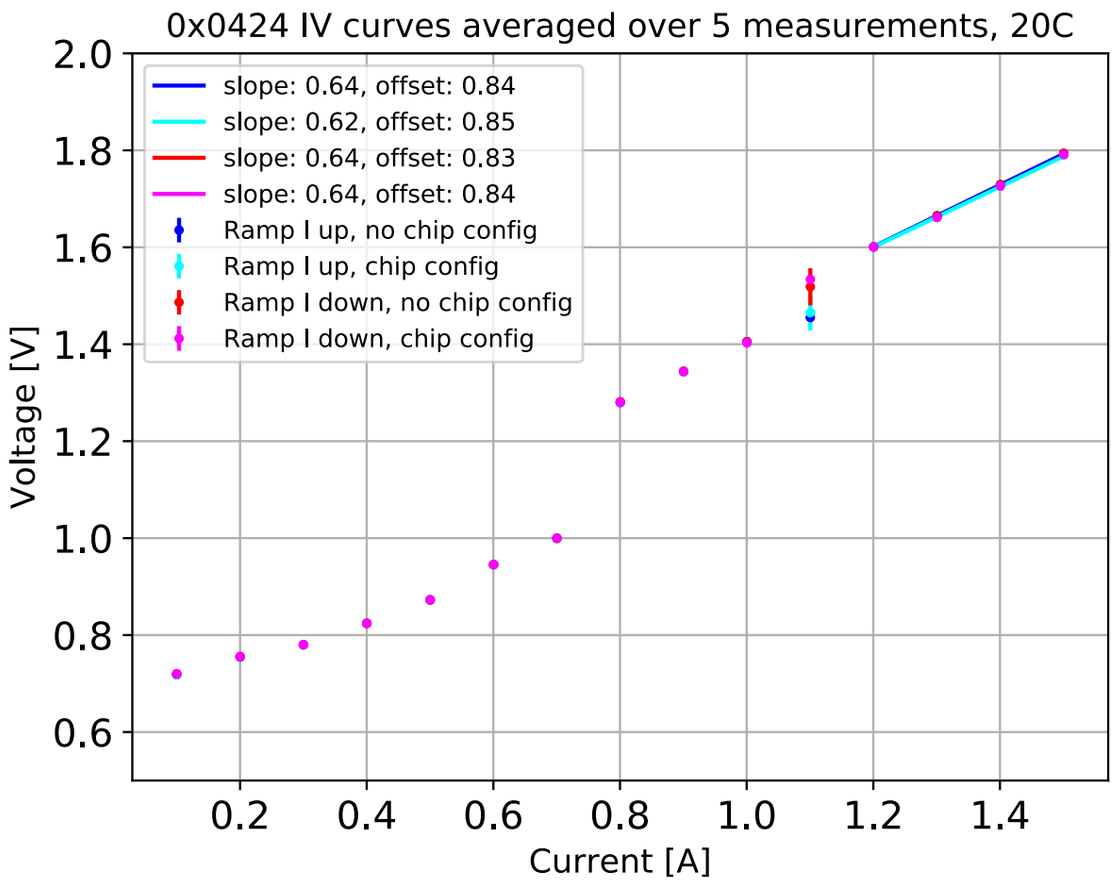
- Small drop in Iref as a function of temperature

IV curves for 0x0424

on bench



in climate chamber



- 0x0424 does not have a pull-up resistor between VDDA and Vref
- Slightly lower offset than 0x429 (0.88 V vs. 0.84 V for 0x0424)
- Slightly higher offset when configuring the chip
  - Slight difference between ramp up/ramp down in chip turn-on

Voltages as a function of temperature

temperature	VrefA	Vrefd	VDDA	VDDD	Power supply voltage
20.3	0.568	0.537	1.139	1.087	1.67
8.3	0.567	0.536	1.138	1.084	1.67
-1.4	0.566	0.535	1.136	1.081	1.67
-11	0.566	0.532	1.135	1.078	1.67
-20.4	0.565	0.530	1.134	1.075	1.67
-25.0	0.564	0.529	1.134	1.072	1.69 (although started up at 1.36)
-29.8	0.550	0.112	1.103	0.150	1.37
-30.0	0.565	0.528	1.133	1.070	1.69
-34.5	0.559	0.132	1.125	0.163	1.50
-35.3	0.547	0.116	1.098	0.151	1.37

- Power cycles between each measurement
- The chip turns on till about -25C then the chip does not turn on
  - Analog and digital voltages are low

Voltages as a function of temperature

temperature	VrefA	Vrefd	VDDA	VDDD
20	0.566	0.535	1.137	1.082
8.8	0.566	0.534	1.136	1.079
-1.1	0.565	0.532	1.134	1.077
-10	0.564	0.530	1.133	1.073
-20	0.564	0.529	1.132	1.070
-35	0.563	0.526	1.130	1.065

- No power cycles between each measurement
- The chip is functional if it is already turned on before lowering to -35C

Voltages as a function of temperature

Adding 300k between Vref and VDD
(for both analog and digital)

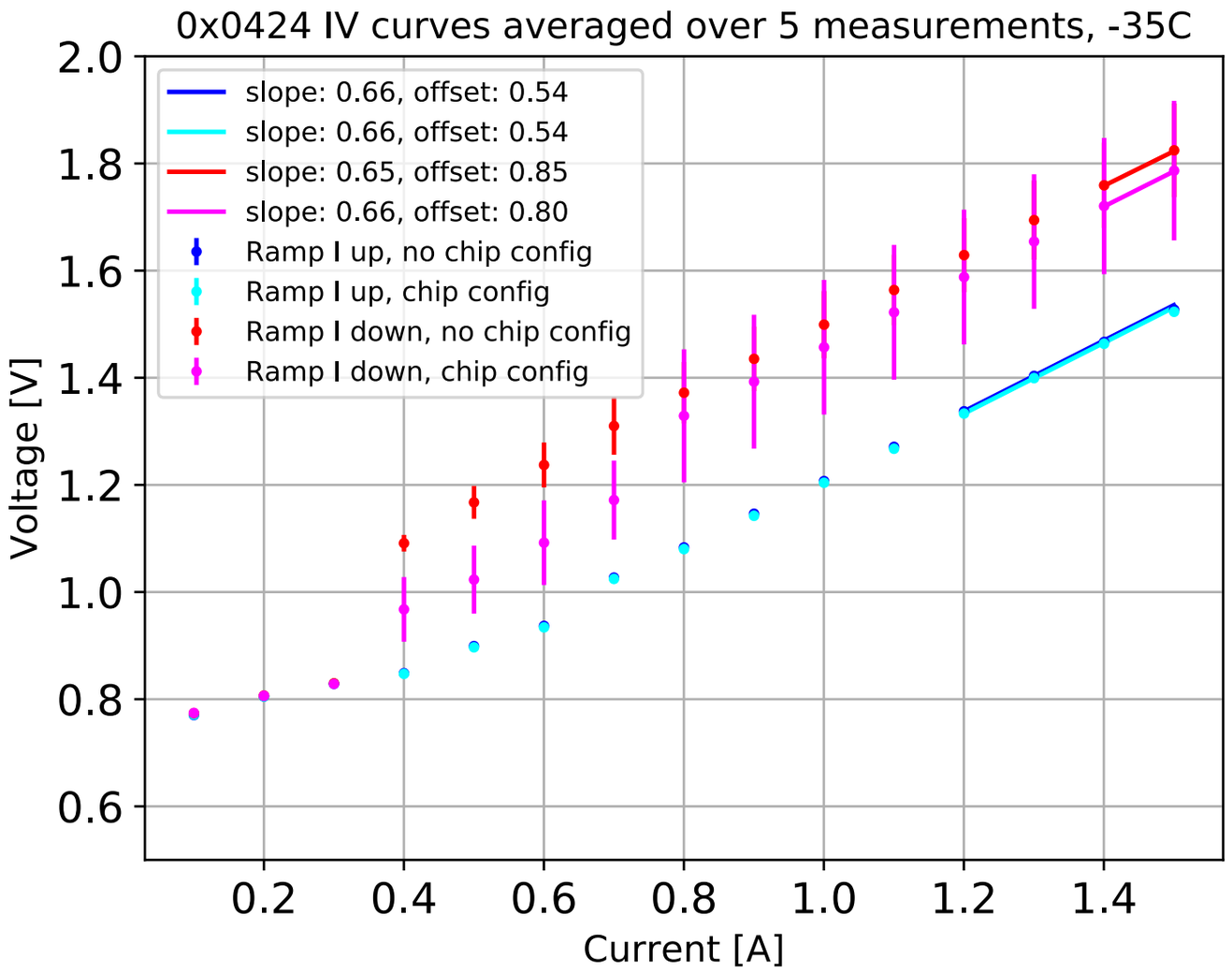
Temperature	VrefA	VrefD	VDDA	VDDD	PS voltage
20	0.591	0.560	1.187	1.133	1.67
8.7	0.590	0.559	1.184	1.129	1.67
-0.9	0.589	0.556	1.183	1.126	1.67
-10.0	0.589	0.555	1.181	1.121	1.68
-20.4	0.588	0.554	1.180	1.119	1.69
-25.3	0.588	0.553	1.180	1.118	1.69
-30.4	0.587	0.552	1.180	1.118	1.38, 1.51, 1.70
-35.1	0.564	0.118	1.133	0.155	1.37

Powering pLL from an external 1.15 V source

Temperature	VrefA	VrefD	VDDA	VDDD	PS voltage
18.4	0.567	0.536	1.138	1.085	1.67
-1.4	0.566	0.534	1.137	1.079	1.68
-10.9	0.566	0.532	1.135	1.076	1.68
-20.5	0.565	0.531	1.134	1.073	1.68
-25.4	0.561	0.125	1.127	0.159	1.51
-25.4	0.565	0.530	1.134	1.072	1.68
-30.3	0.560	0.129	1.126	0.161	1.51

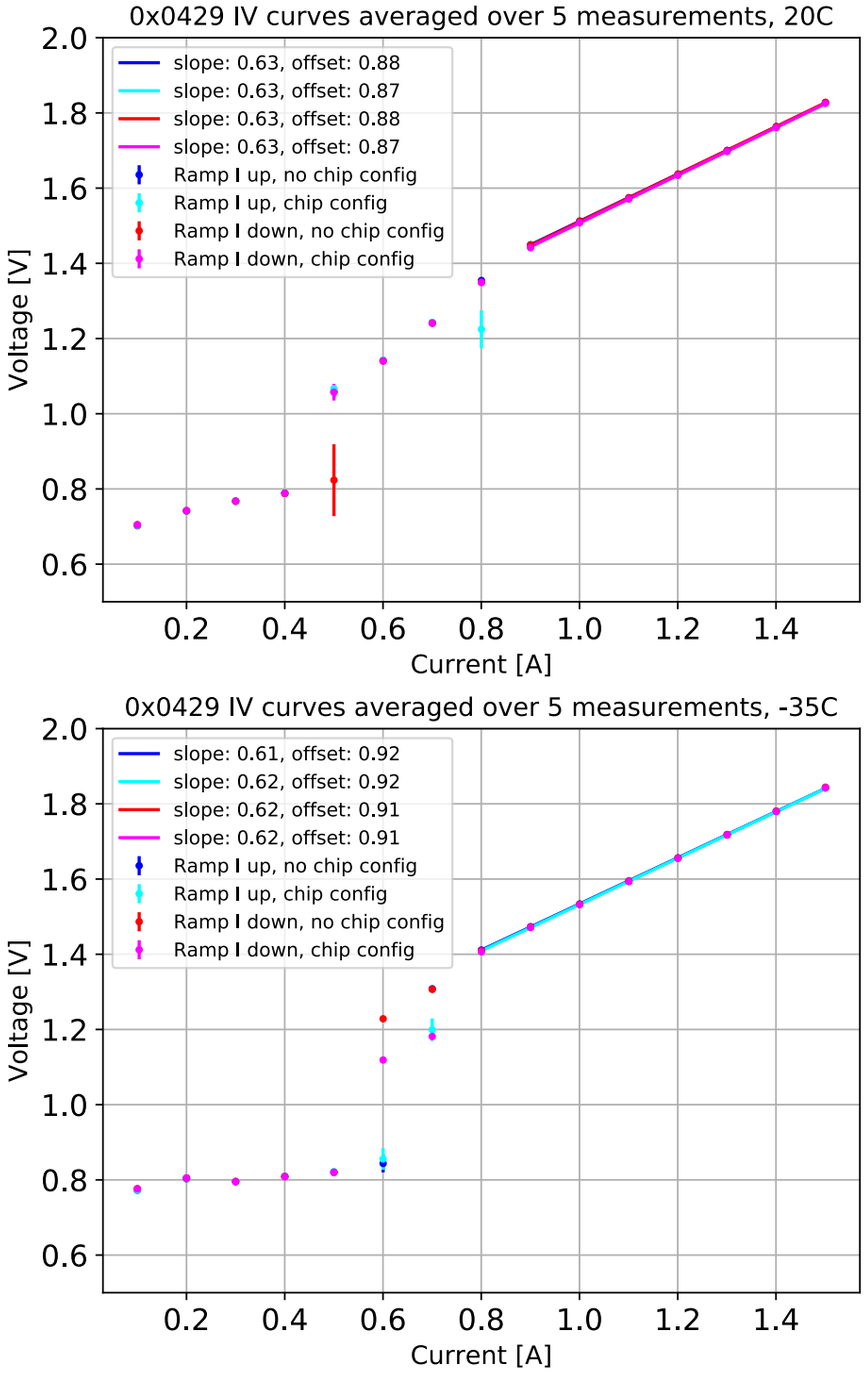
- Cannot get the chip to power on at lower temperature

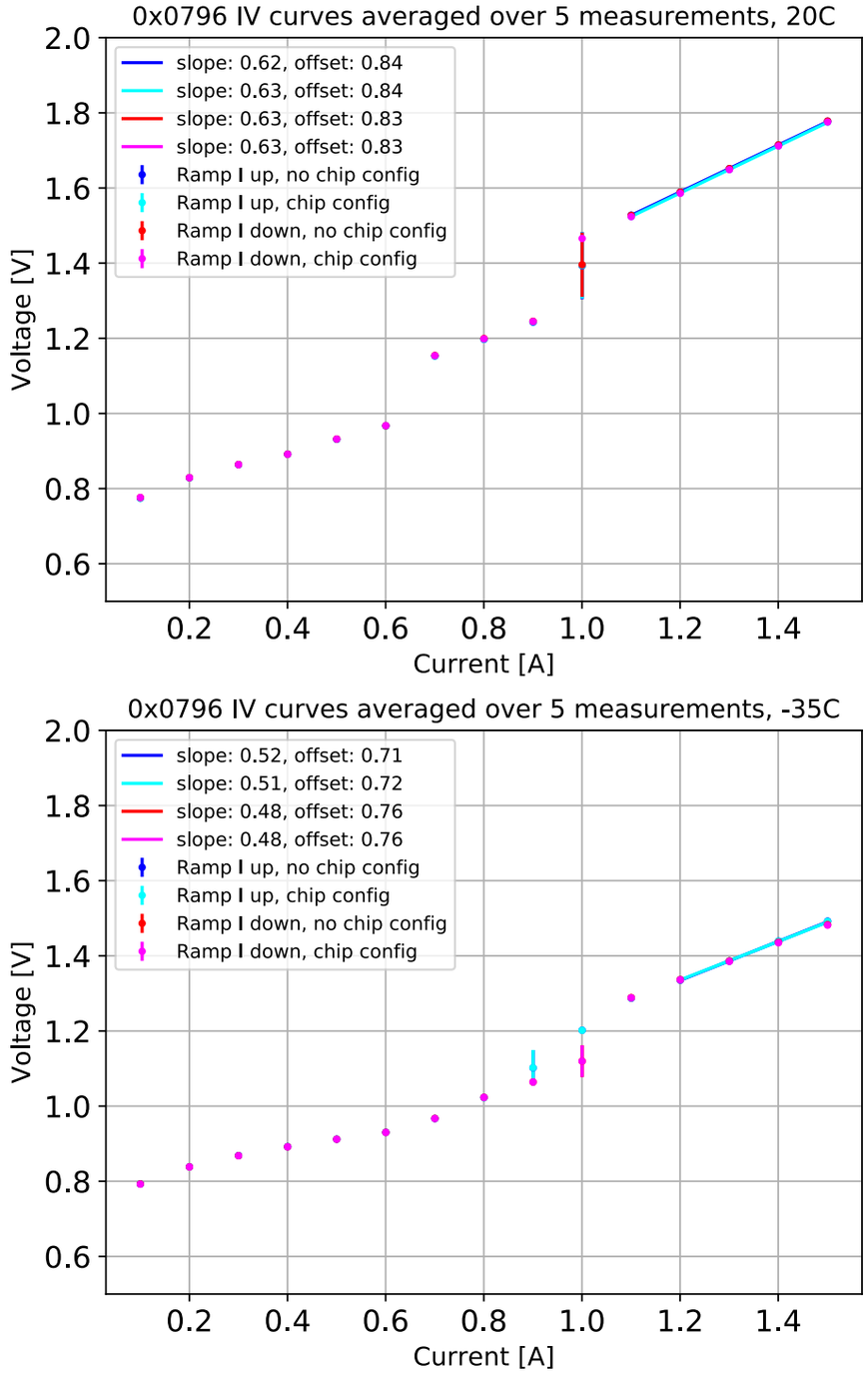
IV curves at -35C, no power cycle



- When chip already powered at -35C and ramping down (red curve), get expected offset
- Chip is functional at -35C as long as it is not power cycled or have too low of current

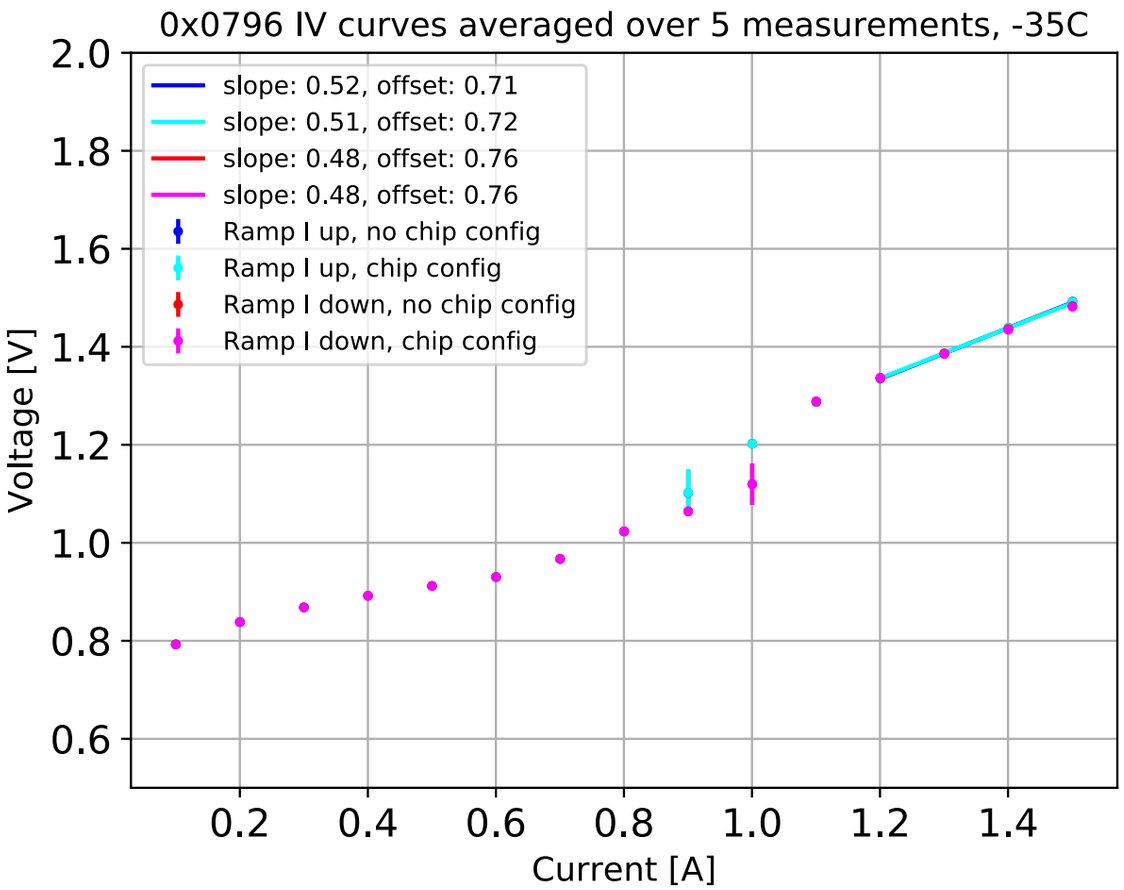
Comparing I-V curves

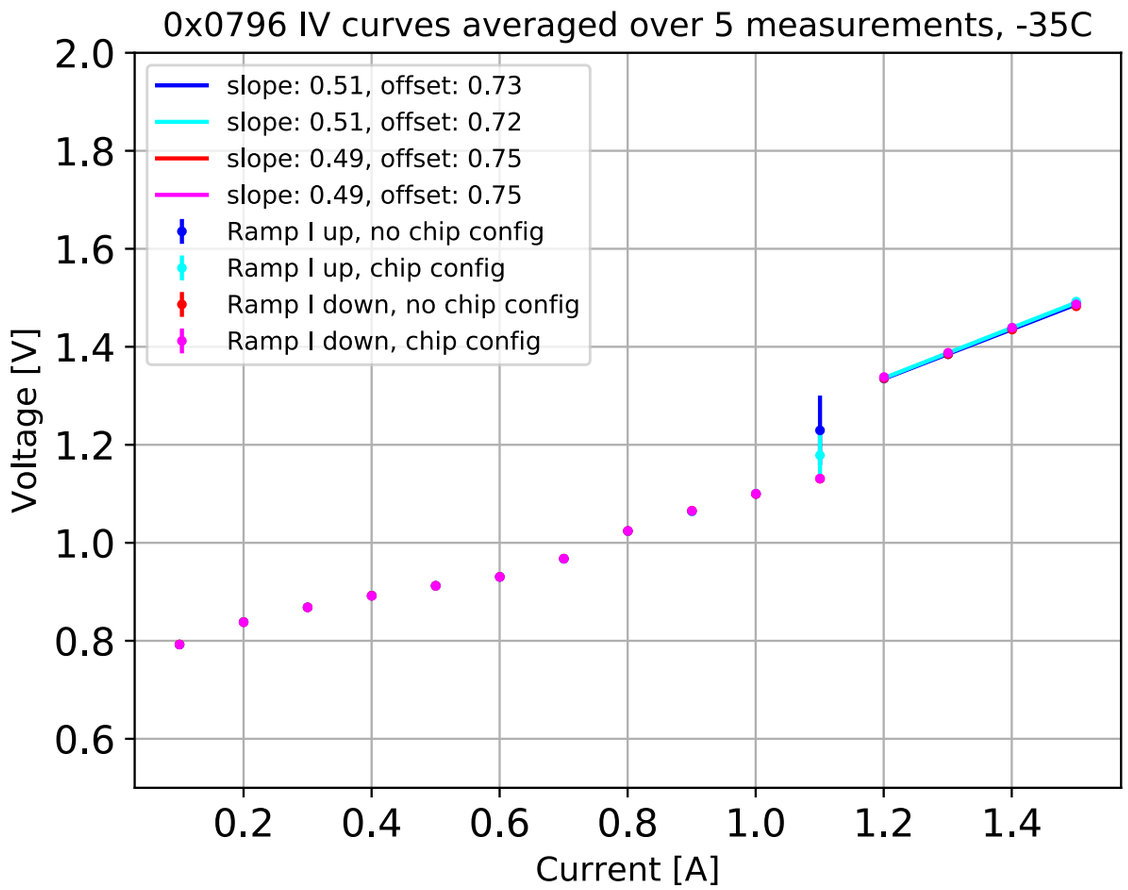




- 0x0796 has a resistor between VDDA and Vref: offset is lower for 0x796
- Drop in voltage for 0x796 from measurement at 20C to -35C

0x796 after adjusting Iref at -35C

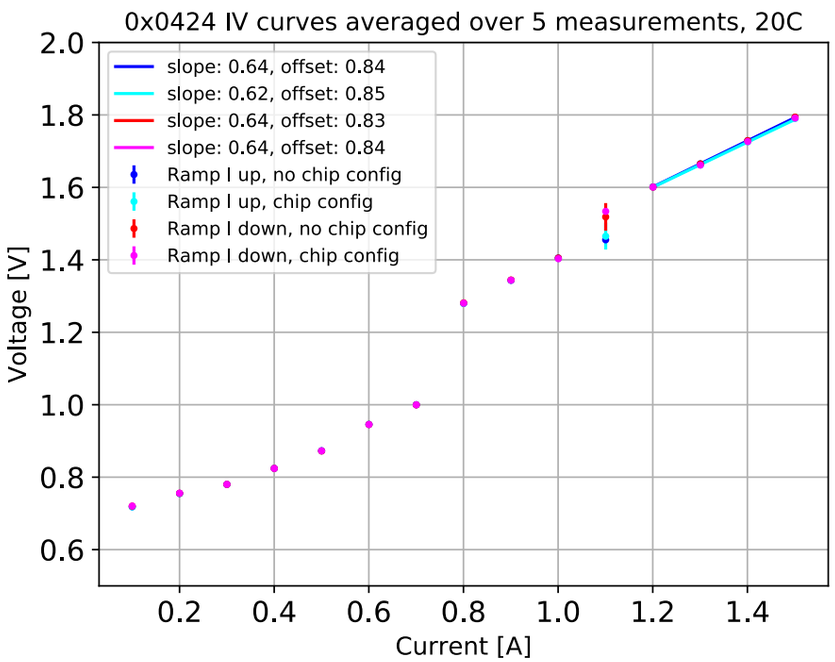




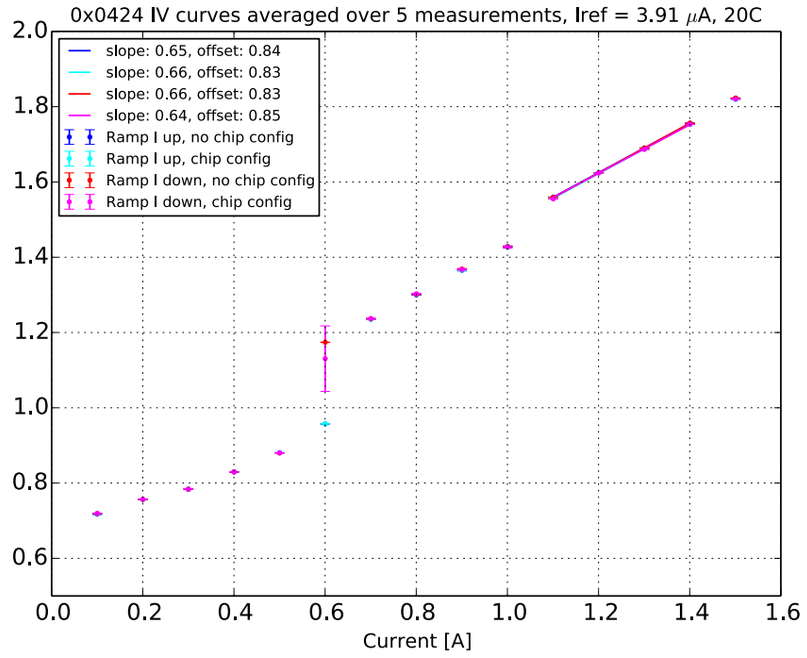
- Iref dropped 0.05 µA when going from +20 C to -35 C
- Iref was adjusted from setting 7 to setting 8 so Iref was 4.1 µA
  - Iref is not very dependent on current, see backup
- No impact on the offset

IV curve depending on Iref

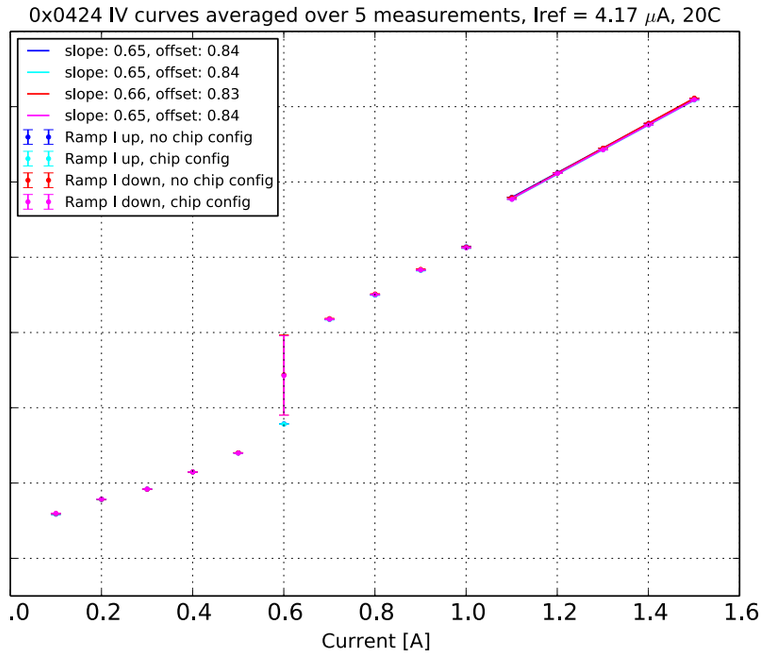
Iref (7): 4.04µA



Iref (6): 3.91µA

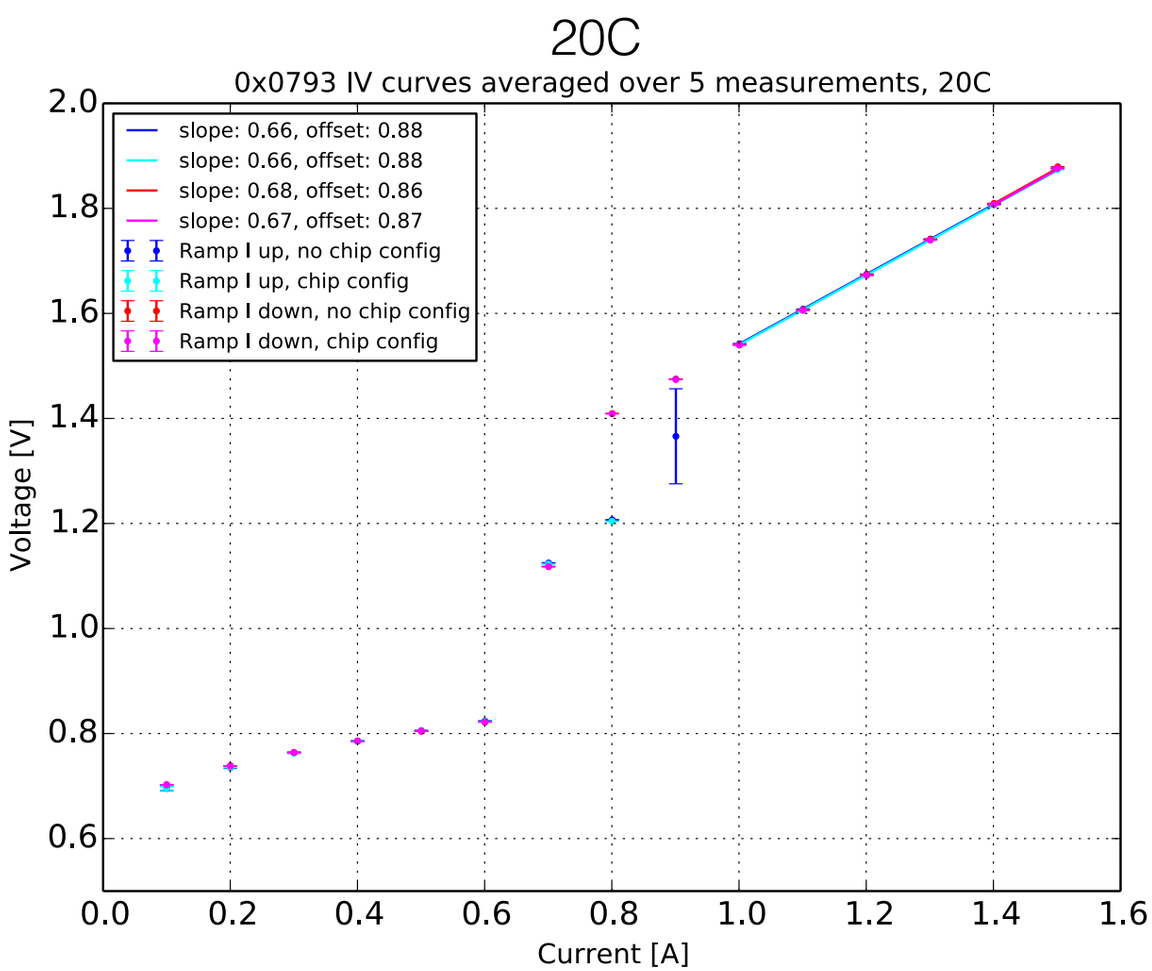


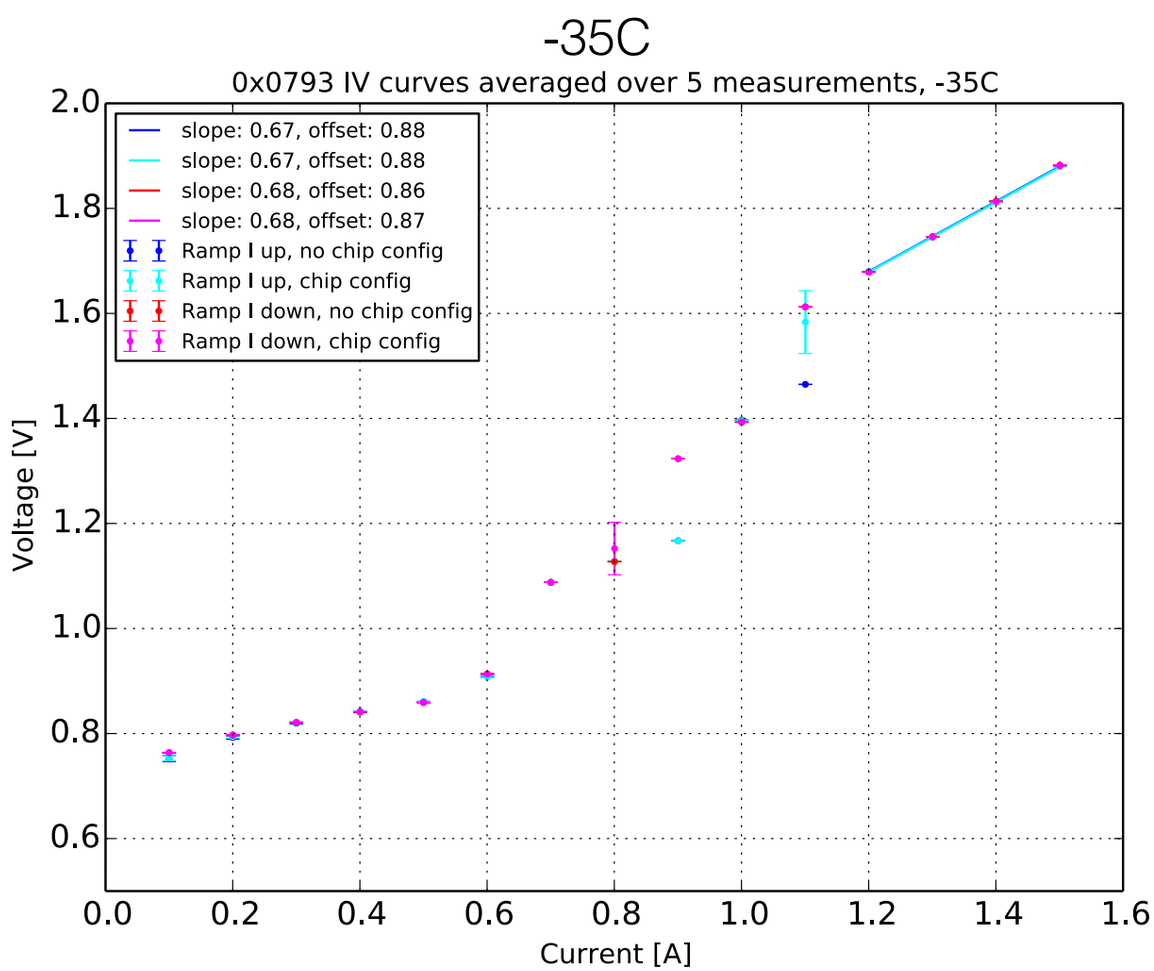
Iref (8): 4.17µA



- Iref is the reference current, usually set to 4µA

IV curve on hybrid





- Offset is about 0.88, slope is 0.67
  - Slope is steeper than for other chips
- Chip turn-on is 1.6V (warm) - 1.65V (cold): higher than for other chips
- Seems that offset resistors are ~consistent across set of chips tested
- Would want to possible change the slope resistors
- Note: could not measure Iref and trim voltages because MUX connection is not working