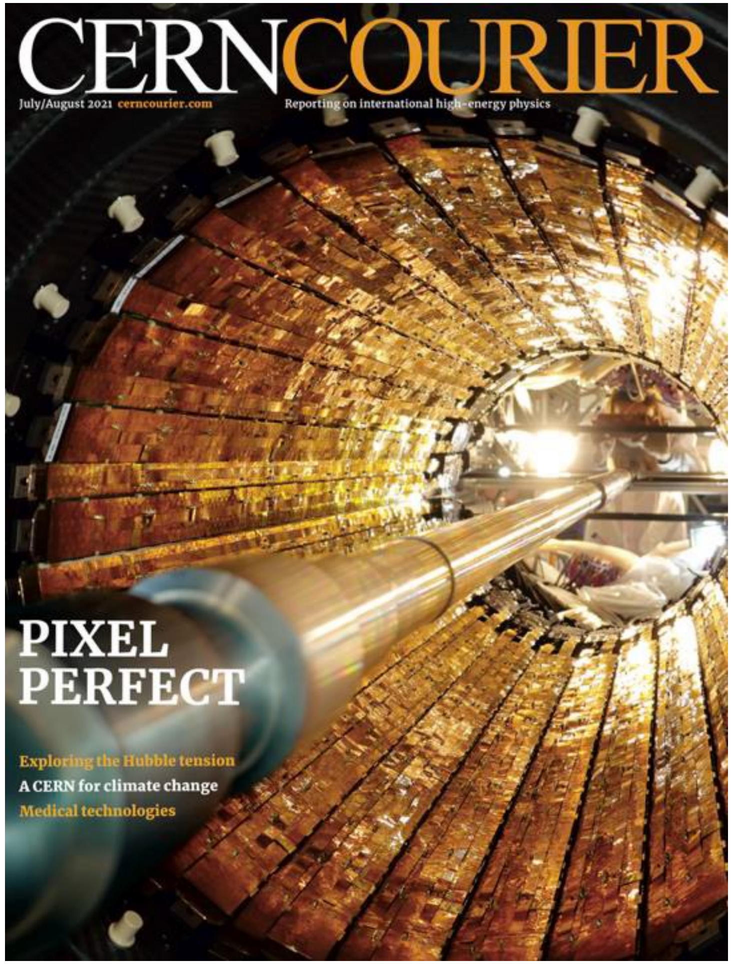
MAPS-based tracking detectors for collider experiments

Nicole Apadula

Brown Bag Instrumentation Seminar

April 23, 2024

MAPS: state-of-the-art detectors



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Exploring the Hubble tension

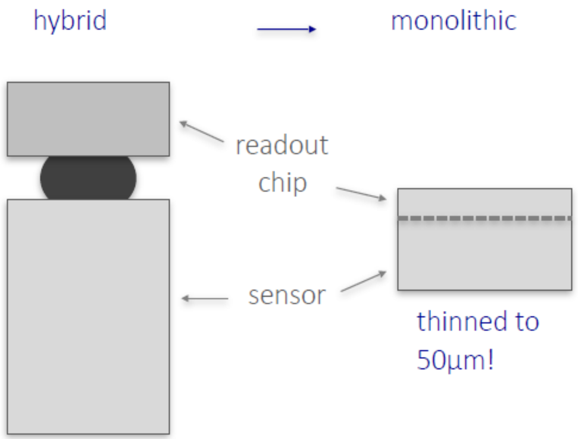
A CERN for climate change

Medical technologies

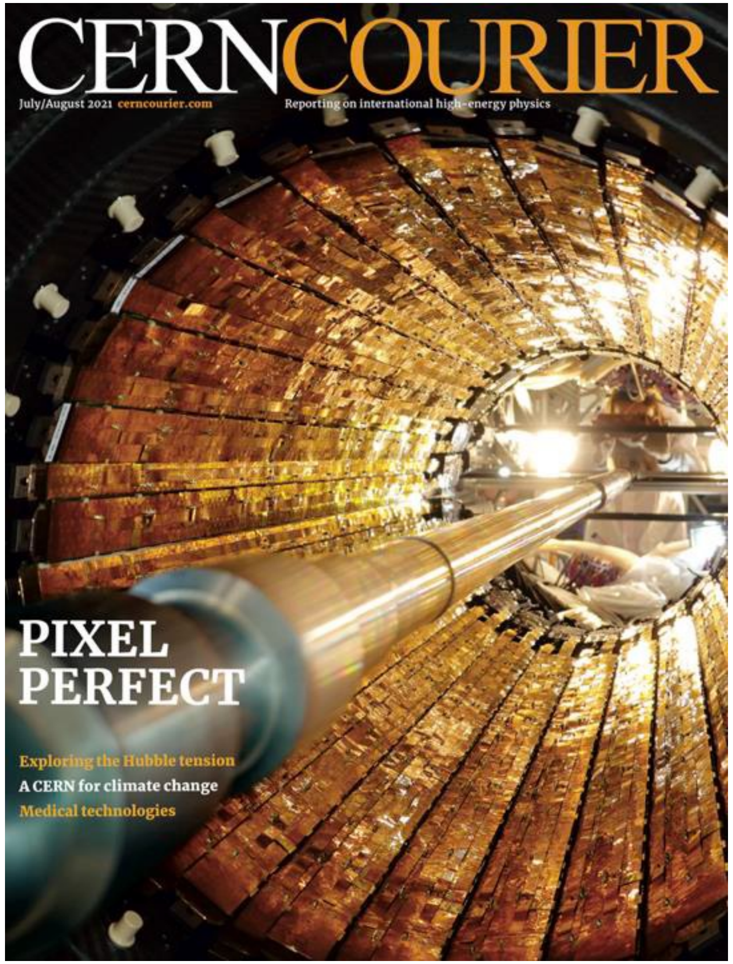
- **Pros:**
  - Good spatial resolution
  - Low material budget
  - Low power consumption
  - High efficiency

- **Limits:**
  - **Standard process**: sensitive expitaxial layer not depleted → slow response, integration time > 2 µs
  - Limited radiation hardness

Monolithic Active Pixel Sensors



MAPS: Current



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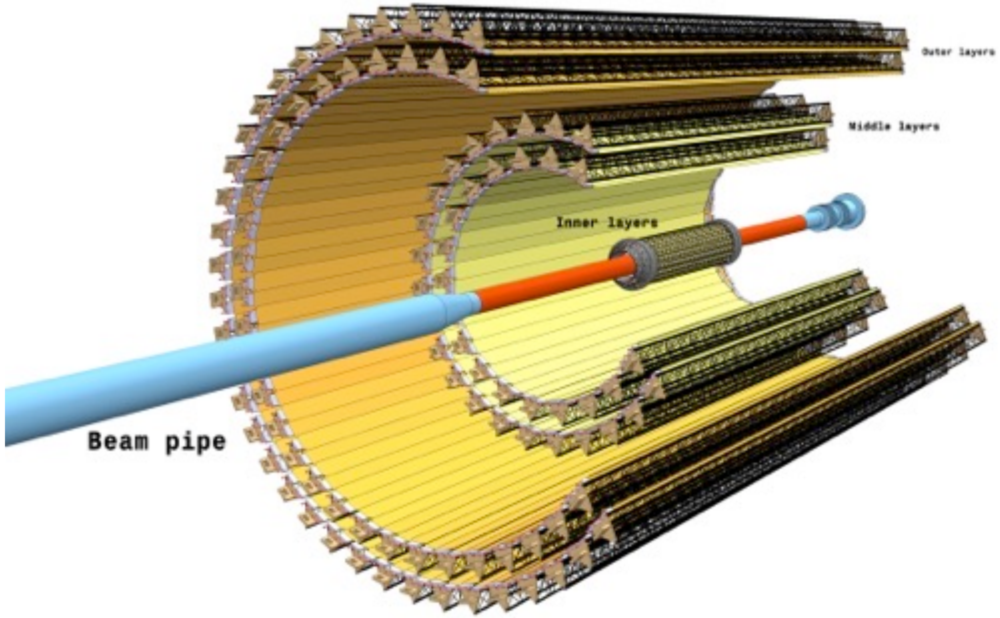
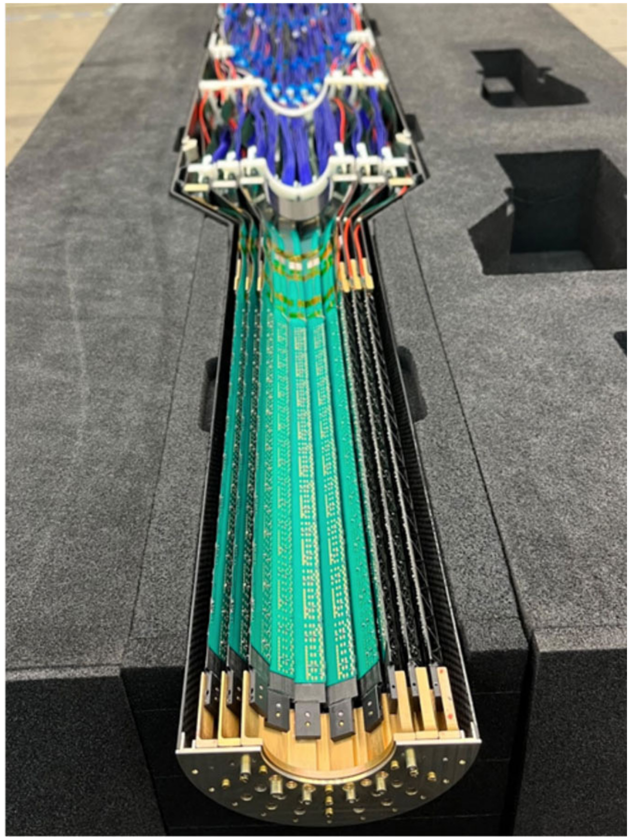
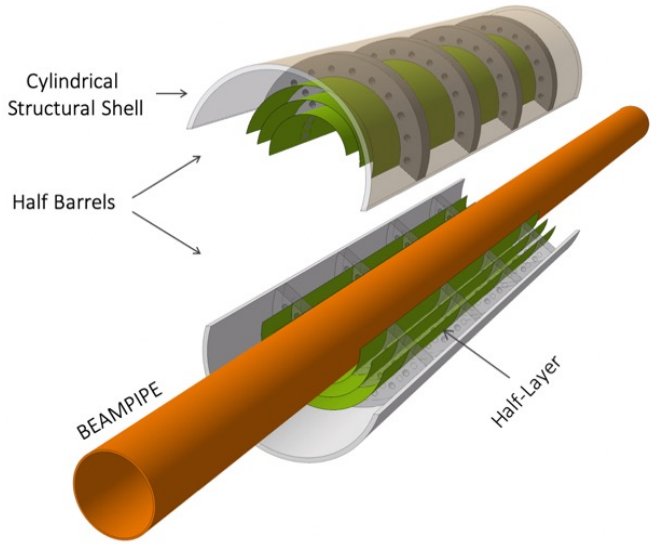
ALICE ITS2





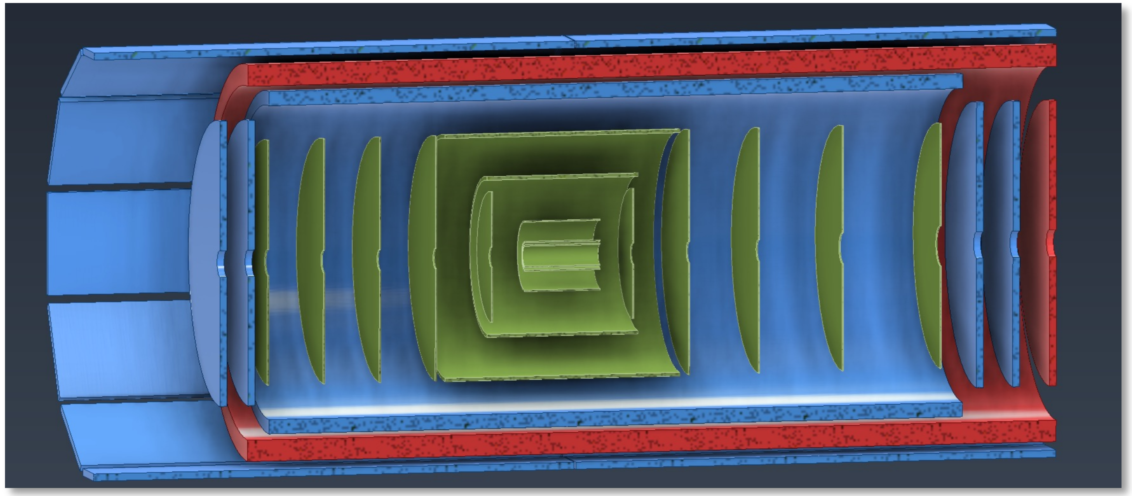
sPHENIX MVTX

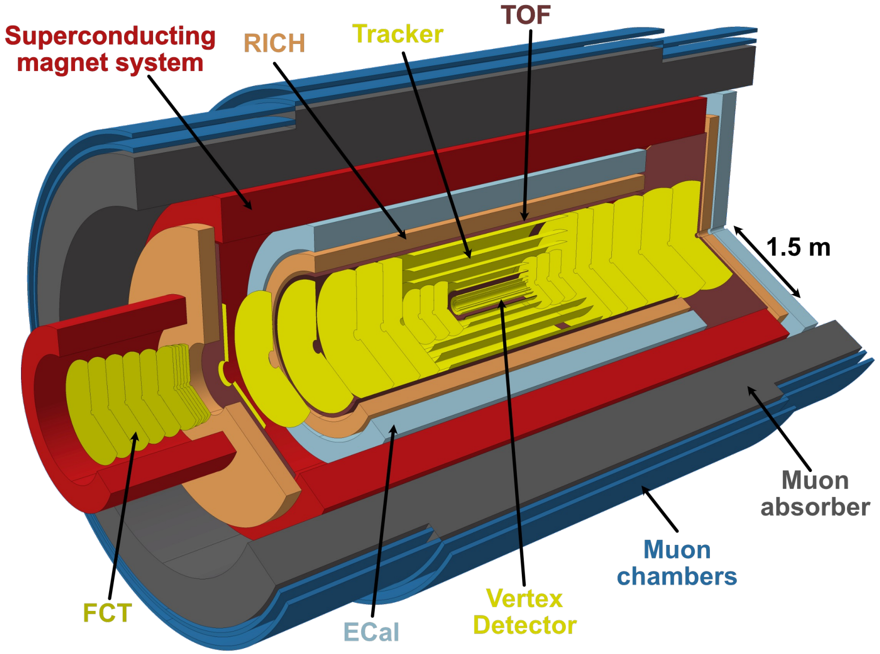
MAPS: Upcoming



ALICE ITS3
(2029)

ePIC SVT
(2032)

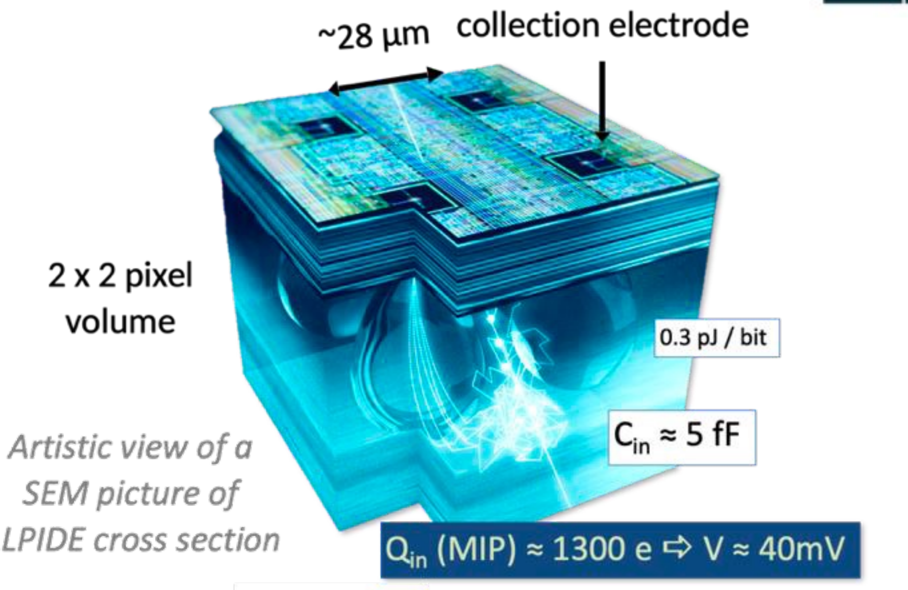




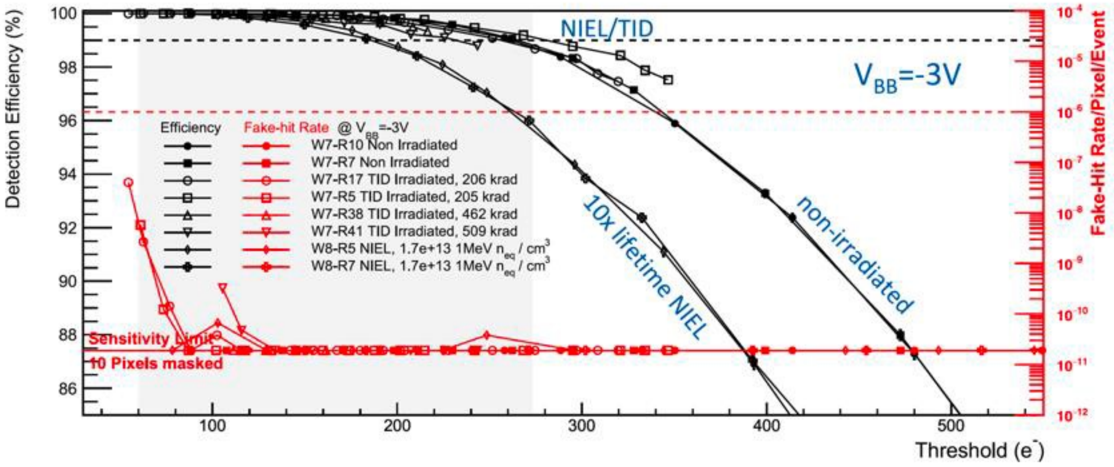
ALICE 3
(2035)

MAPS: ALPIDE

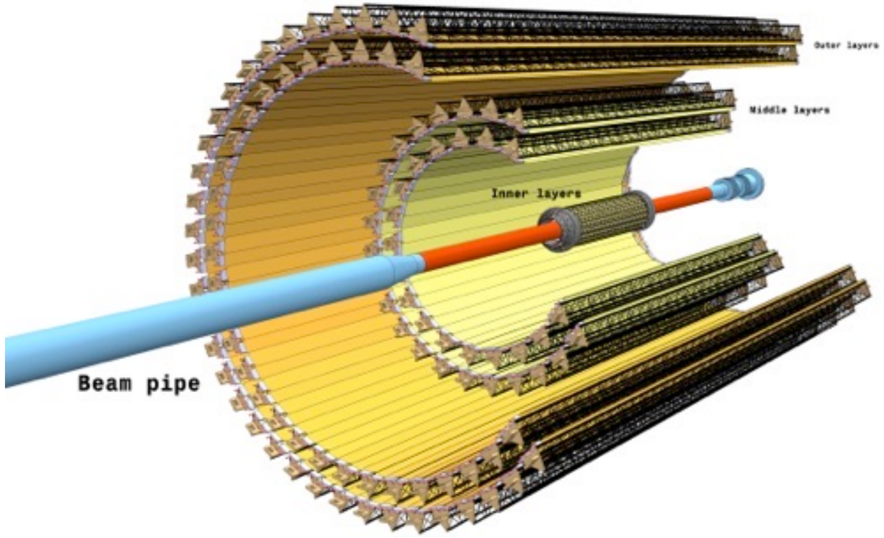
- CMOS Pixel Sensor – Tower Semiconductor 180nm
- ALPIDE Key Features
  - **In-pixel:** Amplification, Discrimination, multi-event buffer
  - **In-matrix zero suppression:** priority encoding
  - **Low power:** < 50 mW/cm^2 (<140mW full chip)
  - **Detection efficiency** > 99%
  - **Spatial Resolution** ~5 μm
  - **Low fake-hit rate:** << 10^{-6}/pixel/event (10^{-8}/pixel/event measured in data taking)
  - **Radiation tolerance:** > 270 krad (TID), 1.7 10^{13} 1 MeV/neq (NIEL)



Artistic view of a SEM picture of ALPIDE cross section

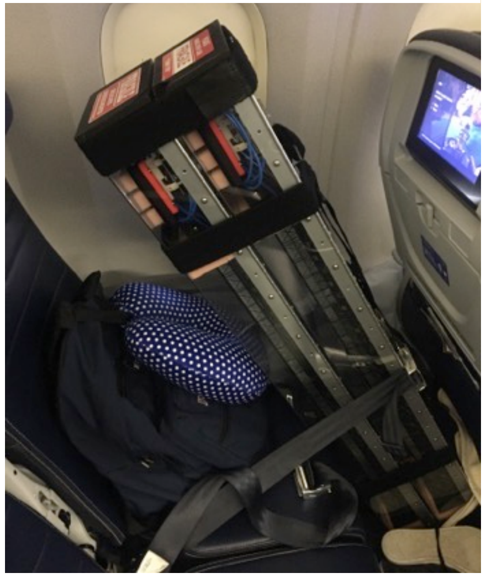


ALICE ITS2

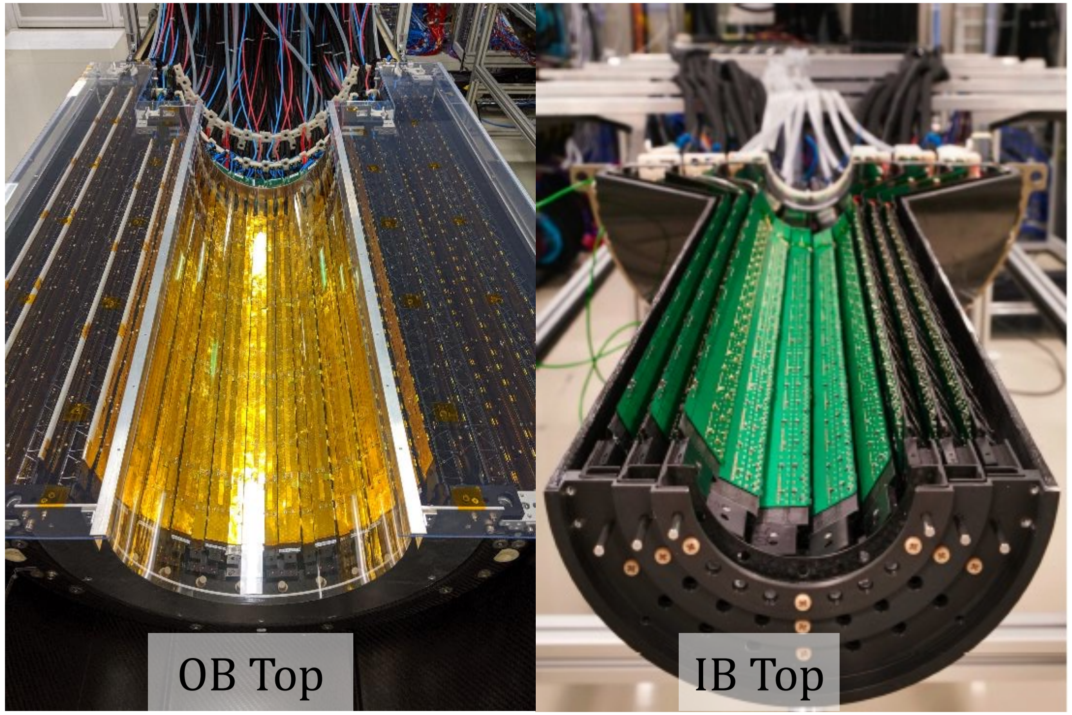


ITS2: 7 layers
~10 m^2 Si
Built at 11 sites over
2+ years

64 staves built
& delivered by
LBNL



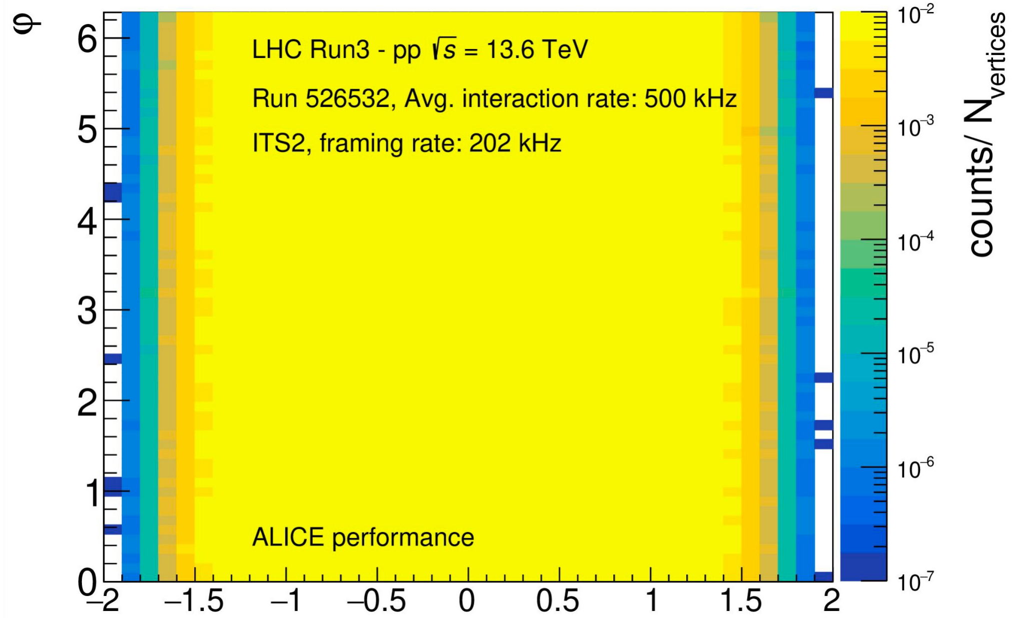
Installed 2020



~72000 chips (65% yield)
~2600 modules (85% yield)
~280 staves (95% yield)

ITS2 in LHC Run 3

- Online tracking quick data QA
- Good quality of **angular distribution of tracks**



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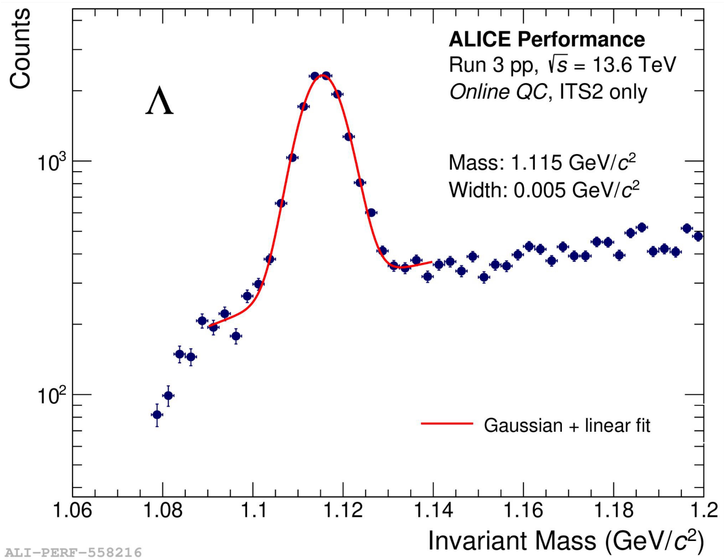
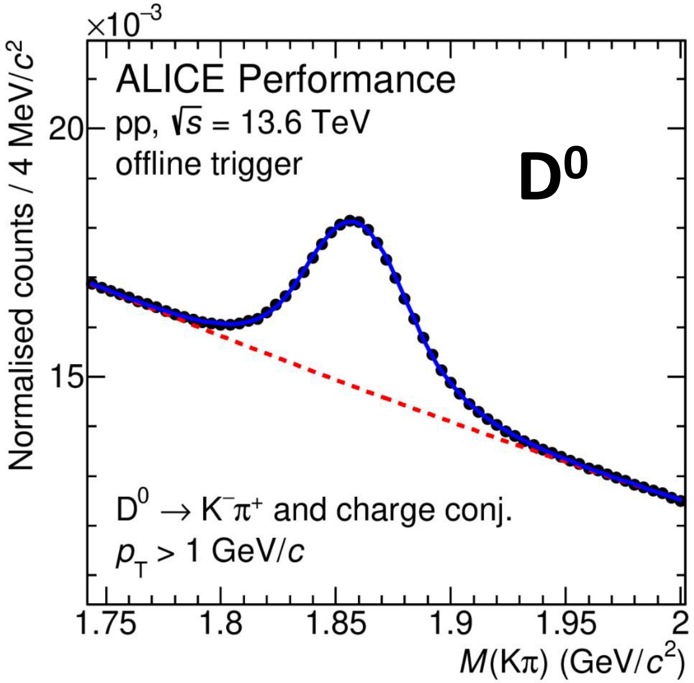
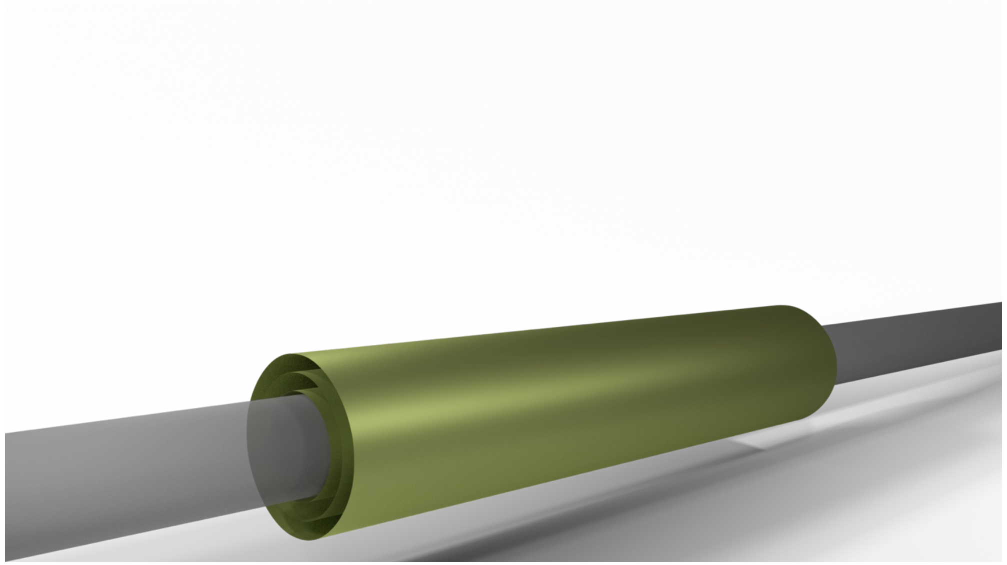


ALI−PERF−558216



- **Online physics performance QA:** Λ invariant mass peaks from ITS2 standalone tracks
- First **charm meson** measurements with Run 3 pp data (13 TeV)

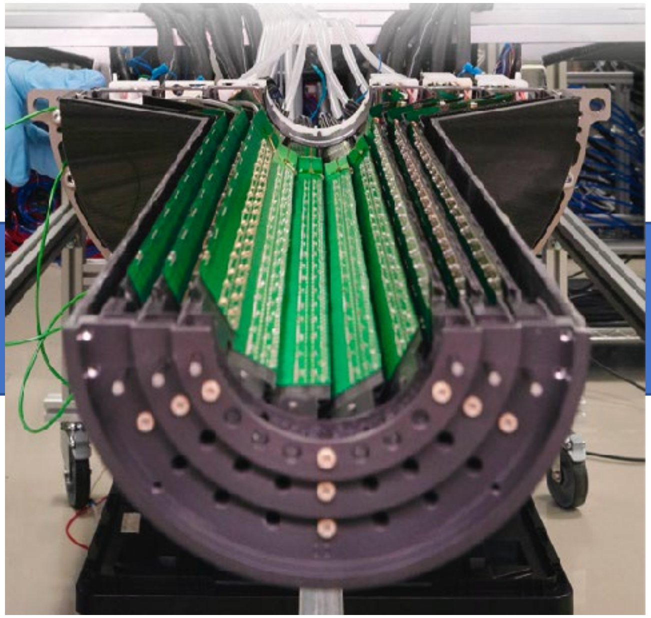


What comes next?

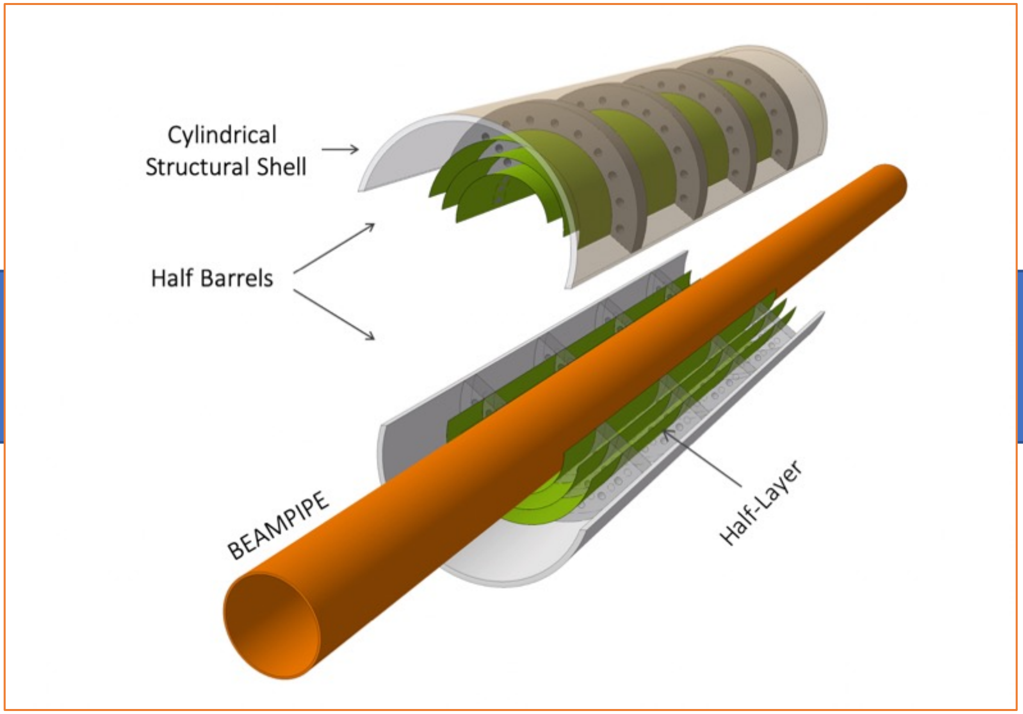
ITS3: Thinner & closer to the beam pipe

ITS3 Detector Layout

Replace during LS3



with

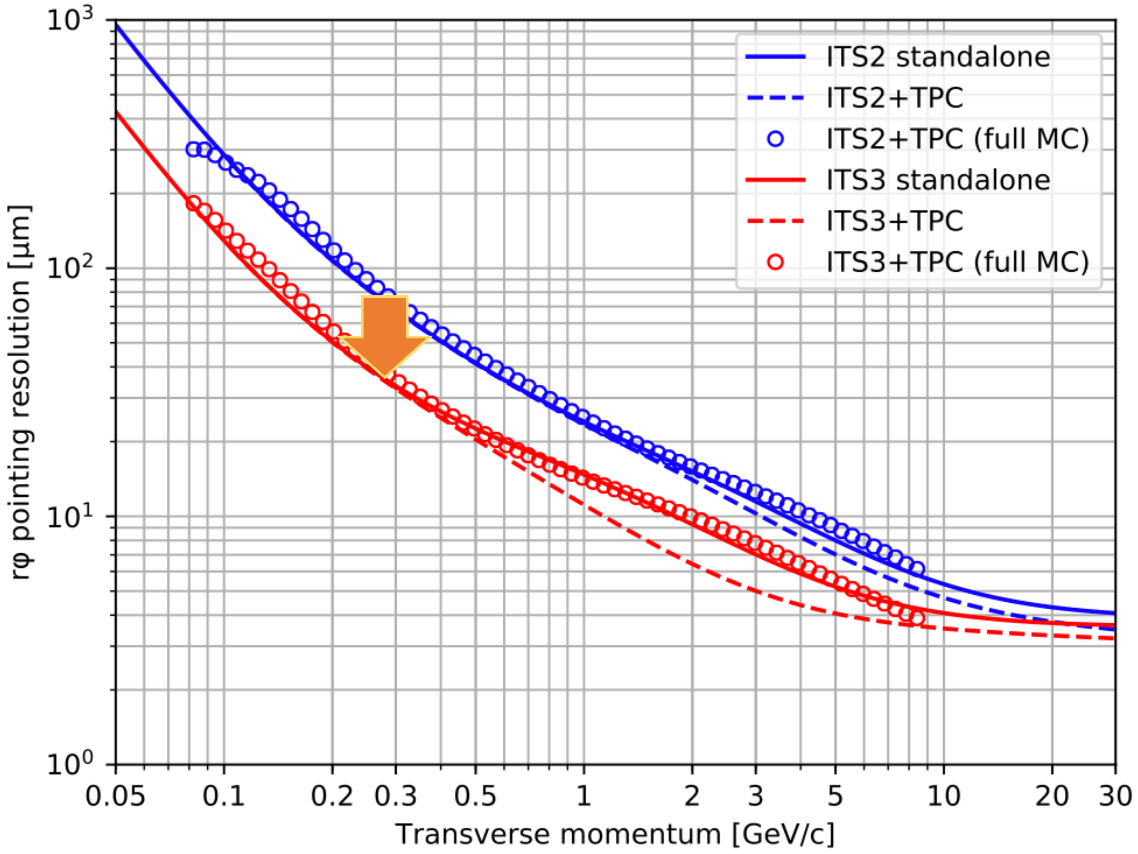


Improve pointing resolution
- Closer to the beam pipe: 23 mm → 18 mm

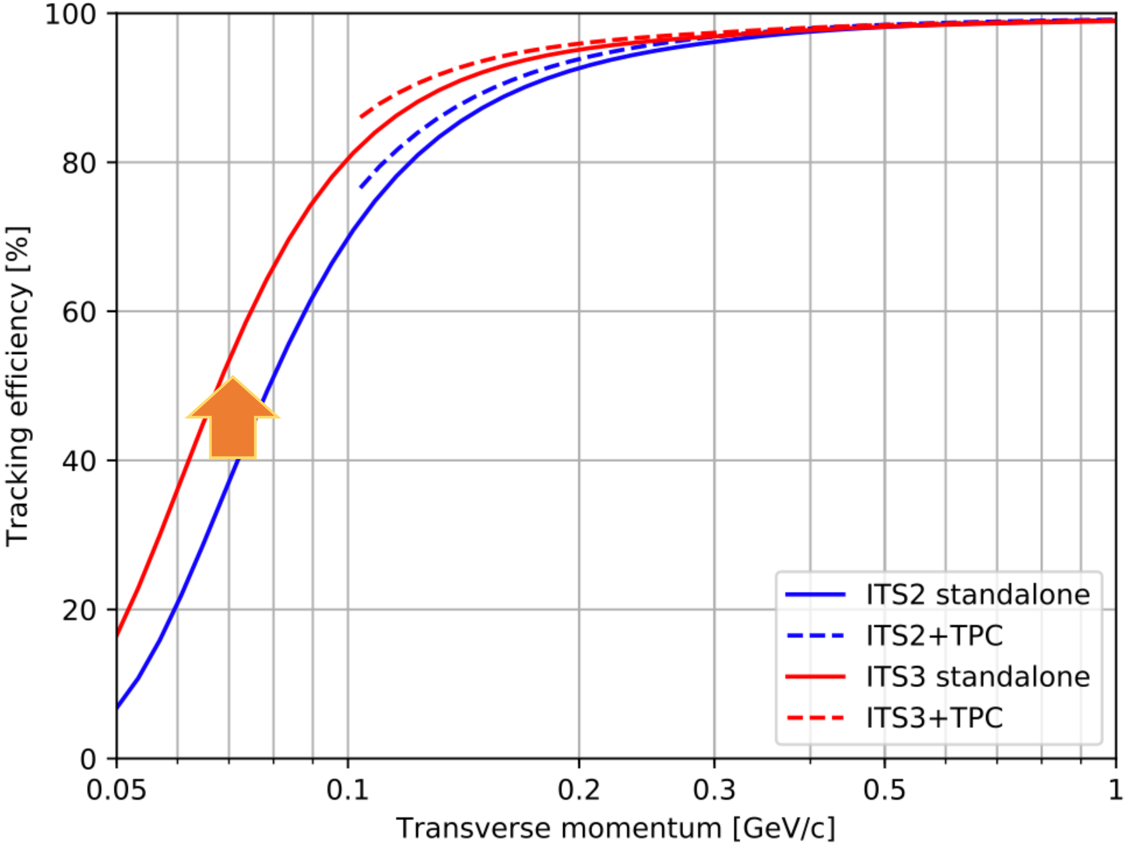
Better tracking resolution (especially at low p_T)
- Less material: 0.3% X_0 → ~0.05% X_0

MAPS sensors
- Wafer-scale (up to ~28 x 10 cm)
- Ultra-thin (20 – 40 μm)
- Bent (R = 18, 24, 30 mm)

Improvement with ITS3 over ITS2



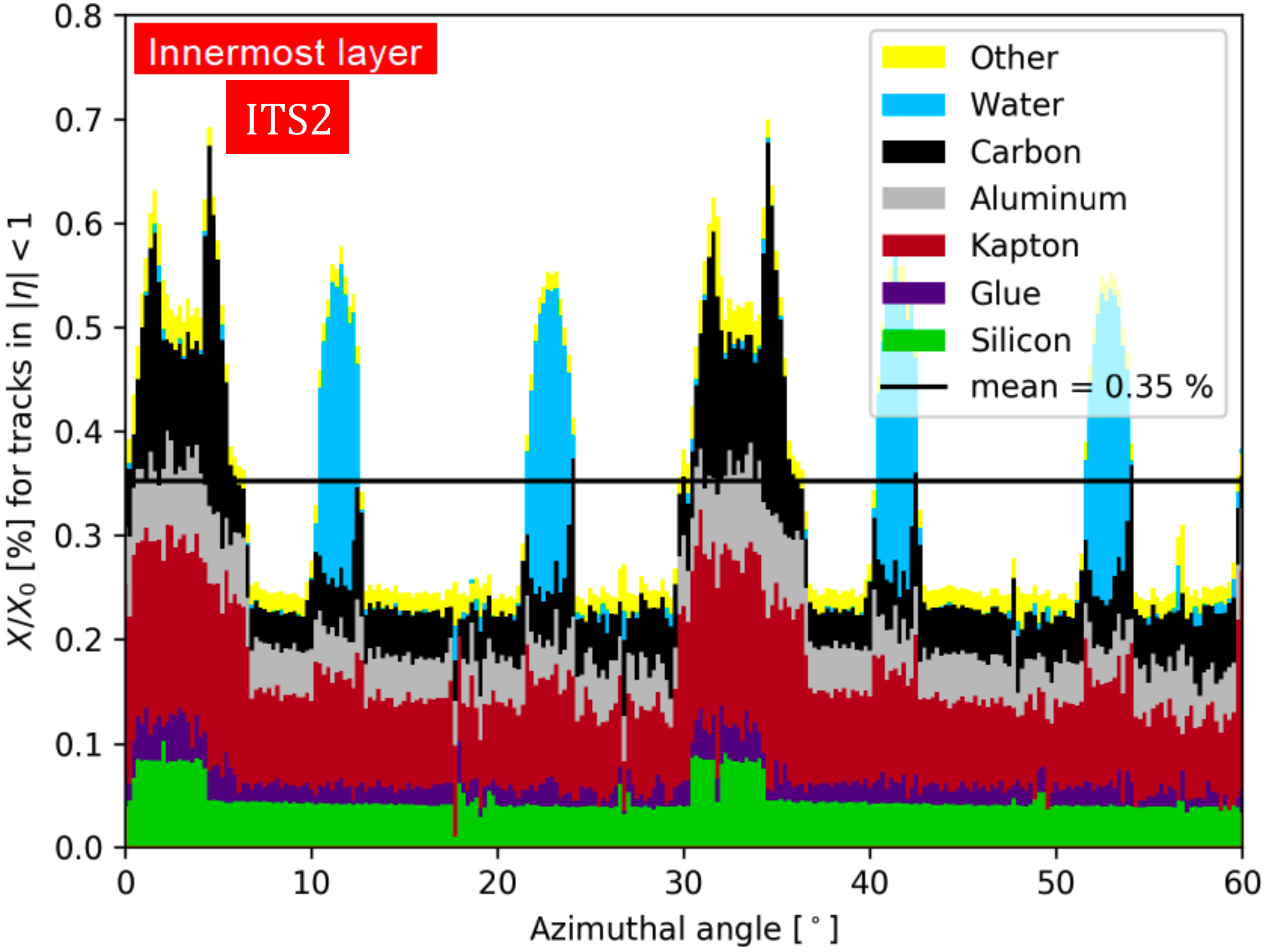
ALICE-PUBLIC-2018-013



Pointing Resolution 2x better

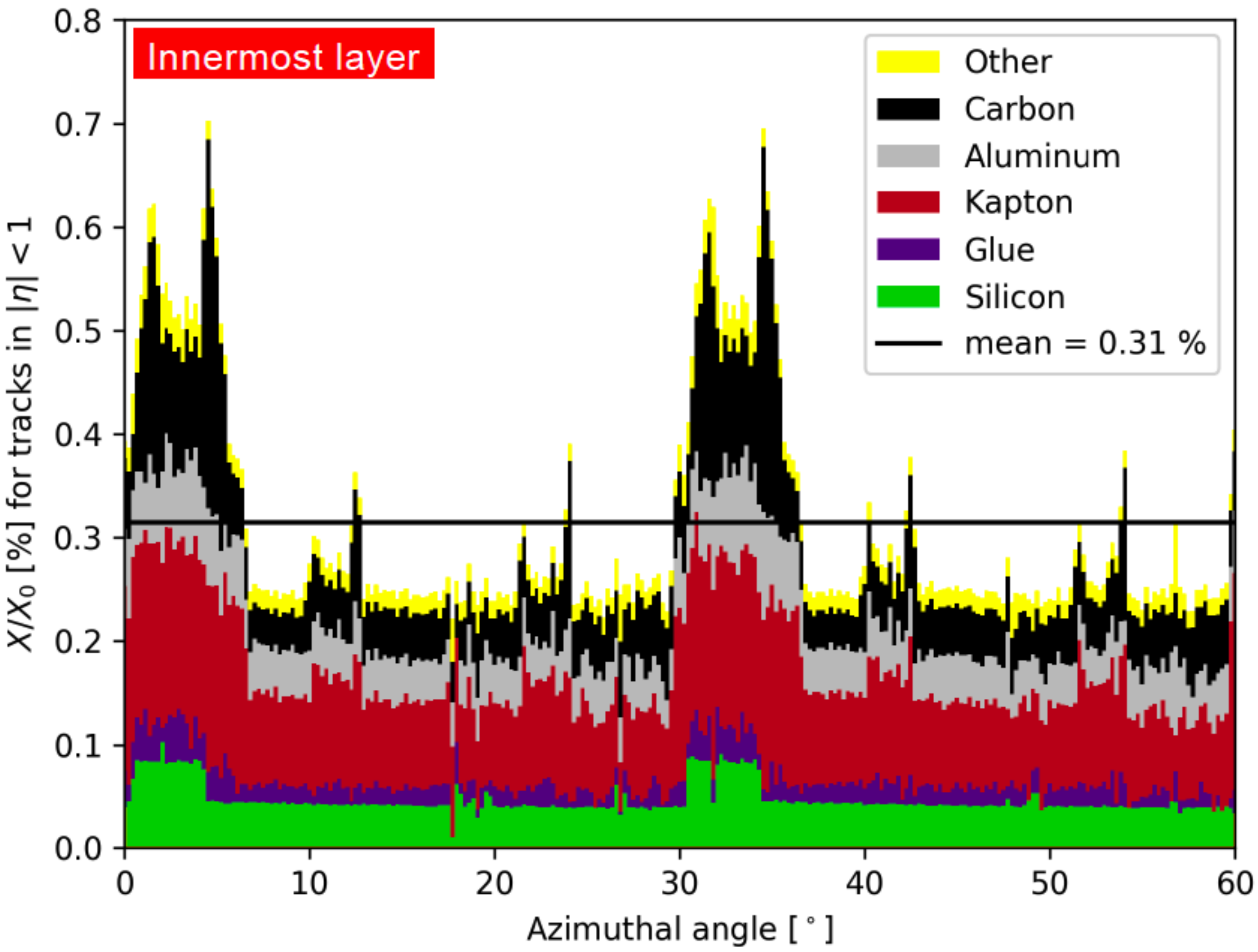
Improved tracking efficiency for low p_T

How?→Reduce Material Budget



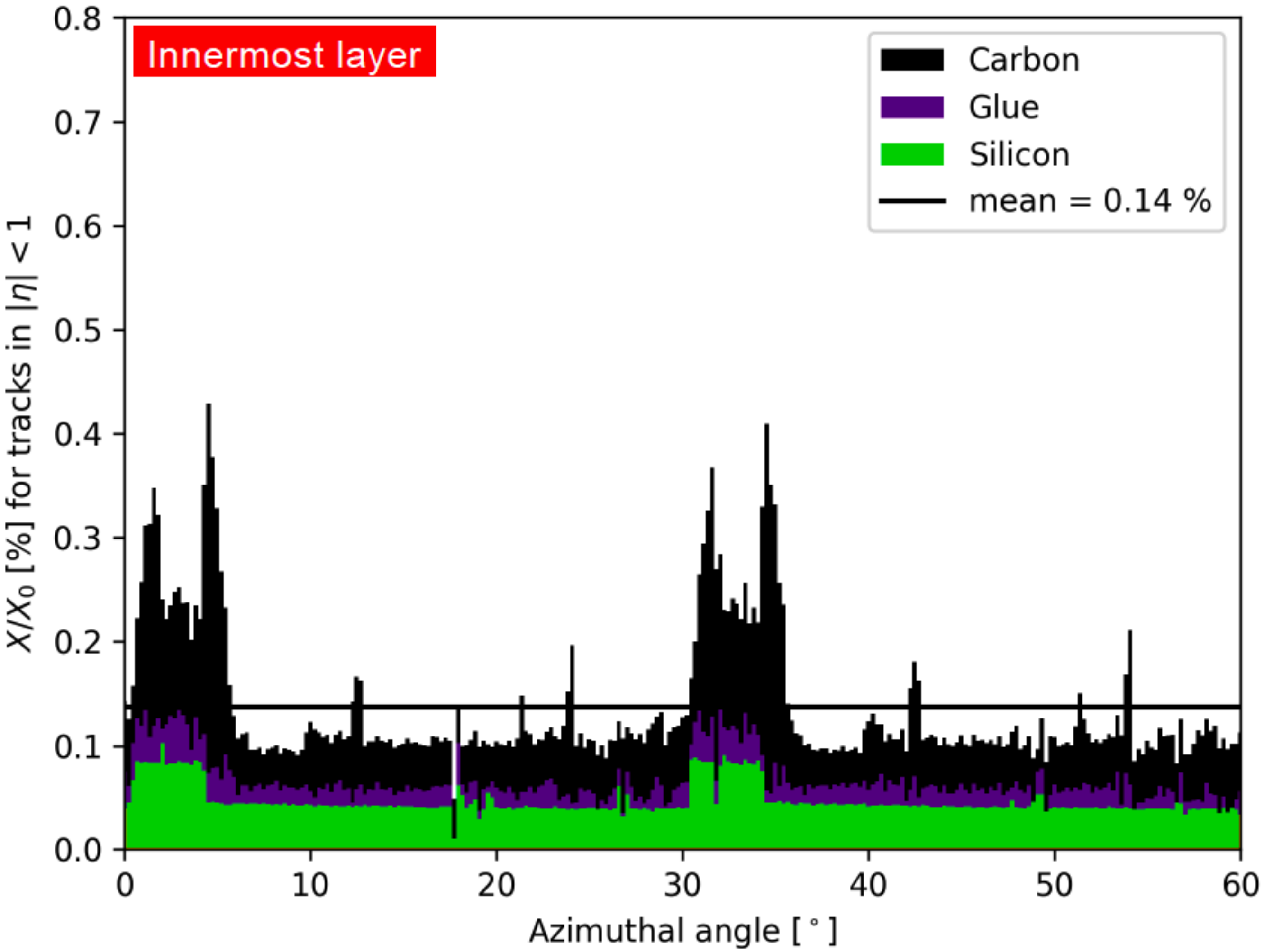
- Observations:
  - Silicon makes up ~15% of total material
  - Irregularities due to support, cooling, & overlap

How?→Reduce Material Budget



- Observations:
  - Silicon makes up ~15% of total material
  - Irregularities due to support, cooling, & overlap
- Remove water cooling
  - If power consumption low enough

How?→Reduce Material Budget



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- Remove circuit board for power & data
  - If integrated on chip

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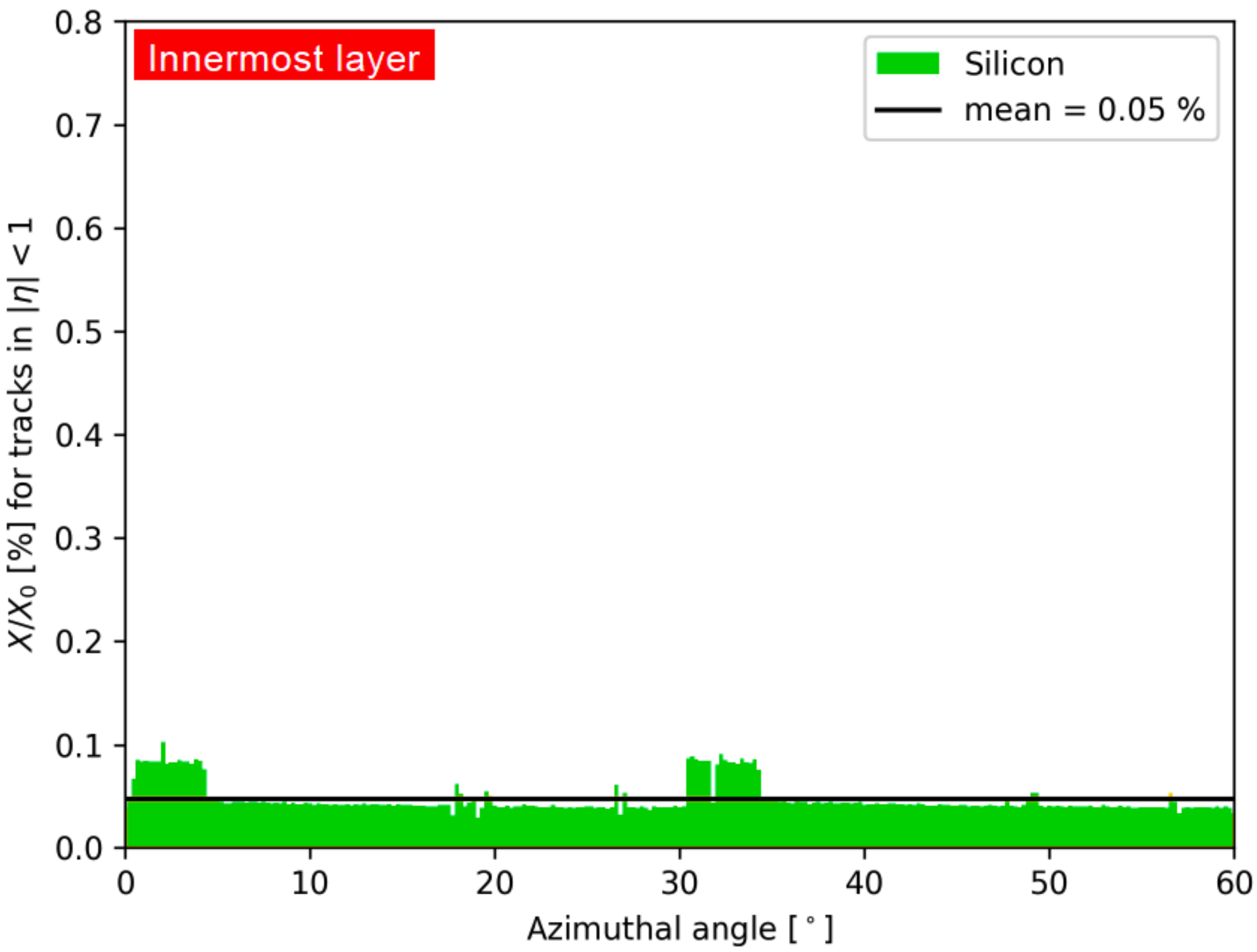
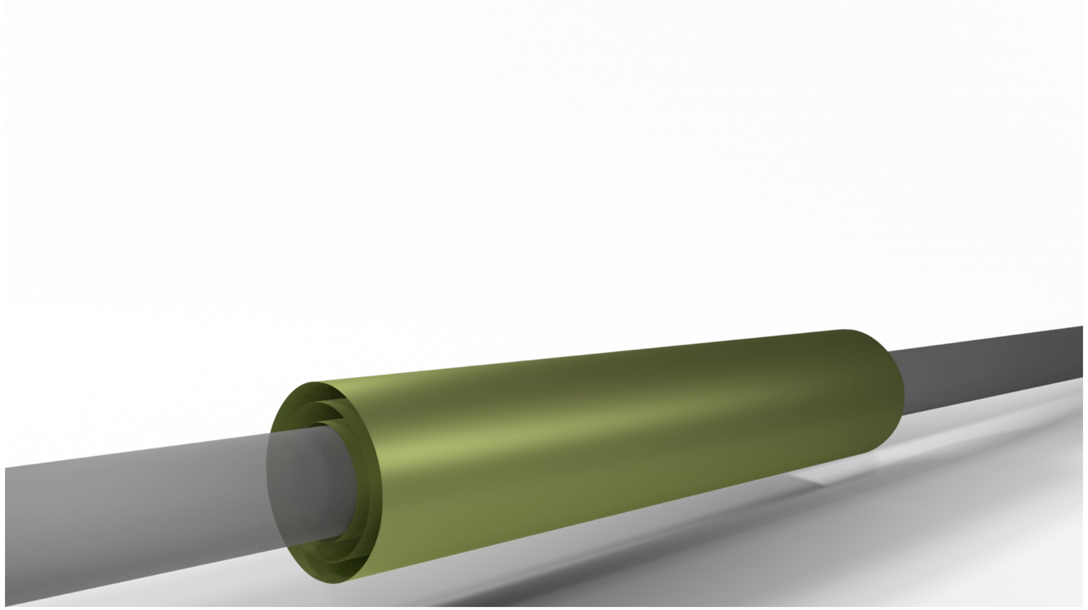
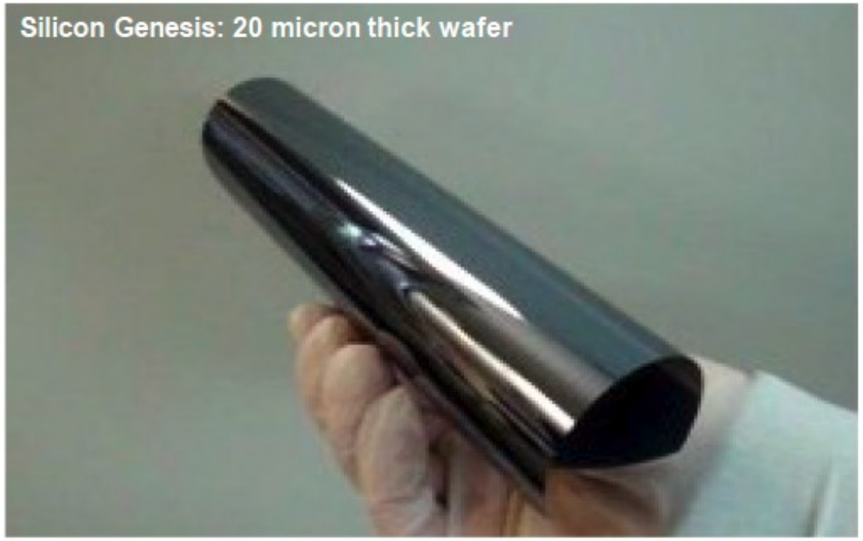


- Observations:
  - Silicon makes up ~15% of total material
  - Irregularities due to support, cooling, & overlap
- Remove water cooling
  - If power consumption low enough
- Remove circuit board for power & data
  - If integrated on chip
- Remove mechanical support
  - Self-supporting arched structure from rolling Si wafers

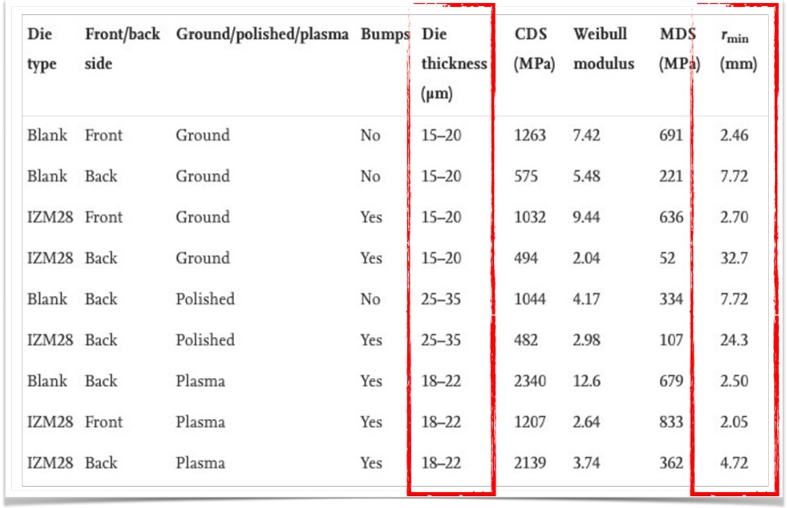
Thinning & Bending Silicon



- Below 50 µm, Si wafers become flexible, “paper-like”
- Bending Si wafers + circuits is possible & has been tried
  - Radii much smaller than needed have been achieved



Silicon Genesis: 20 micron thick wafer

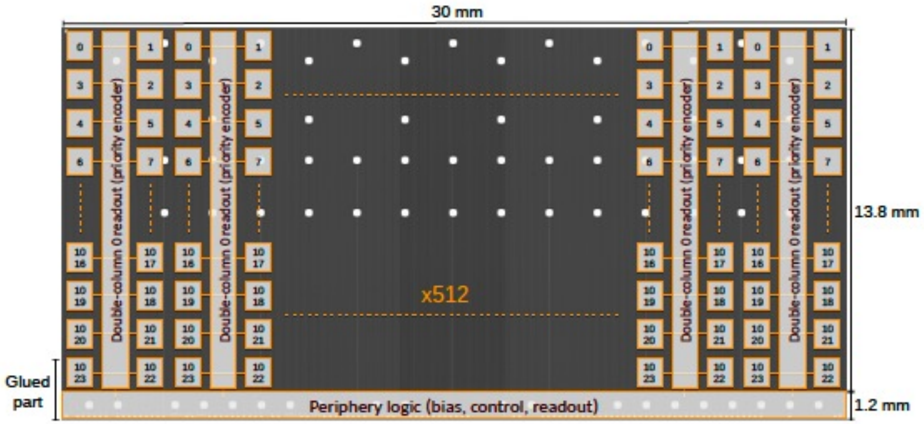


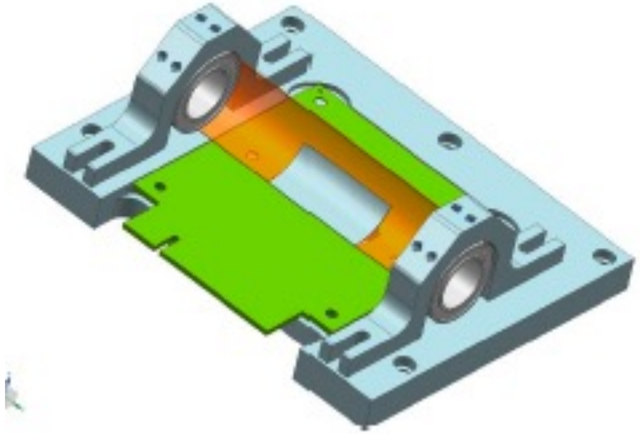
Die type	Front/back side	Ground/polished/plasma	Bumps	Die thickness (µm)	CDS (MPa)	Weibull modulus	MDS (MPa)	r_{min} (mm)
Blank	Front	Ground	No	15–20	1263	7.42	691	2.46
Blank	Back	Ground	No	15–20	575	5.48	221	7.72
IZM28	Front	Ground	Yes	15–20	1032	9.44	636	2.70
IZM28	Back	Ground	Yes	15–20	494	2.04	52	32.7
Blank	Back	Polished	No	25–35	1044	4.17	334	7.72
IZM28	Back	Polished	Yes	25–35	482	2.98	107	24.3
Blank	Back	Plasma	Yes	18–22	2340	12.6	679	2.50
IZM28	Front	Plasma	Yes	18–22	1207	2.64	833	2.05
IZM28	Back	Plasma	Yes	18–22	2139	3.74	362	4.72

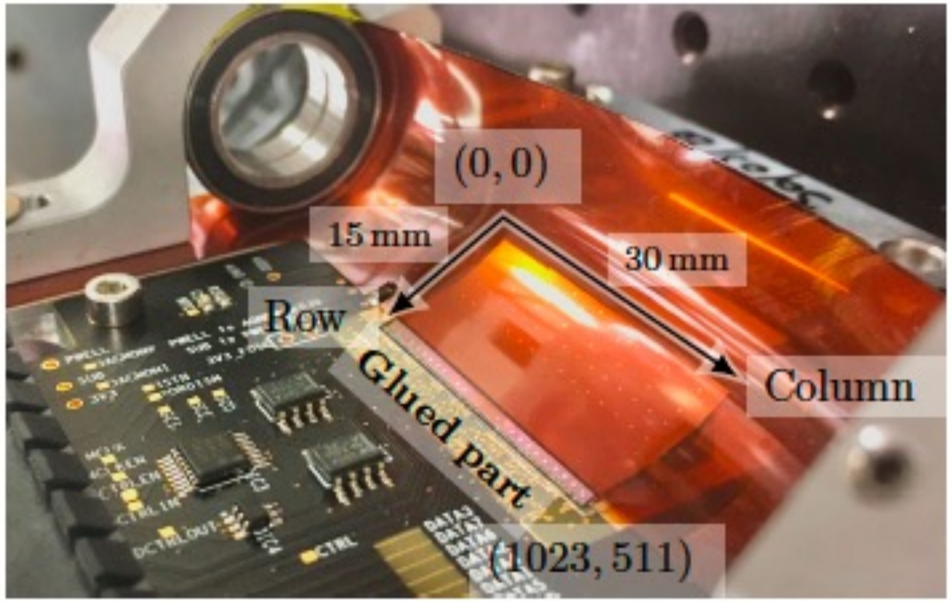
D.A. van den Ende et al., Microelectronics Reliability, vol. 54, pp. 2860-2870, 2014
http://dx.doi.org/10.1016/j.microrel.2014.07.125

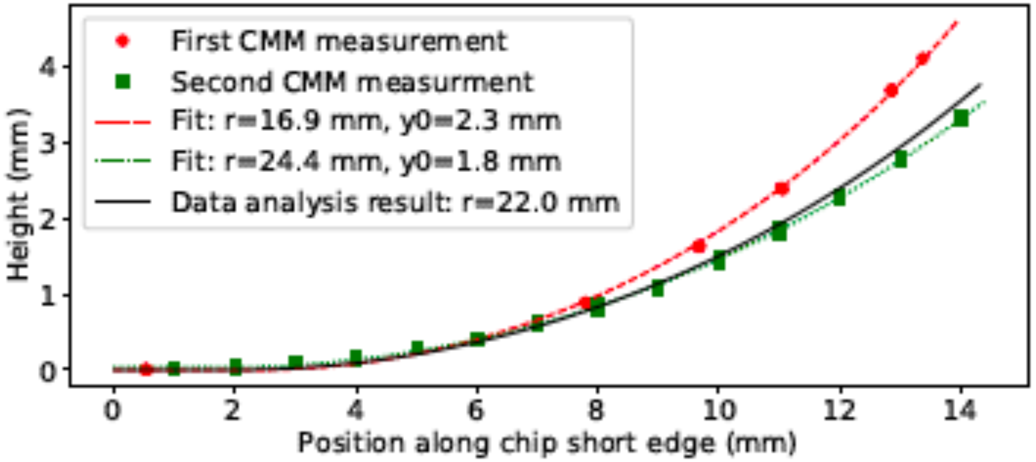
Testing bent silicon with ALPIDE

- Bent along short side
  - Affects pixel matrix only
  - Bonding area is glued
    - Flat & secured

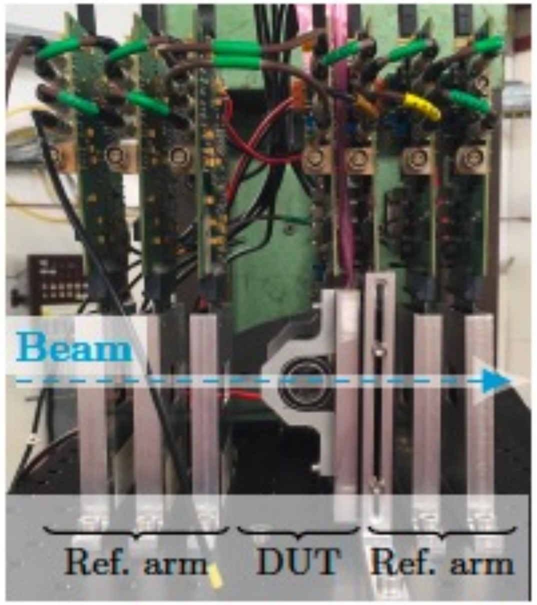






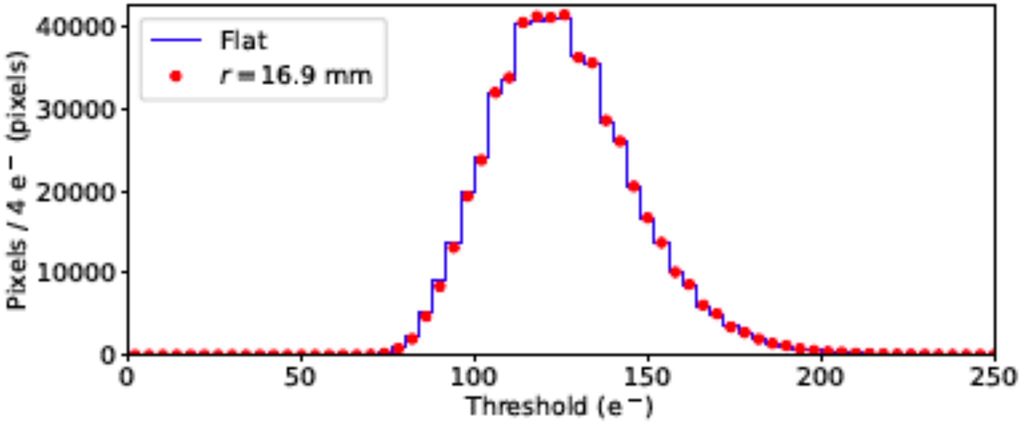


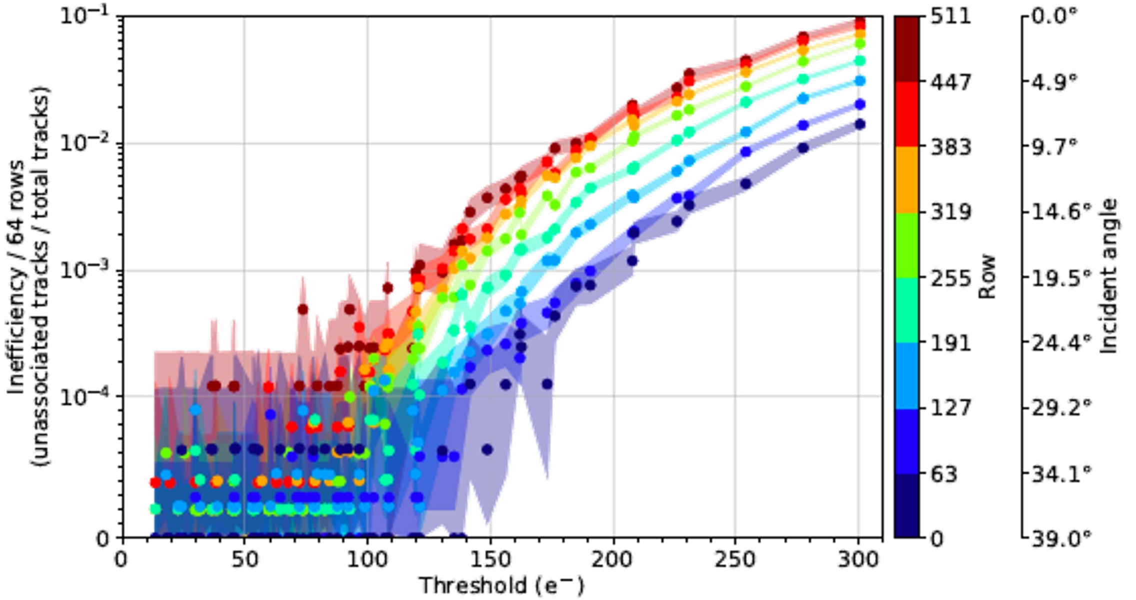
Bent ALPIDE in beam test



DESY
5.4 GeV e^-

- Curvature effect not noticeable on:
  - **Pixel thresholds, FHR, pixel responsiveness**
- Difference between pixel threshold negligible before and after bending
- Below threshold of 100 e^- (~operating point) inefficiency < 10^{-4}

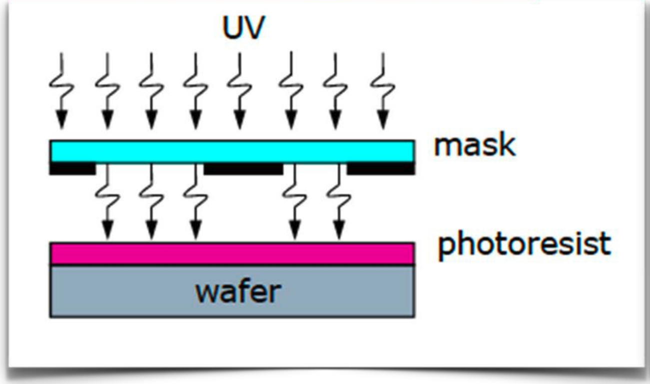




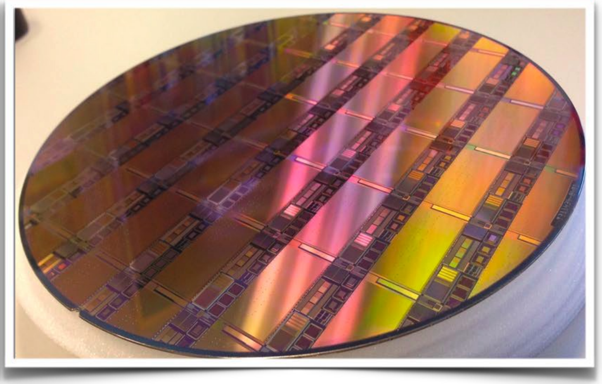
Wafer-scale Chip

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - ~ few cm^2
  - Modules → chips tiled & connected to flexible printed circuit board

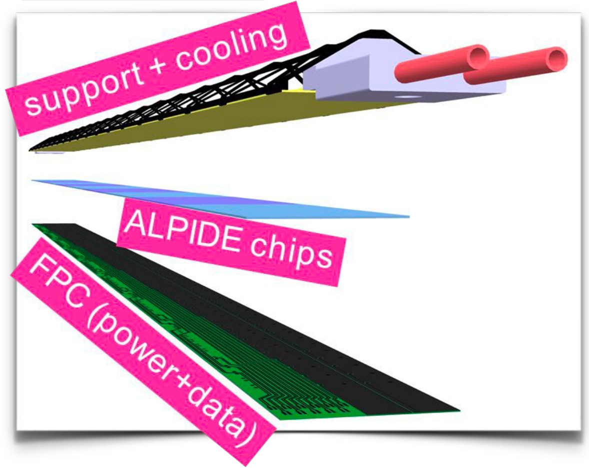
Principle of photolithography



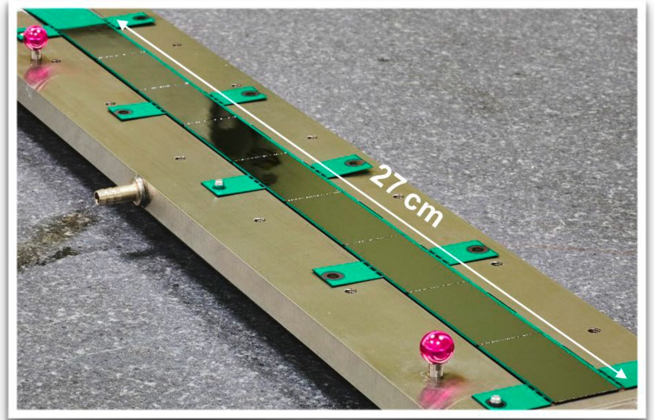
200 mm ALPIDE prototype wafer



Stave design



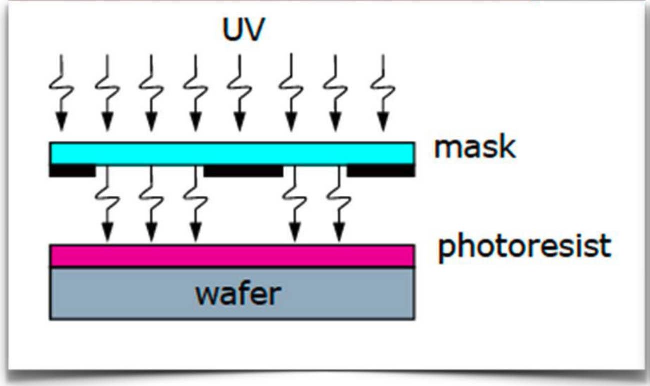
FPC + chips



Wafer-scale Chip

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
    - ~ few cm^2
    - Modules → chips tiled & connected to flexible printed circuit board
- New option: **stitching**, i.e. aligned exposures of a reticle to produce larger circuits
    - Actively used in industry
    - Requires dedicated chip design
- Switch to **65 nm CMOS process**
    - 200 mm wafer (ALPIDE, 180 nm CMOS) → 300 mm wafer (65 nm)

Principle of photolithography



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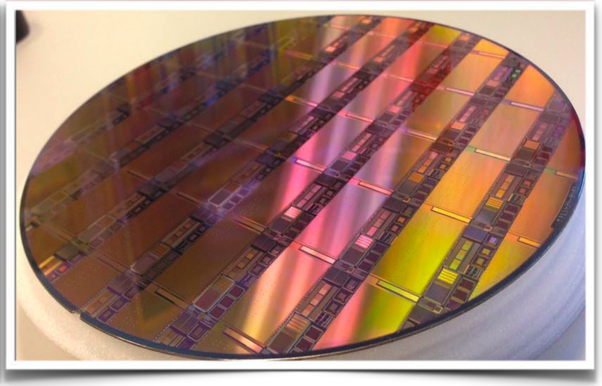
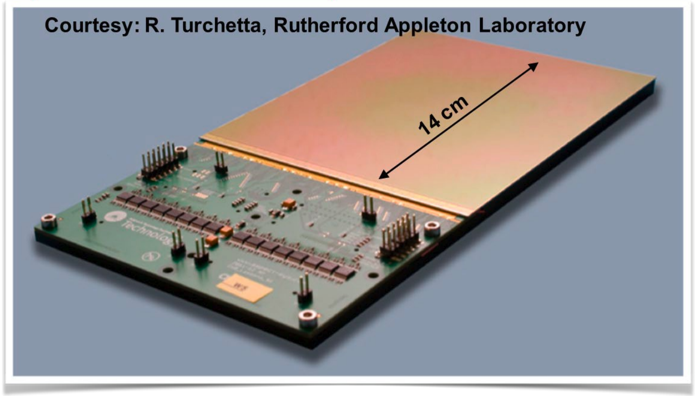


Wafer-scale sensor

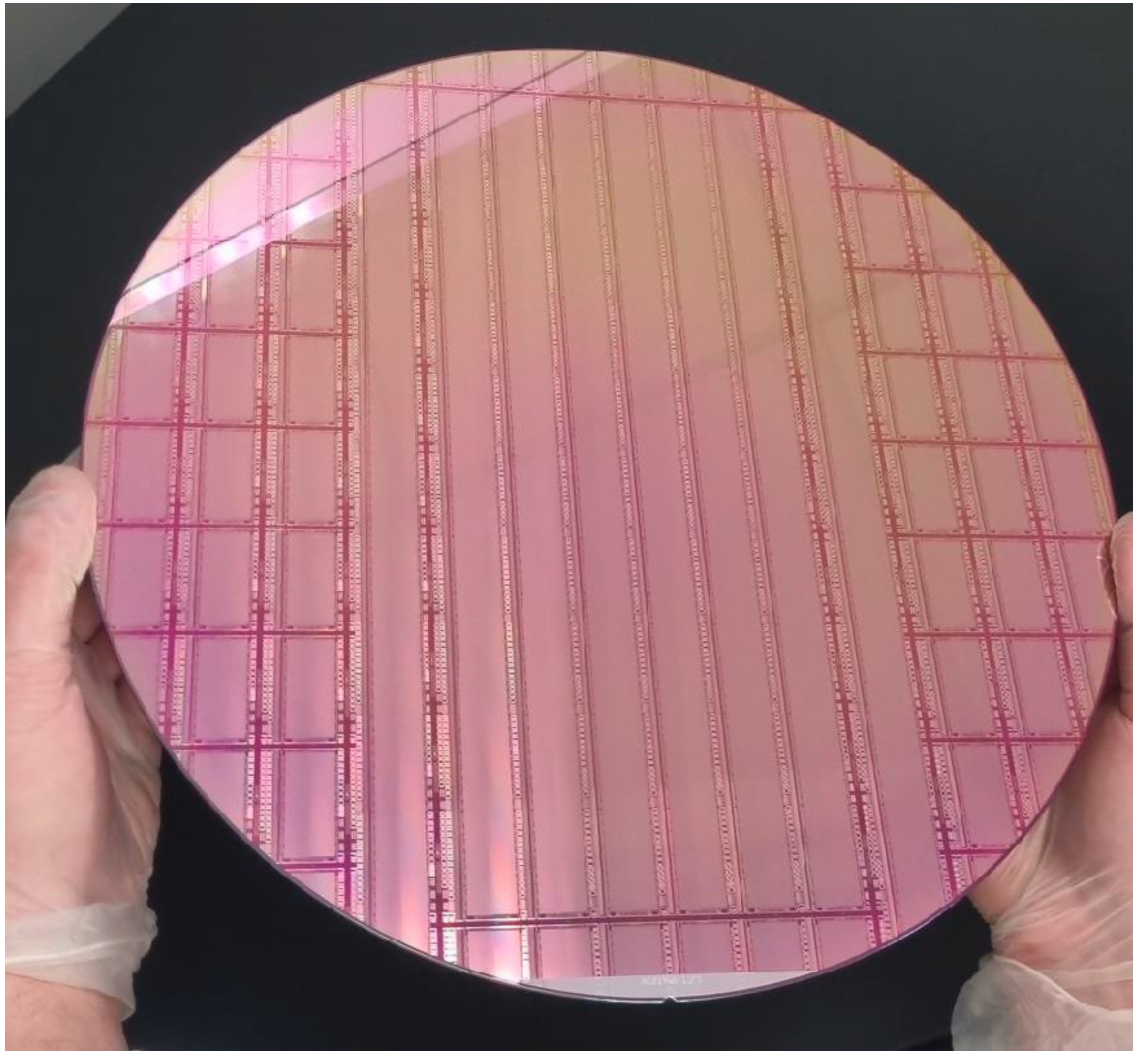


Courtesy: R. Turchetta, Rutherford Appleton Laboratory

180 nm → 65 nm

Large area 65 nm chip development

- **MLR1 (2021):**
  - verification of 65 nm technology. Large number of test structures
- **ER1 (2023): first stitched MAPS**
  - Large design exercise, proof of stitching principles, learning methodology & yield
- **ER2 (submission end of 2024):** first ITS3 sensor prototype
- **ER3 (submission end of 2025):** ITS3 sensor production



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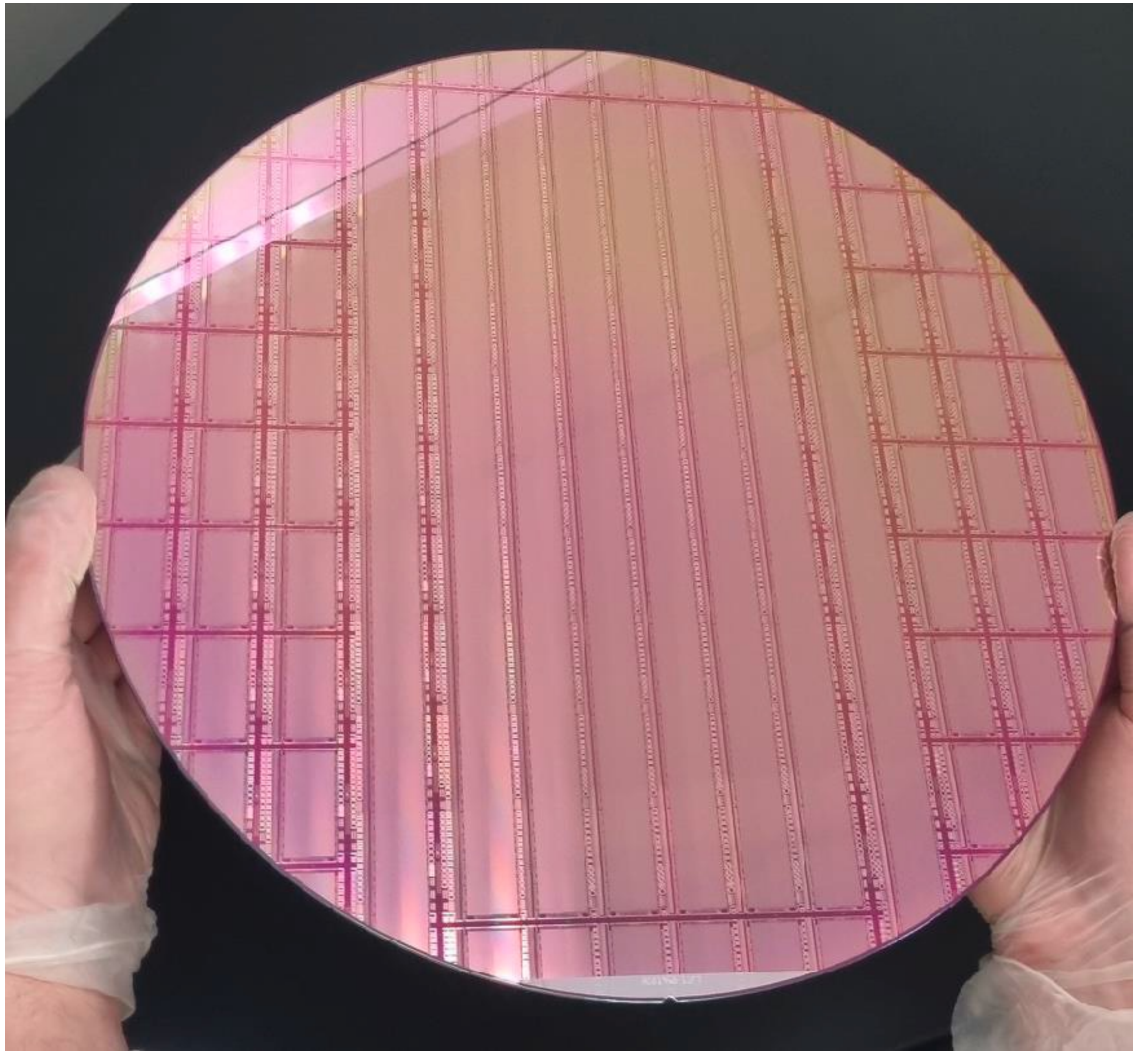
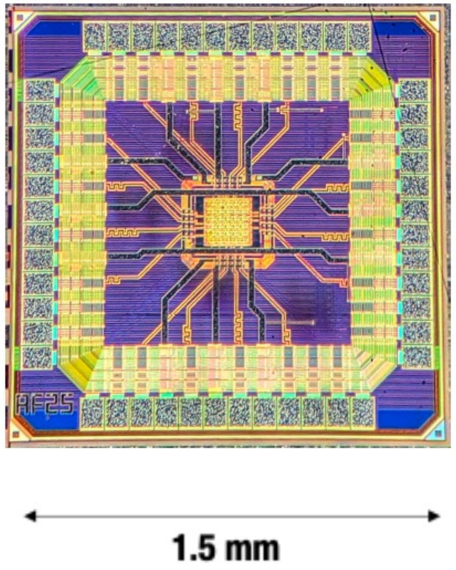


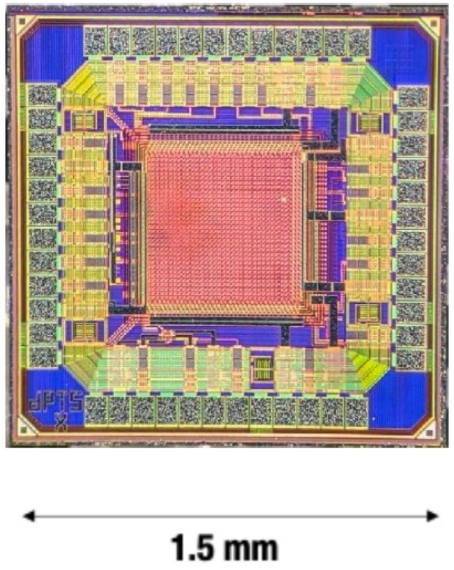
MLR1

APTS Analogue Pixel Test Structure



Matrix: 6x6
Readout: analogue readout of 4x4
Pitch: 10,15,20,25 µm
Process: all 3 variants

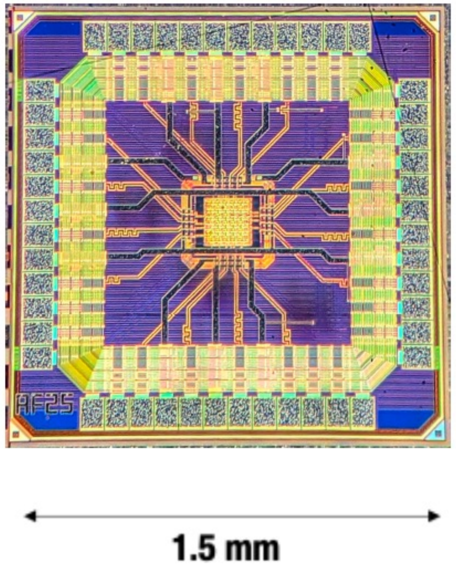
DPTS Digital Pixel Test Structure



Matrix: 32x32
Readout: async. digital with ToT
Pitch: 15 µm
Process: 1 variant (modified with gap process)

MLR1

APTS Analogue Pixel Test Structure



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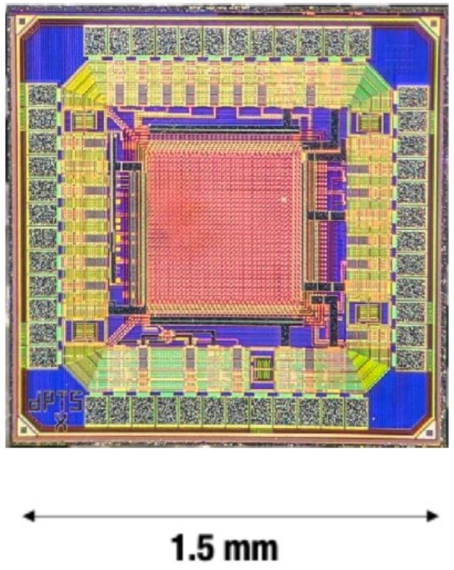

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Pitch: 15 µm
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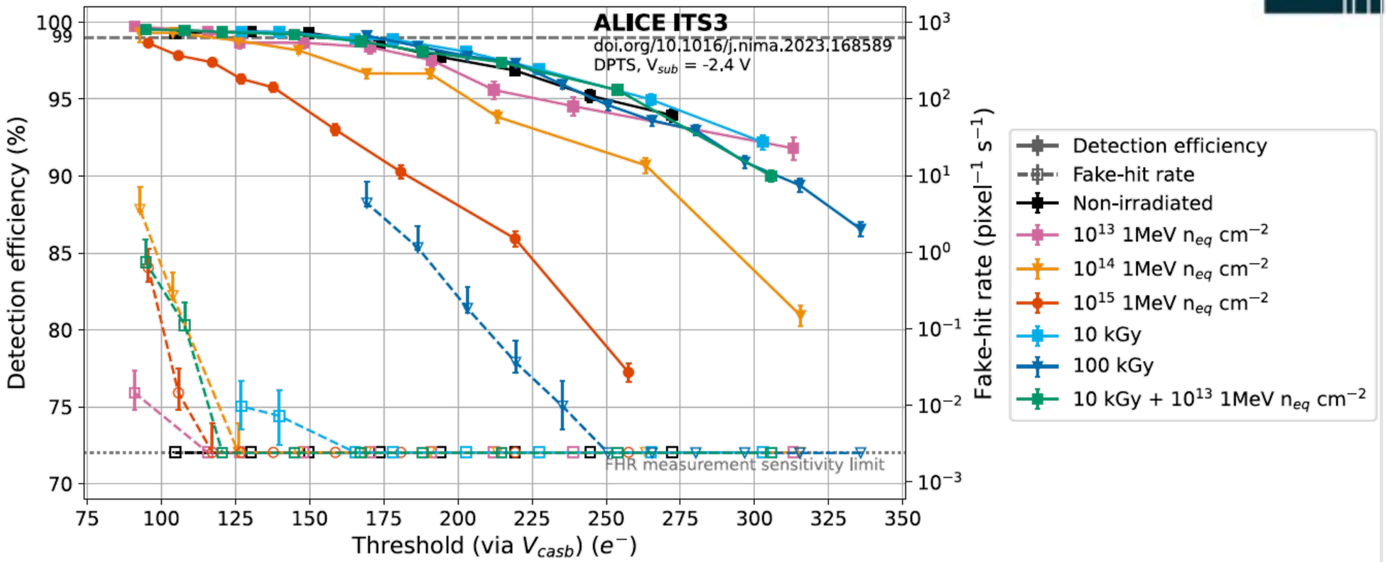
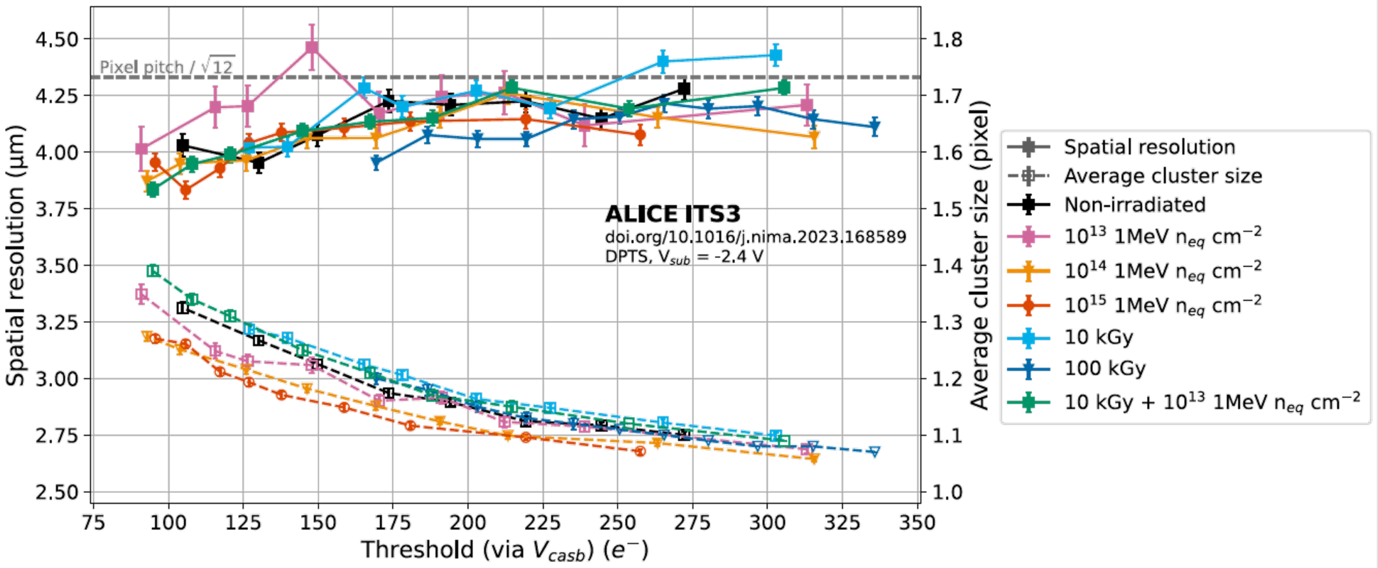
DPTS

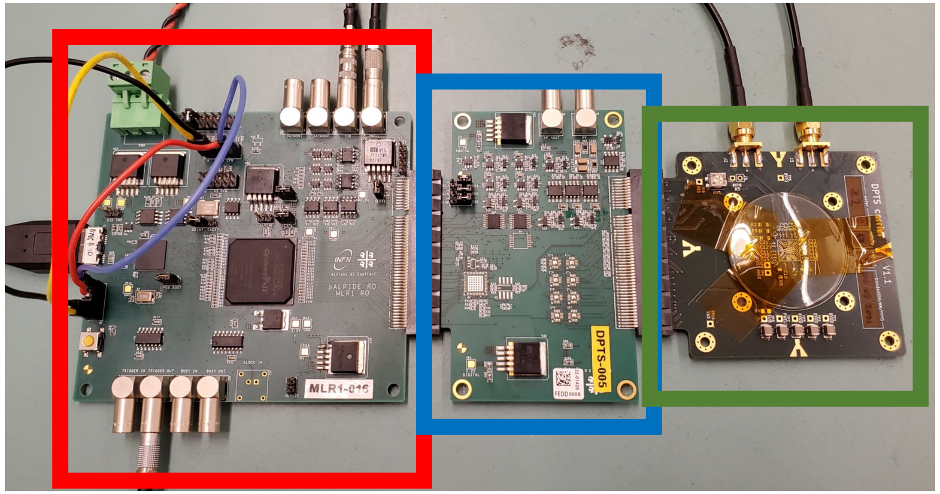
- **Radiation hardness**: works within ITS3 NIEL+TID requirement
- **Spatial resolution:** not affected by irradiation
- **Cluster size:** average increases slightly

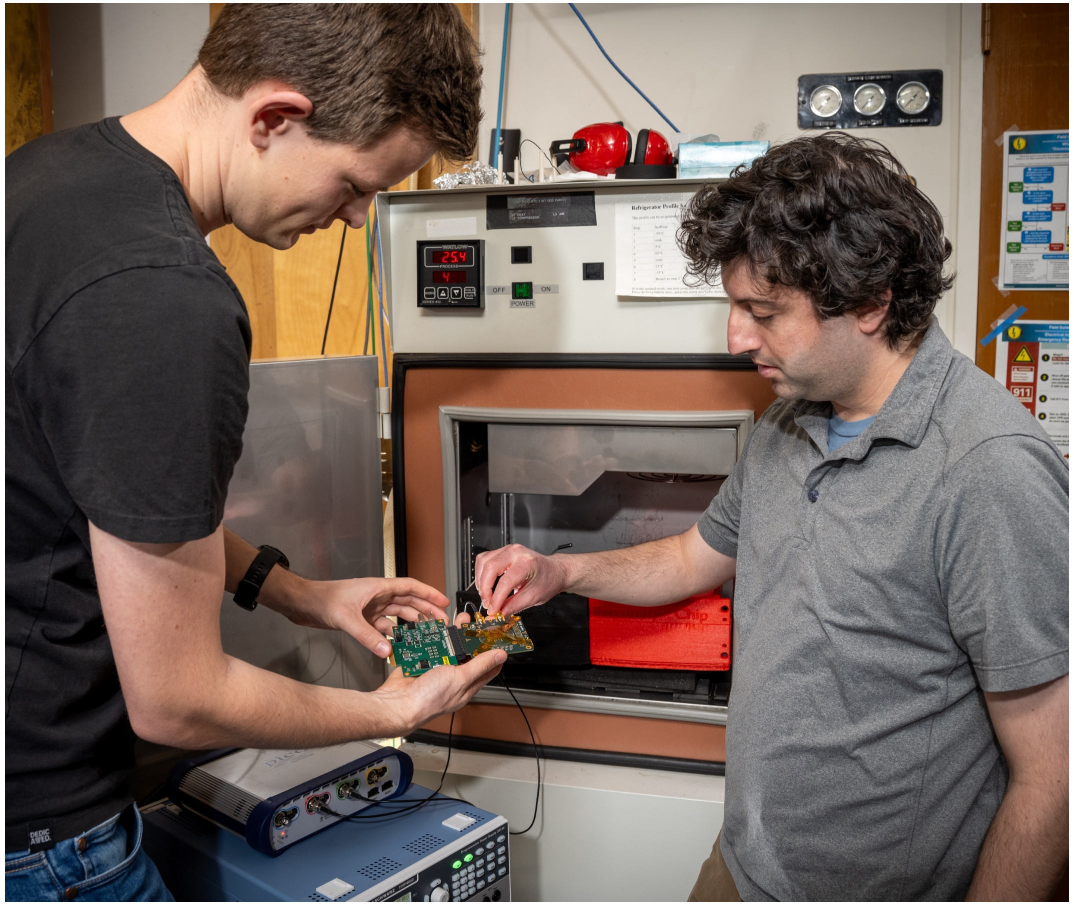




Temperature dependence

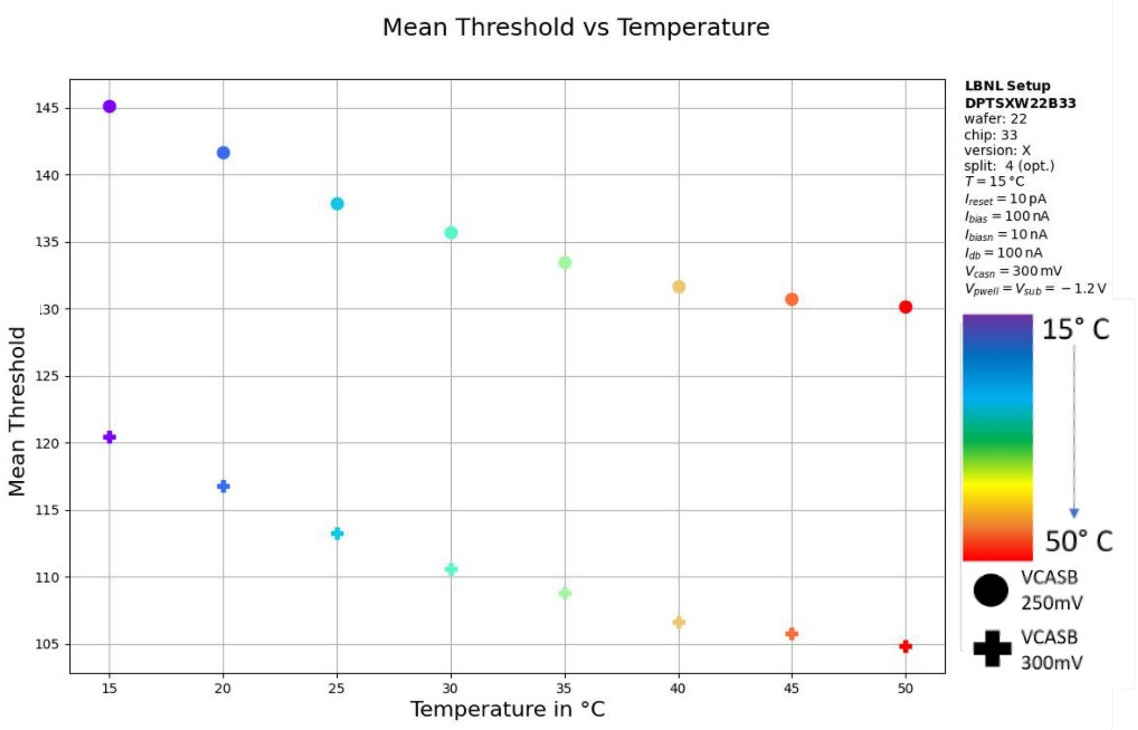
- Climate Chamber
  - Used in Range 15 – 50°C
  - High stability <0.5°C
- Fe55 source
- DPTS **DAQ**, **Proximity** & **Chip Carrier**

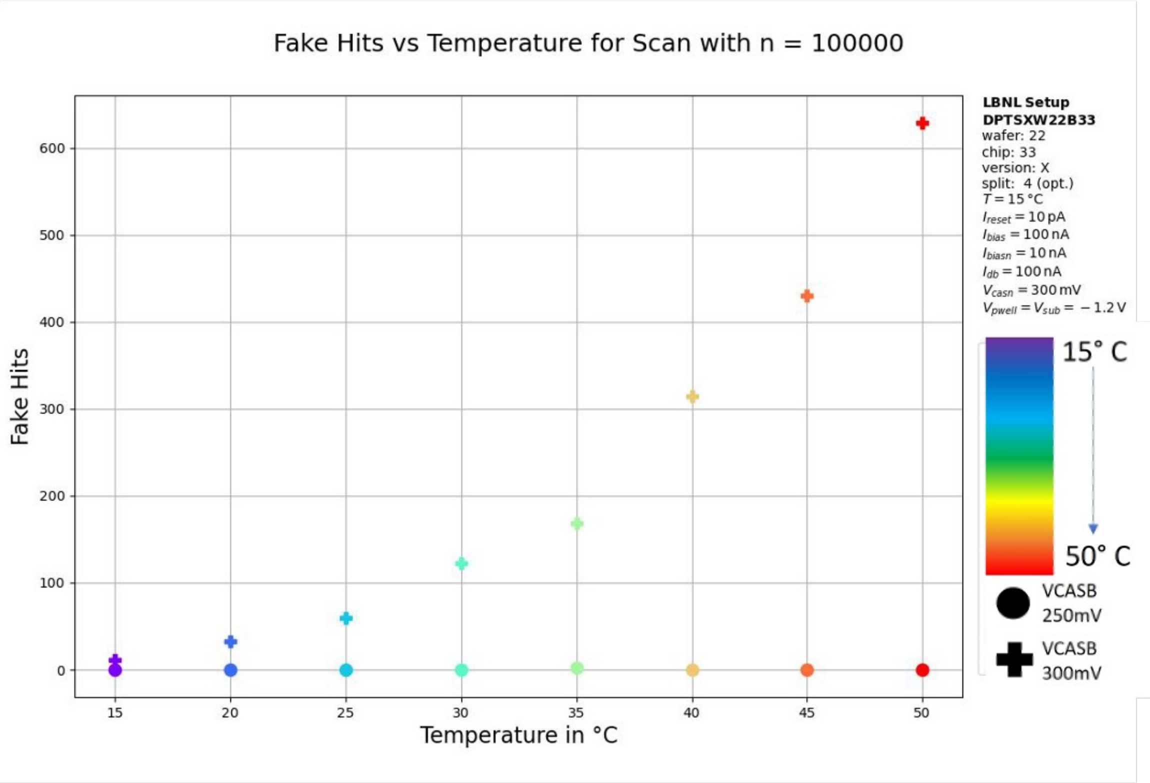




Picture: Thor Swift / Berkeley Lab

Threshold & Fake-hit rate



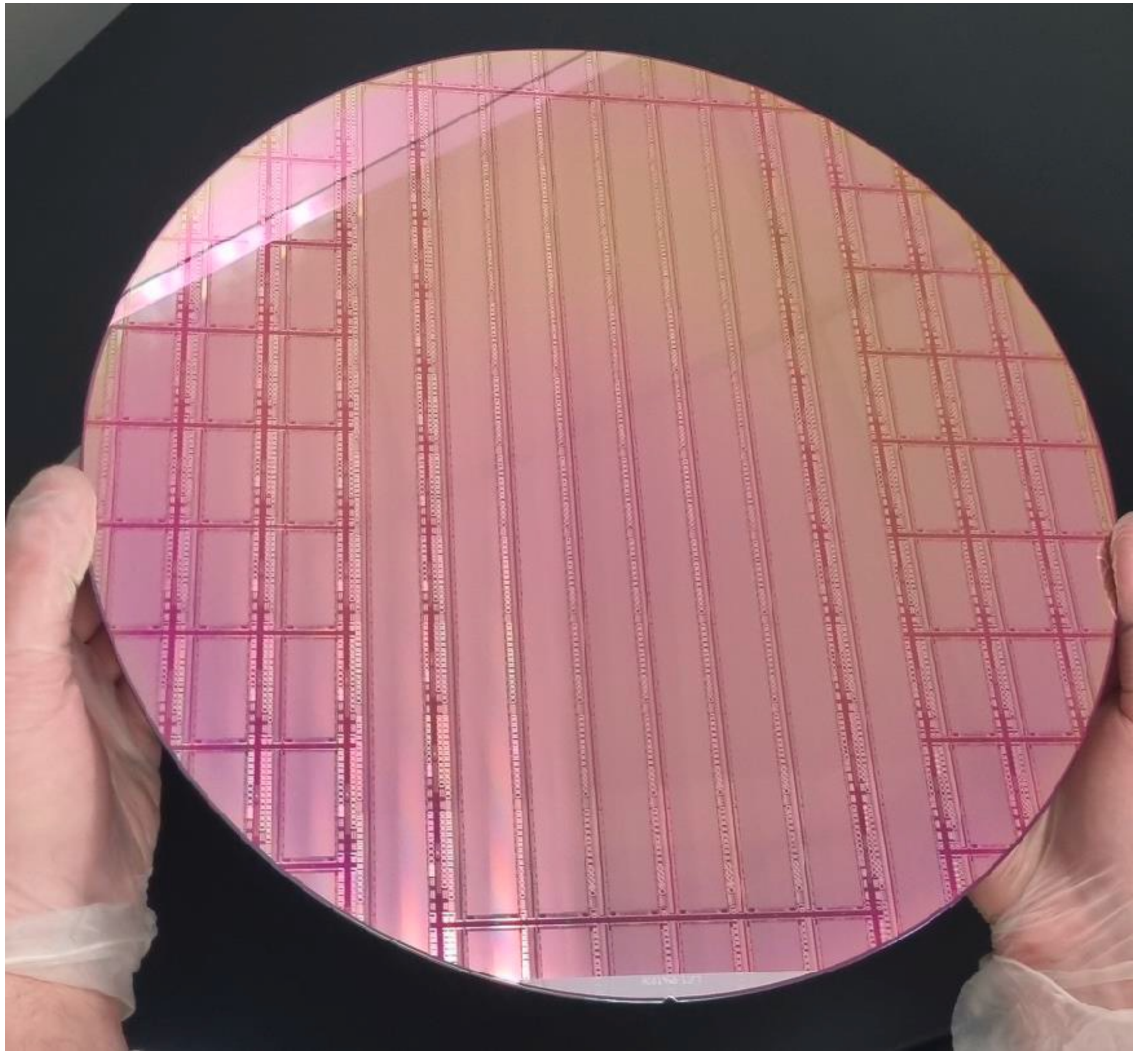


- Threshold: 0.5 e^- decrease per °C
- For higher temperatures effect no longer linear
- Threshold can be adjusted/corrected with configuration parameters

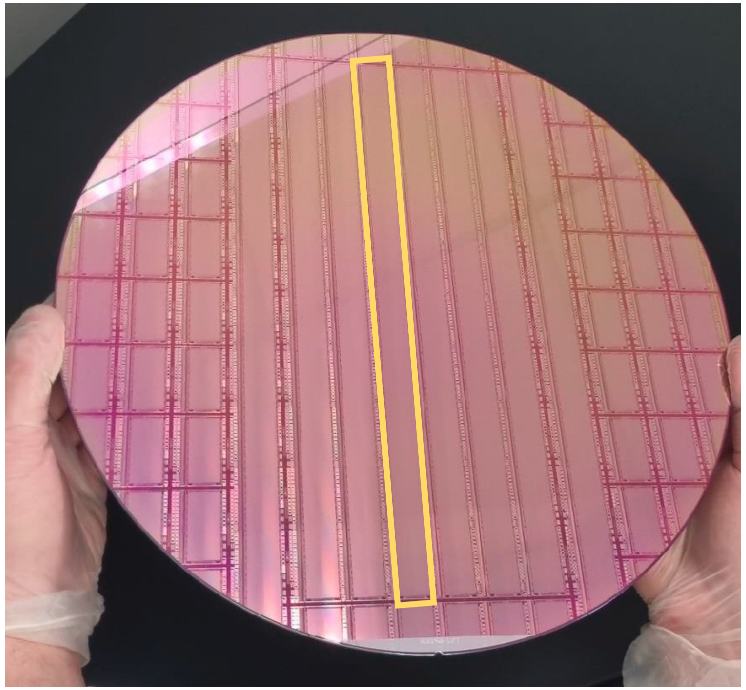
Temperature ↑ → Threshold ↓ → Fake-hit Rate ↑

65 nm submissions

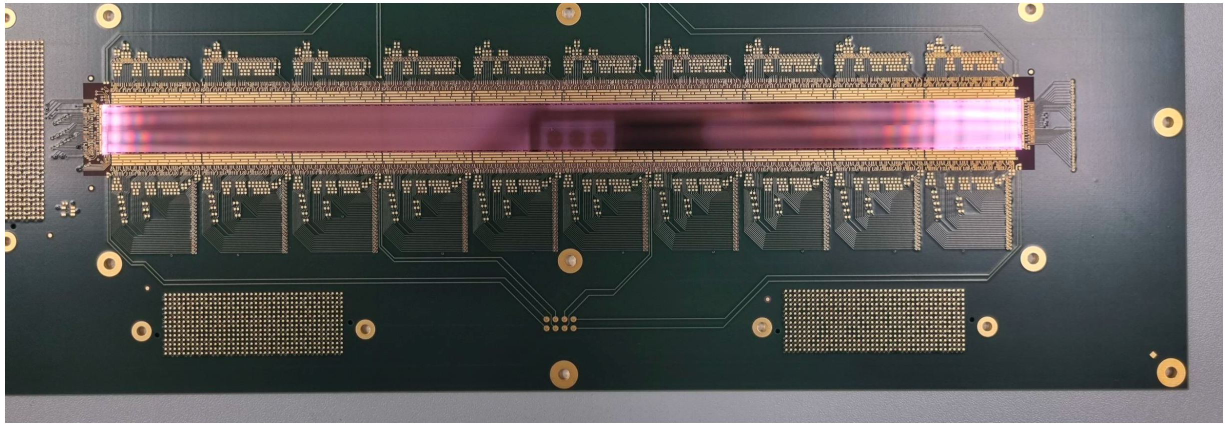
- **MLR1 (2021):** ✓
  - verification of 65 nm technology. Large number of test structures
- **ER1 (2023): first stitched MAPS**
  - Large design exercise, proof of stitching principles, learning methodology & yield
- **ER2 (submission end of 2024):** first ITS3 sensor prototype
- **ER3 (submission end of 2025):** ITS3 sensor production



ER1: MOSS

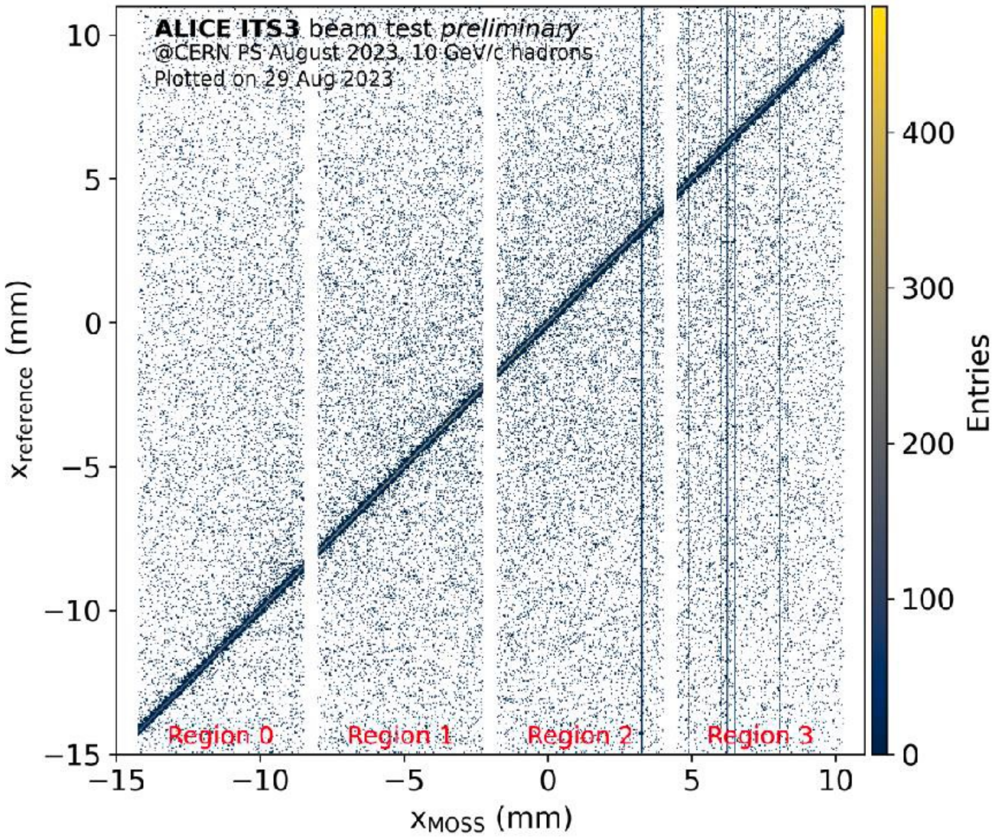


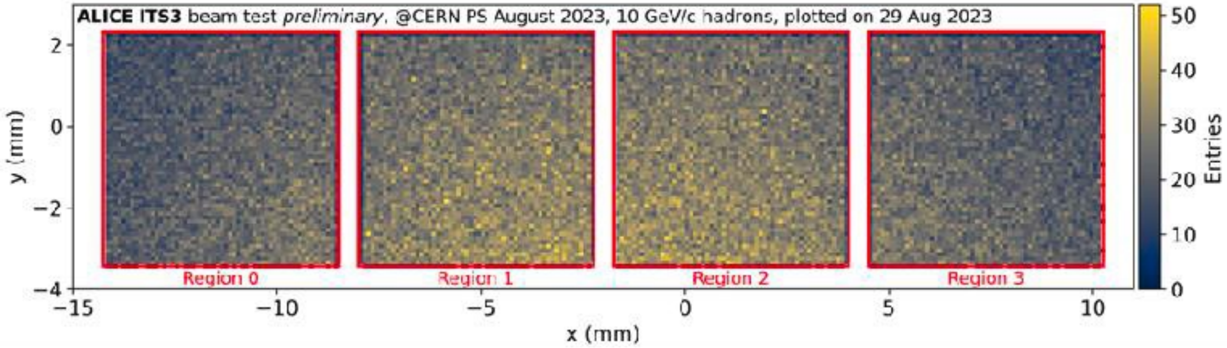
- MOSS: 14 x 259 mm^2
- 6.72M Pixel
  - 22.5 x 22.5 μm^2 and 18 x 18 μm^2
- **Primary objectives:**
  - Learn design with **stitching**
  - **Distribute** power & signals on wafer-scale chip
  - Study manufacturing **yield** & **constraints**
  - Study **power, leakage, noise, spread**

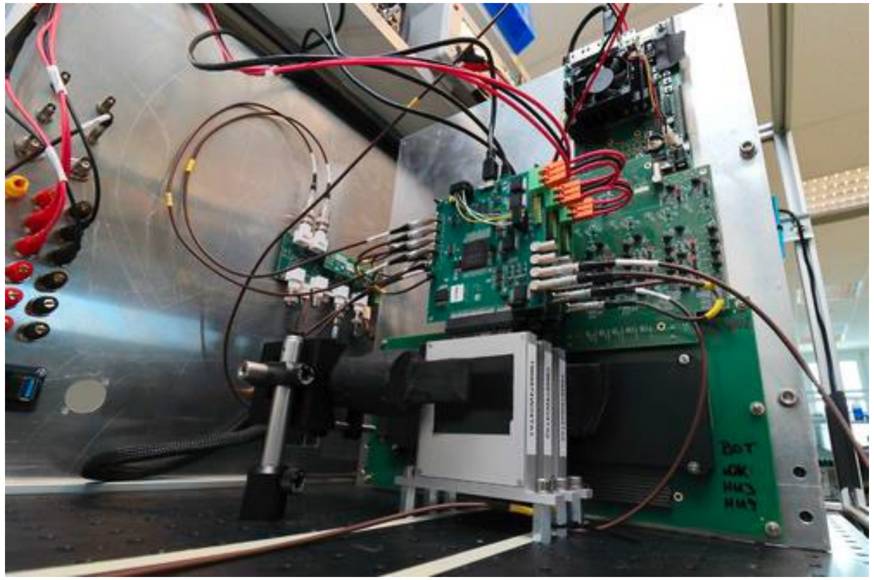


MOSS test beams

- Several campaigns since 2023
- Works out of the box
- Parameters still to be optimized & more data to be analyzed
- Very encouraging first results!







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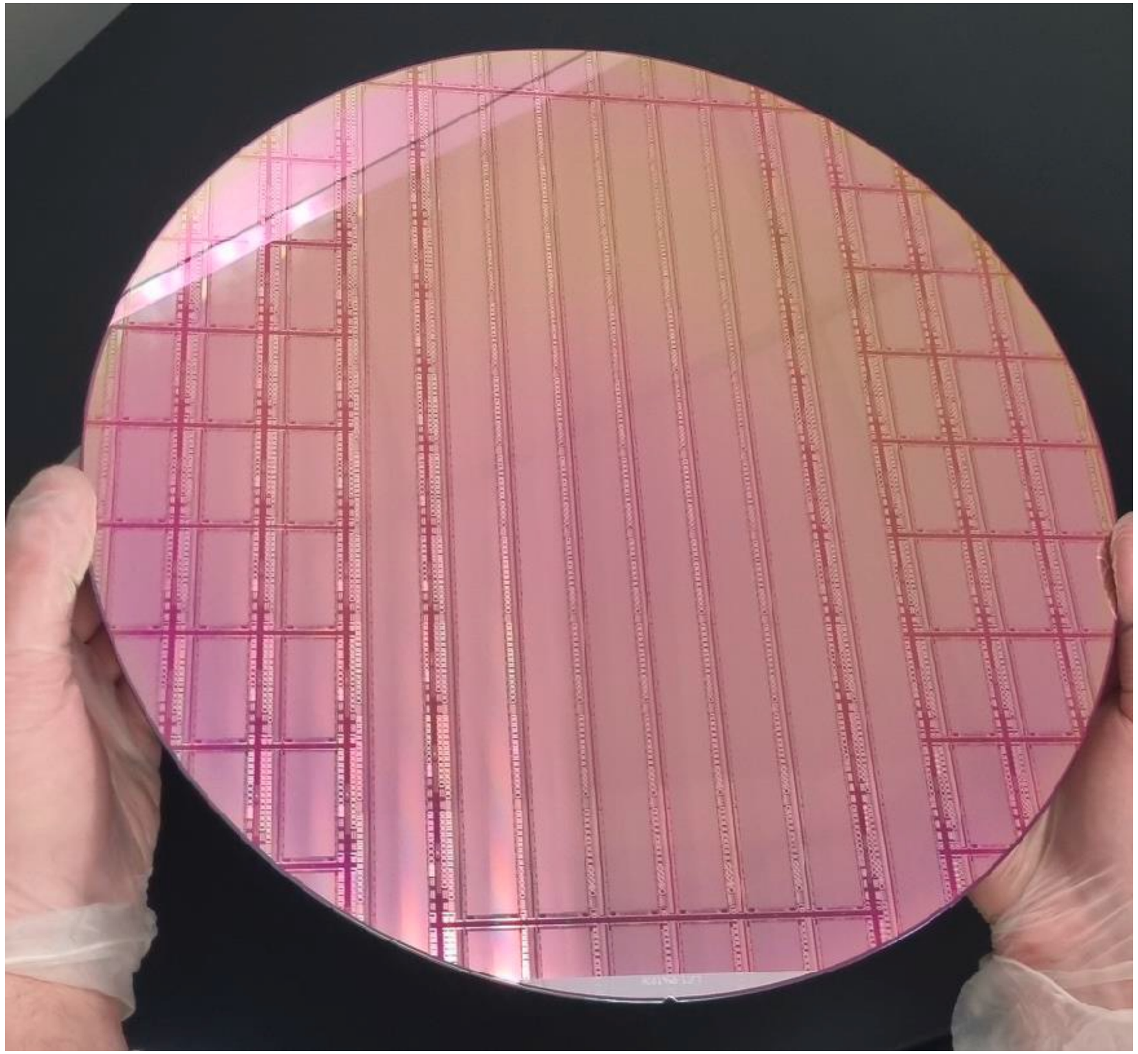
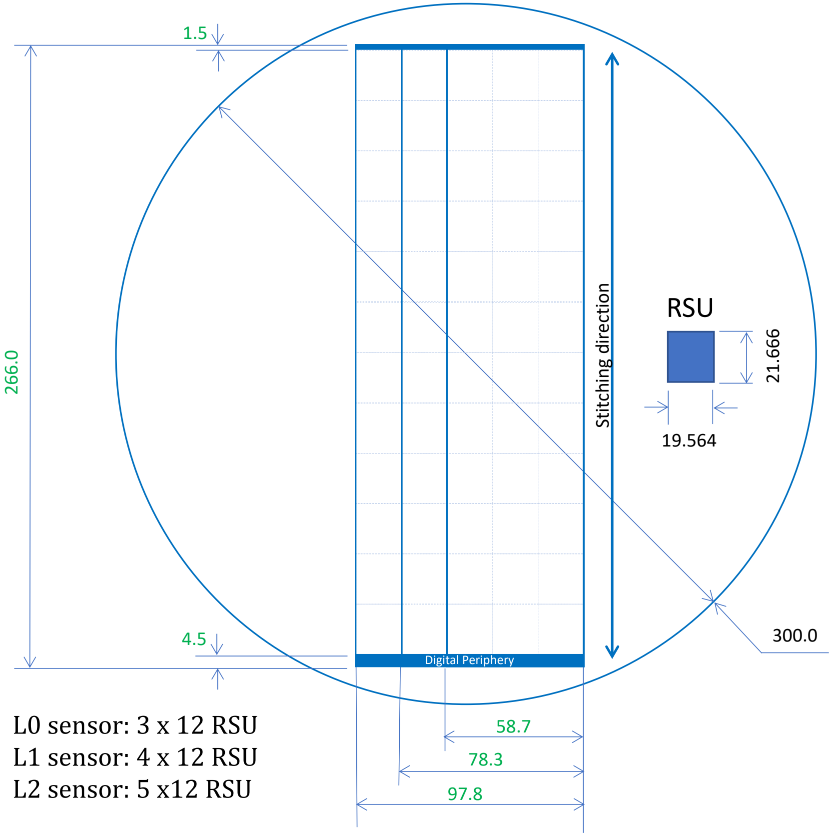


ER2 & ER3: MOSAIX

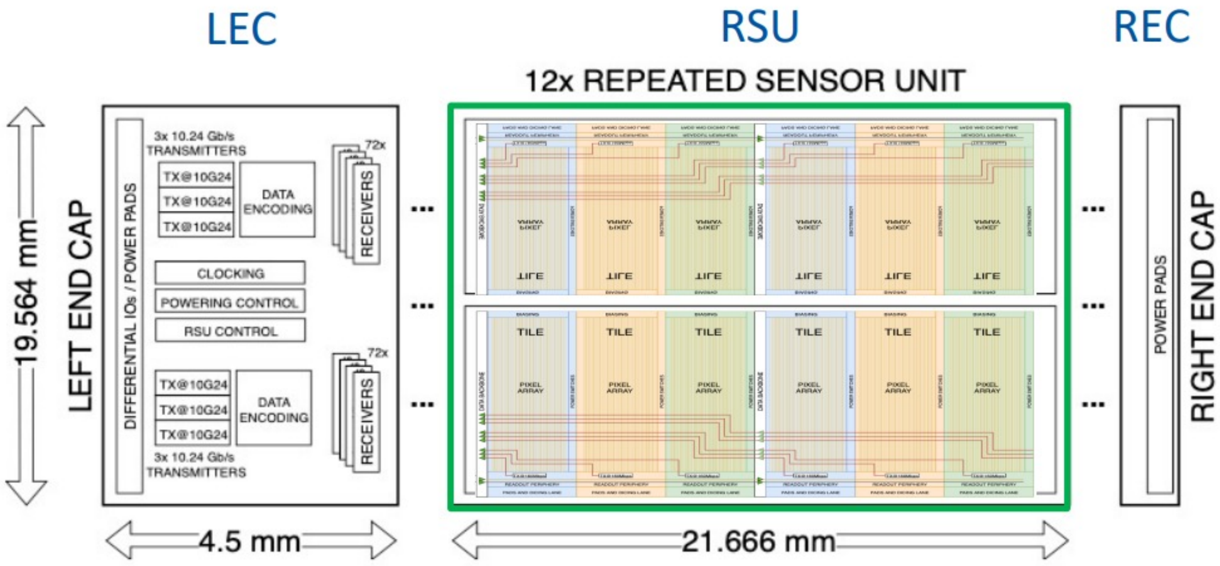
- Complex circuit designed, led by ITS3 team at CERN
  - Approximately 30 FTE of designers working on the submission



L0 sensor: 3 x 12 RSU
L1 sensor: 4 x 12 RSU
L2 sensor: 5 x12 RSU

ER2 sensor widths

19.564 x 3 = 58.692
19.564 x 4 = 78.256
19.564 x 5 = 97.820

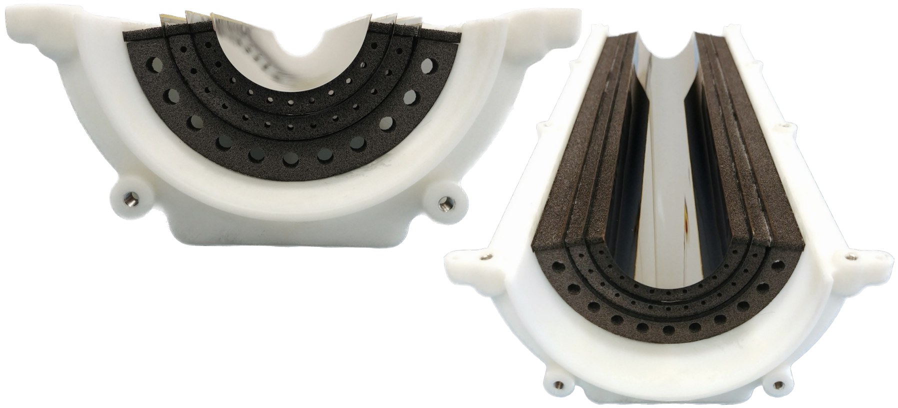


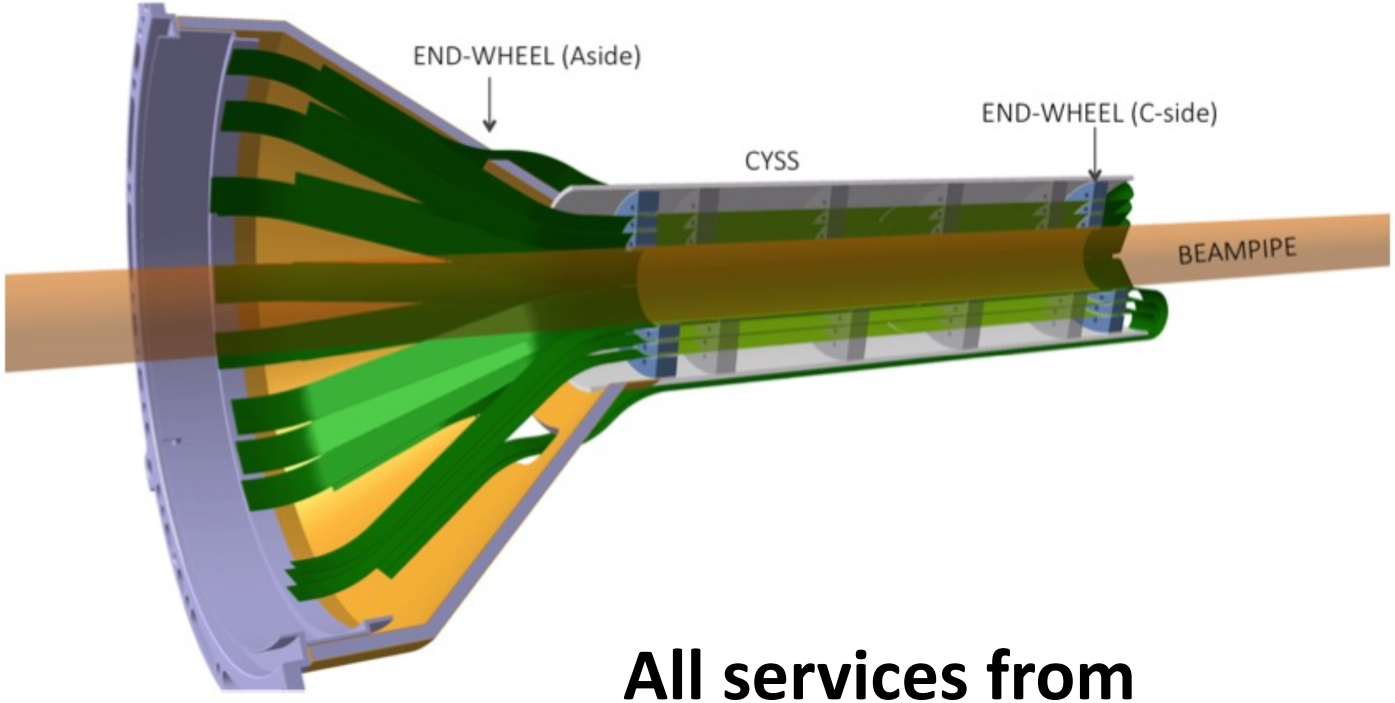
Pixel size: ~ 20 x 22 μm^2
Frame duration: 2 to 5 μs
Data link: 10.24 Gbps

ITS3

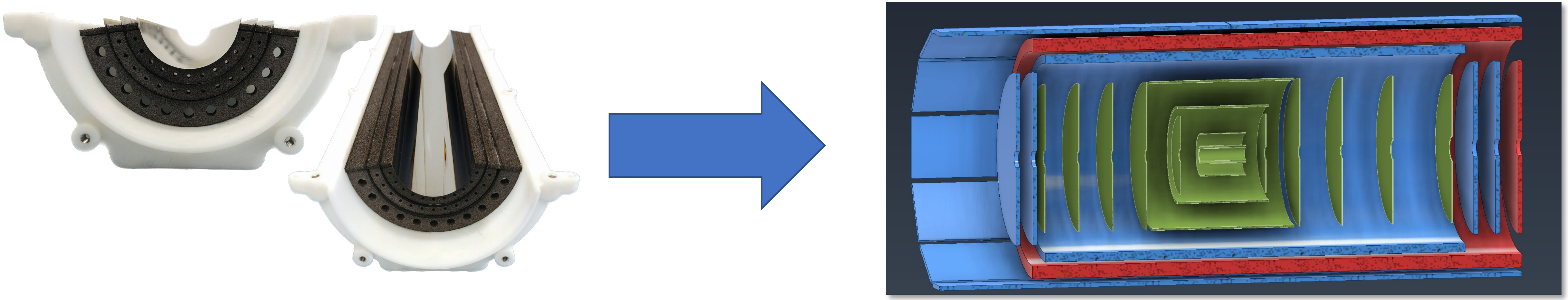
0.18 m^2 Si

6 MOSAIX sensors





All services from one end (like ITS2)

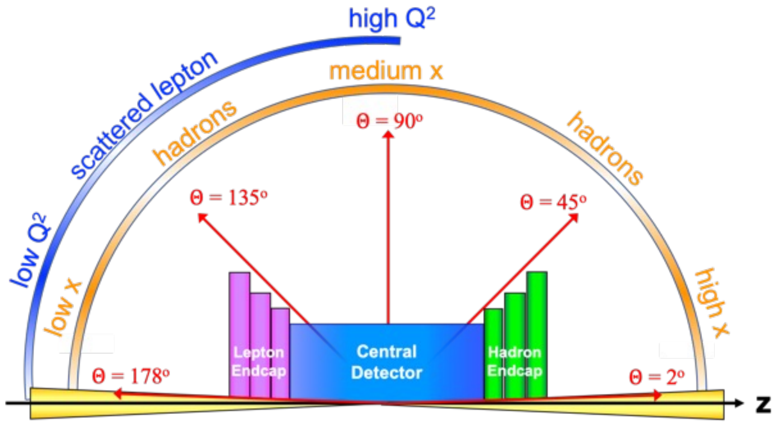


65nm MAPS for the EIC

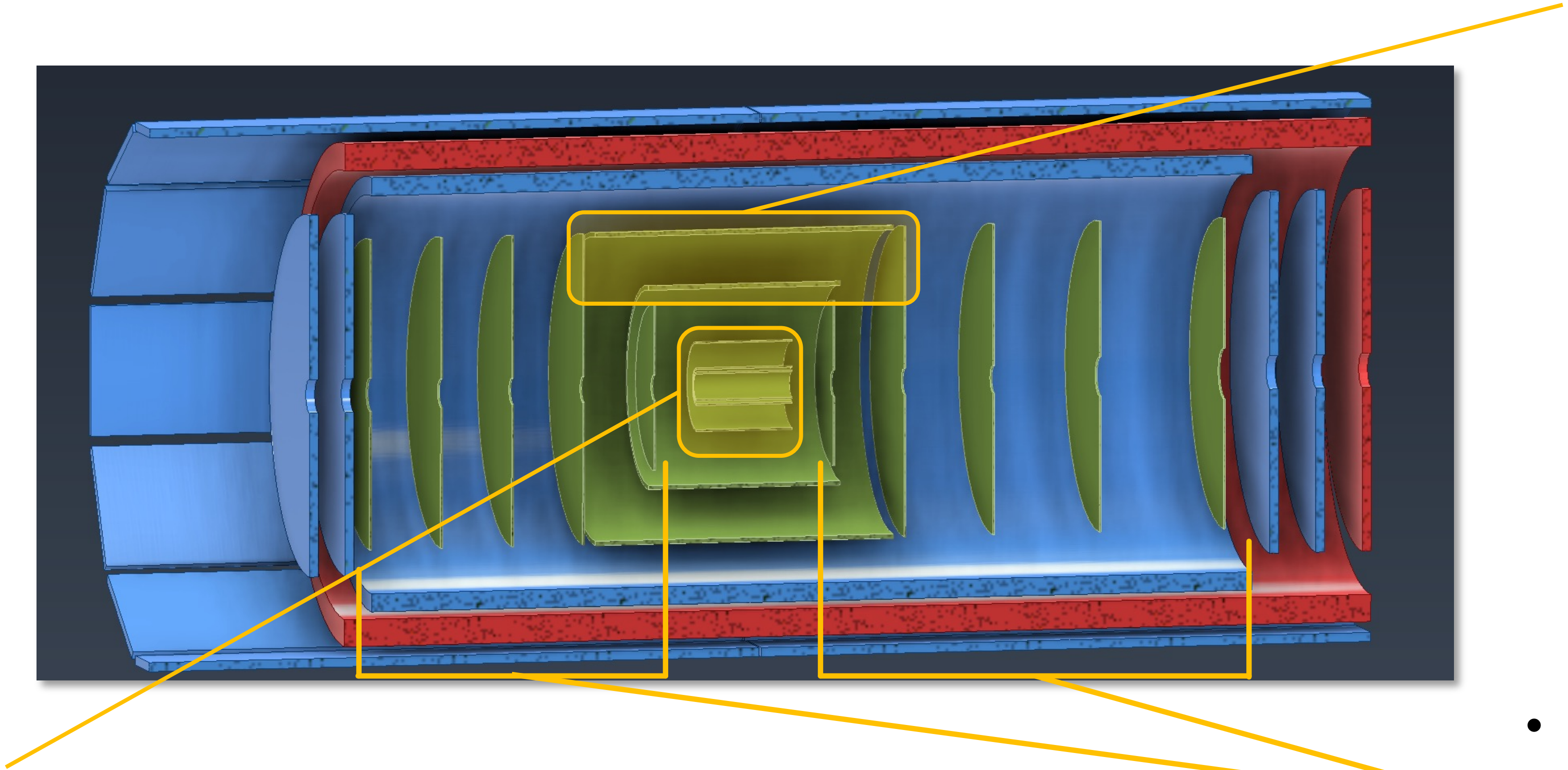
EIC tracking performance requirements

- Based on physics in the Yellow Report

	Momentum Resolution	Spatial Resolution
Backward (-3.5 to -2.5)	$\sim 0.10\% \times p \oplus 2.0\%$	$\sim 30/pT\ \mu m \oplus 40\ \mu m$
Backward (-2.5 to -1.0)	$\sim 0.05\% \times p \oplus 1.0\%$	$\sim 30/pT\ \mu m \oplus 20\ \mu m$
Barrel (-1.0 to 1.0)	$\sim 0.05\% \times p \oplus 0.5\%$	$\sim 20/pT\ \mu m \oplus 5\ \mu m$
Forward (1.0 to 2.5)	$\sim 0.05\% \times p \oplus 1.0\%$	$\sim 30/pT\ \mu m \oplus 20\ \mu m$
Forward (2.5 to 3.5)	$\sim 0.10\% \times p \oplus 2.0\%$	$\sim 30/pT\ \mu m \oplus 40\ \mu m$



SVT concept



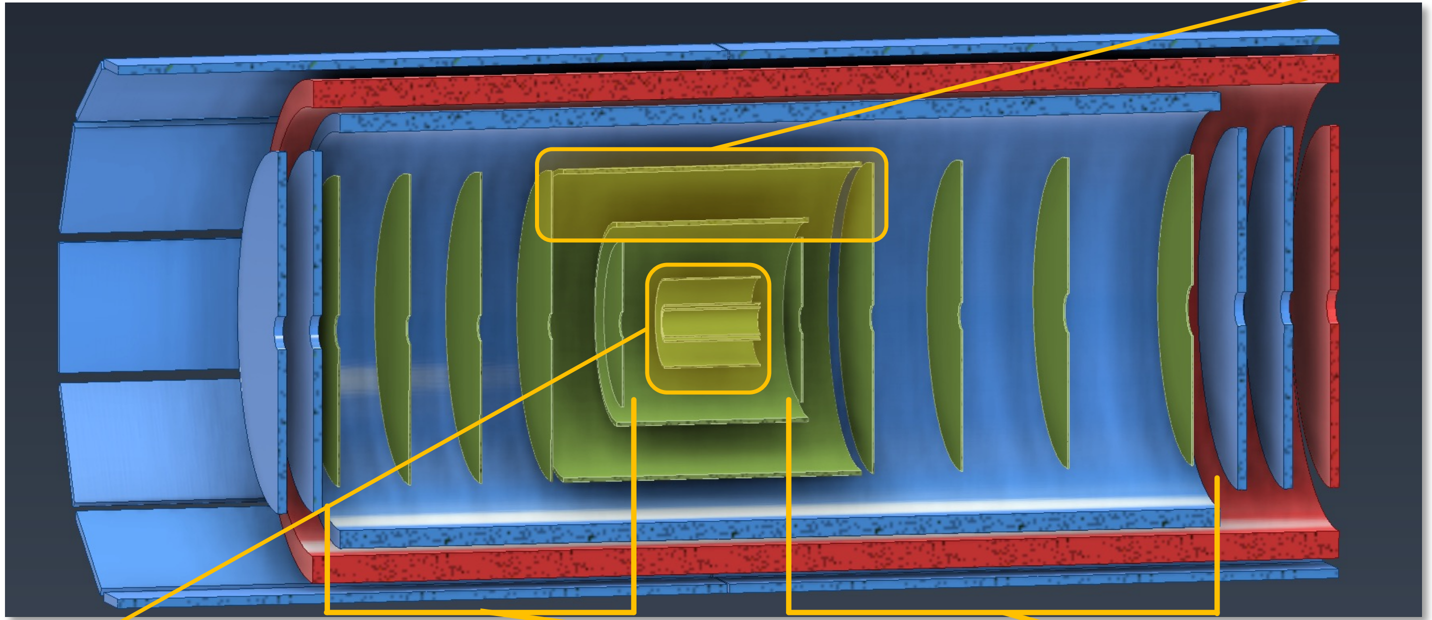
- **Outer Barrel (OB)**
  - Two layers, L3, L4
  - Radii of 27 and 42 cm
  - X/X_0 ~0.25% and ~0.55%
  - More conventional structure w. staves
  - **EIC-LAS MAPS**

~8 m^2 Si

- **Electron/Hadron Endcaps (EE, HE)**
  - Two arrays with five disks
  - X/X_0 ~0.25% per disk
  - More conventional structure
  - **EIC-LAS MAPS**

- **Inner Barrel (IB)**
  - Three layers, L0, L1, L2,
  - Radii of 36, 41, 120 mm
  - Length of 27 cm
  - X/X_0 ~ 0.05% per layer
  - **MOSAIX → 16 sensors**

SVT concept



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  - **MOSAIX → 16 sensors**

EIC-LAS

- The ePIC SVT IB will use 16 MOSAIX thinned, bent, wafer-scale sensors → ~0.3 m^2
- The ePIC SVT OB, EE and HE → ~8 m^2
- This requires a sensor design optimized for **low cost, high acceptance, large area coverage**
- The **EIC-LAS** sensor will be based off ITS3 ER2/ER3 designs with modifications for the SVT
  - Thinned, but *not* wafer-scale
- Modifications of MOSAIX are kept to a minimum → ***ONLY*** in the LEC
  - Work within the available time and resources
  - Reduce risk of submission failure
- Low-material powering, biasing, and slow-control for the EIC-LAS is essential to SVT design and will be provided with a single **Ancillary ASIC** in 180nm Silicon-on-Insulator process

MOSAIX to EIC-LAS

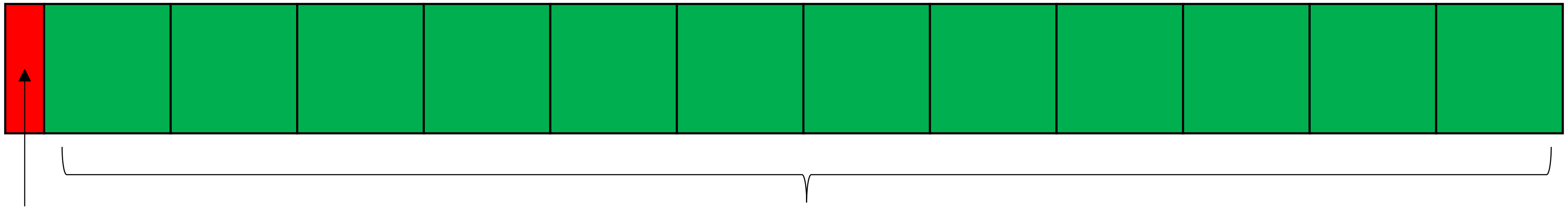
Inner Barrel

Outer Barrel, E/H Endcaps

12 RSUs	Improve yield and coverage →	5 or 6 RSUs	**EIC-LAS**
8 data links	Lower material budget →	Single data link	
7 slow control links	Lower material budget, fit integration requirements →	Multiplex slow control	**Ancillary ASIC**
Direct powering	Lower material budget, fit integration requirements →	Serial powering	

Sensor Power Regions

IB sensor: MOSAIX



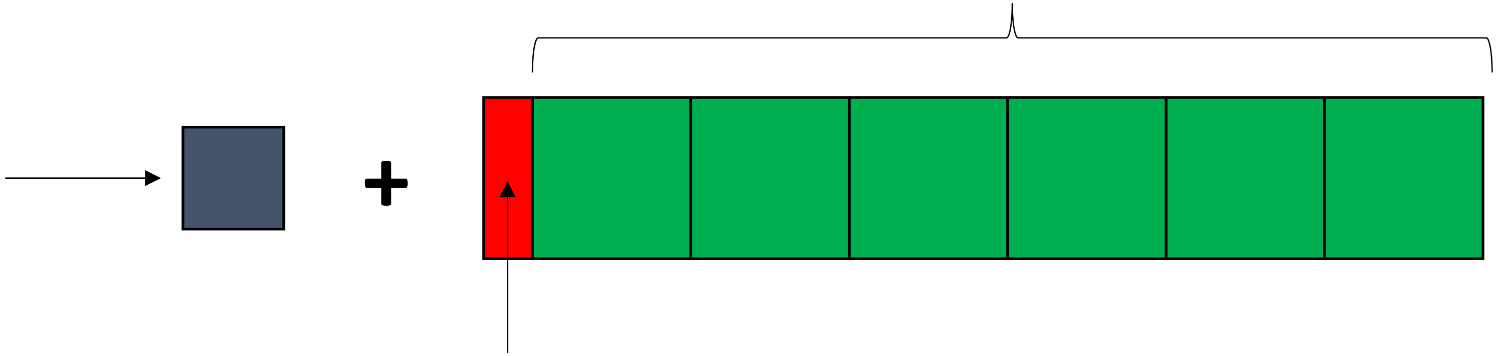
LEC: ~0.8 W/cm²

12 **RSUs**: up to 40 mW/cm²

OB/HE/EE sensor: EIC-LAS

5-6 **RSUs**: same power density as MOSAIX

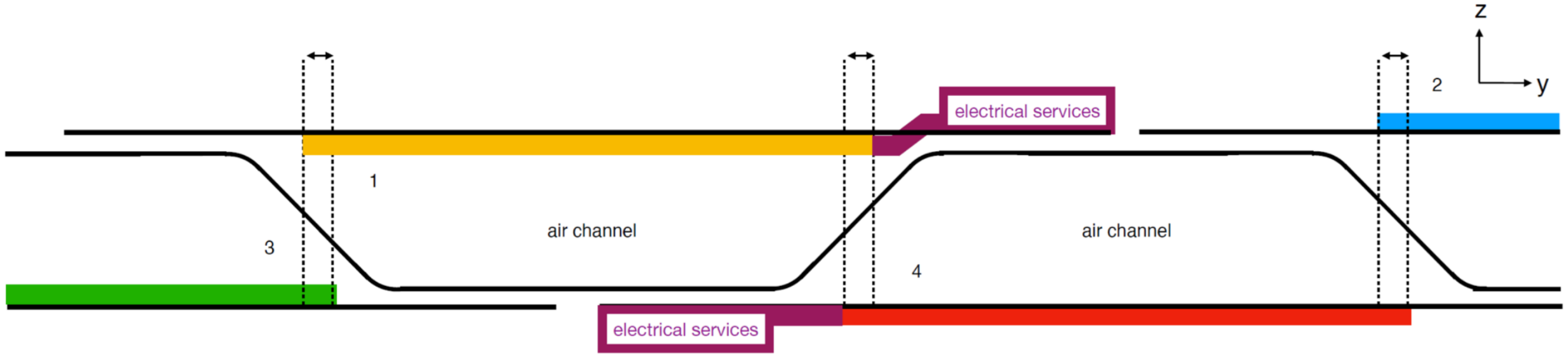
AncASIC:
Size & power TBD



EIC-LAS LEC ≤ MOSAIX LEC

Discs: Sensor Tiling and Grouping

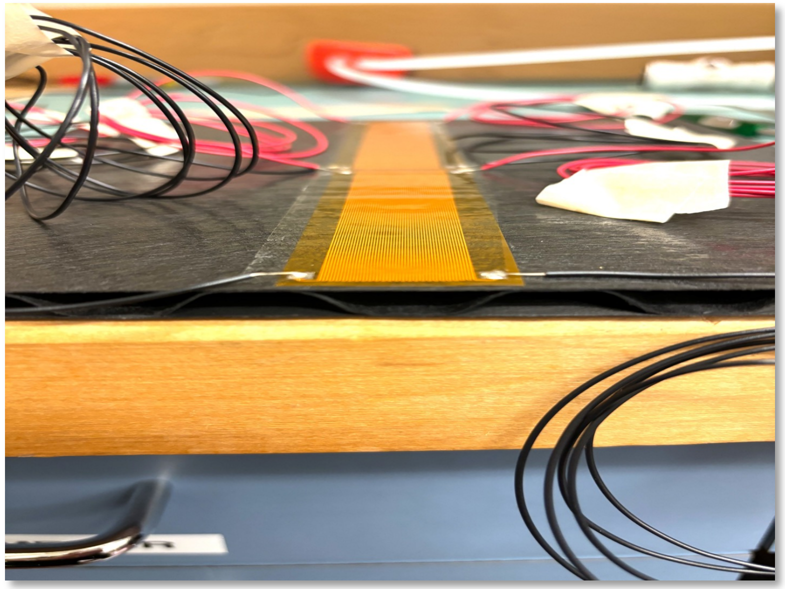
- EIC-LAS with **5** or **6 RSUs**
- Discs are currently foreseen to have a **corrugated** core. Tiling can then be done on four surfaces.
- In sideview, with the length axis of the sensor going into or coming out of the screen:



- Overlap along the length axis is possible by alternation,
- Corrugation pitch and height determine EIC-LAS overlap along the short axis; current values of ~34 mm and 6 mm, respectively, are being further optimized.

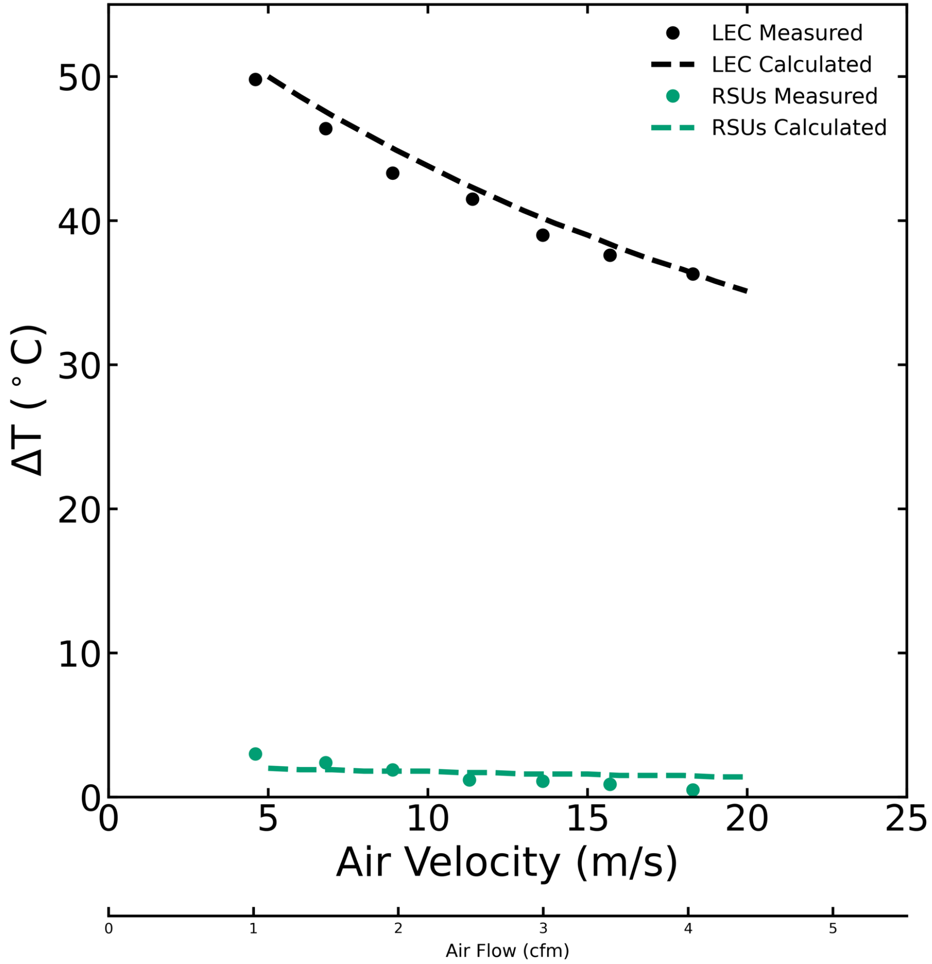
Discs: Corrugated Carbon Fiber

- ***Baseline*** disc design using corrugated carbon fiber
  - Provides a channel for forced air convection
- Air cooling sufficient for **RSUs**
- **LEC** trending in the right direction



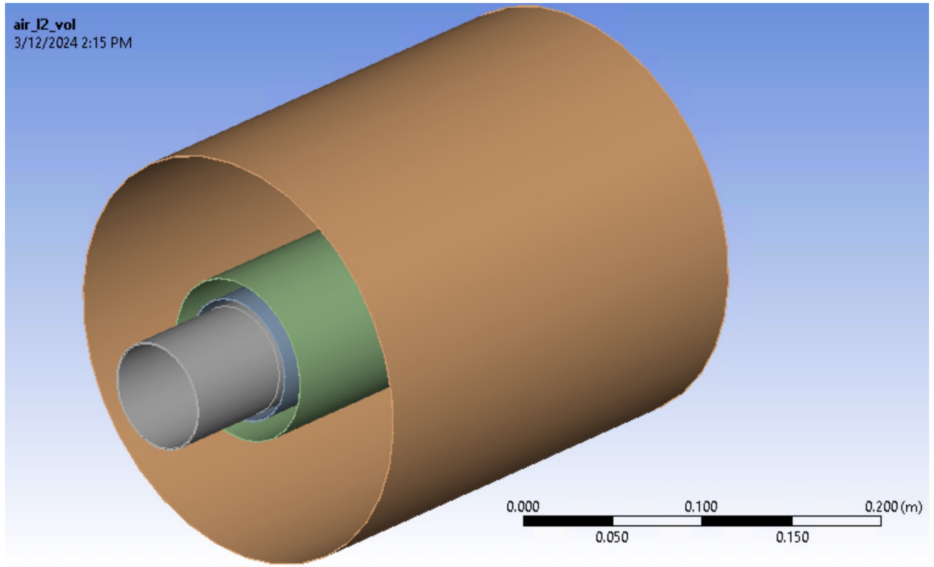
LEC: 1 W/cm^2

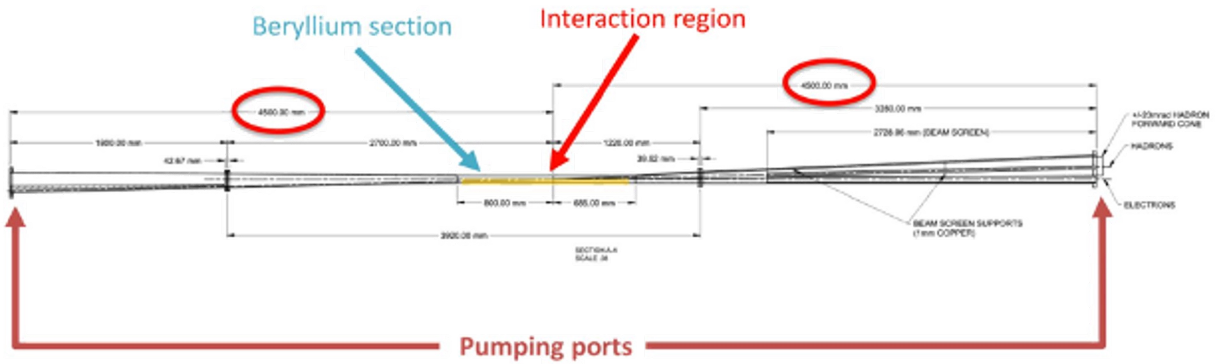
RSUs: 40 mW/cm^2



Beam-pipe Bake-out

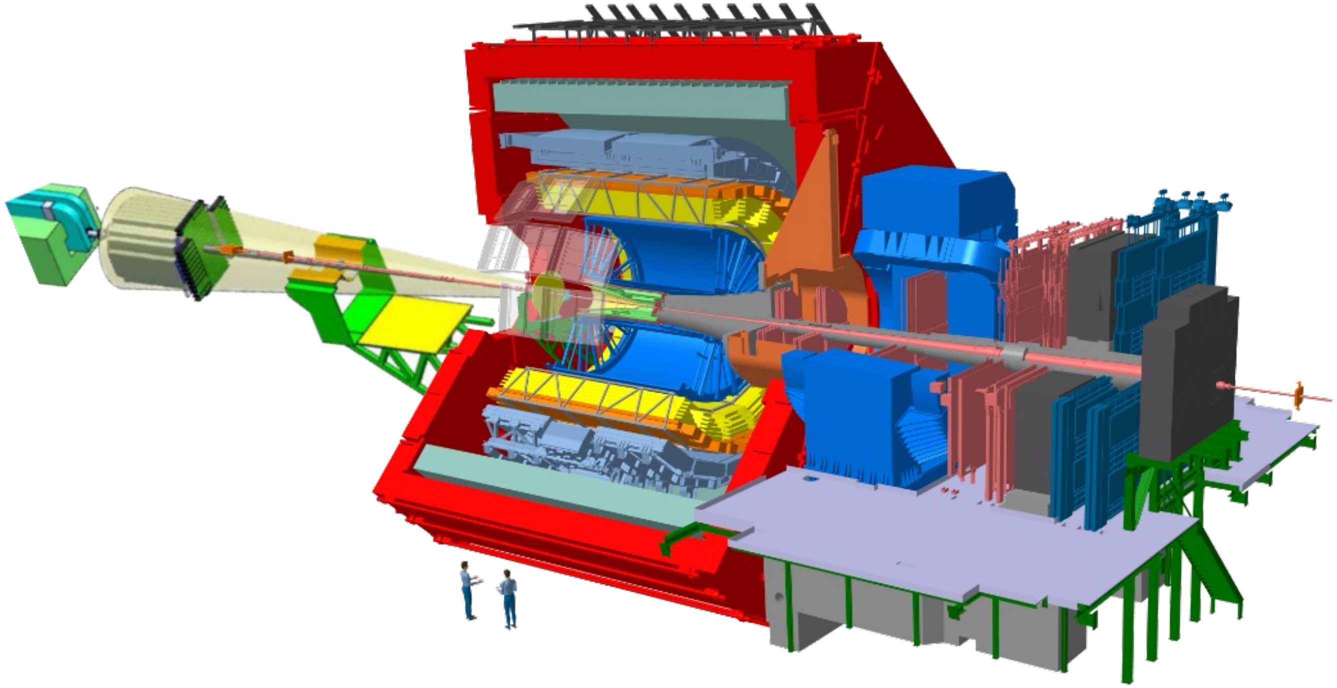
- Beam-pipe bake-out with SVT installed
- Aiming for no additions to cooling
  - No extra material (e.g. insulators) or changes (i.e. liquid instead of air)
- ANSYS studies at JLab and LBNL
  - Flow N2 in beam-pipe to get inner wall >100°C
  - Room temperature air to cool silicon
  - Studies done with both full length of beam pipe and shortened section near SVT IB
- Bench setup at JLab verifies results
  - Covers 1 m of 3 m Be beam pipe section
- Path forward to cool detector



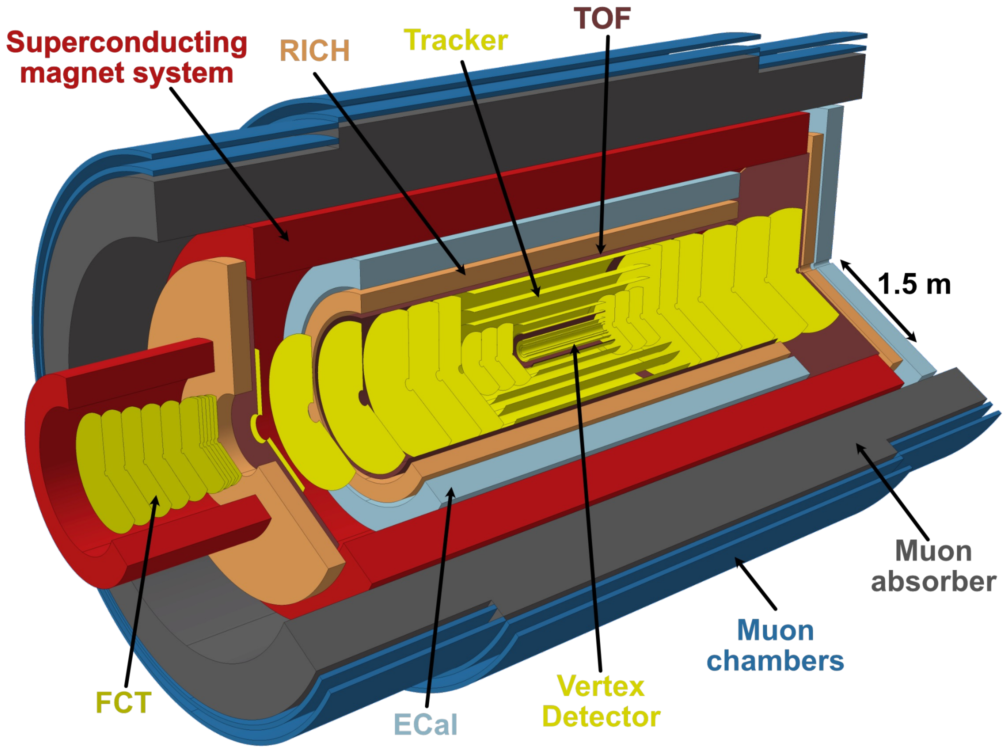


Back to the LHC & getting even larger

Increasing tracker size



ALICE 2.1
~10 m^2 Si



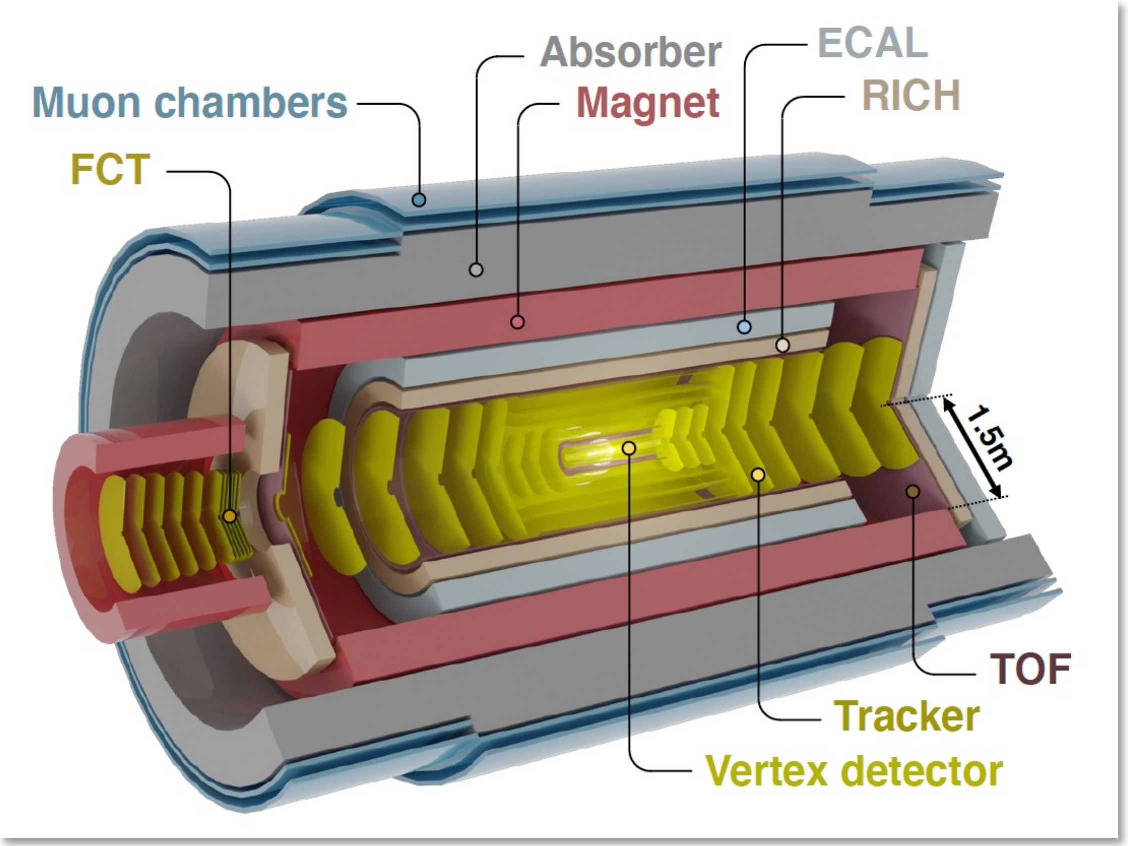
ALICE 3
~60 m^2 Si

ALICE 3 requirements

- High-efficiency for heavy-quark identification
- Vertexing close to beam pipe
- Large acceptance & coverage down to low p_T

Compared to ALICE 2.1

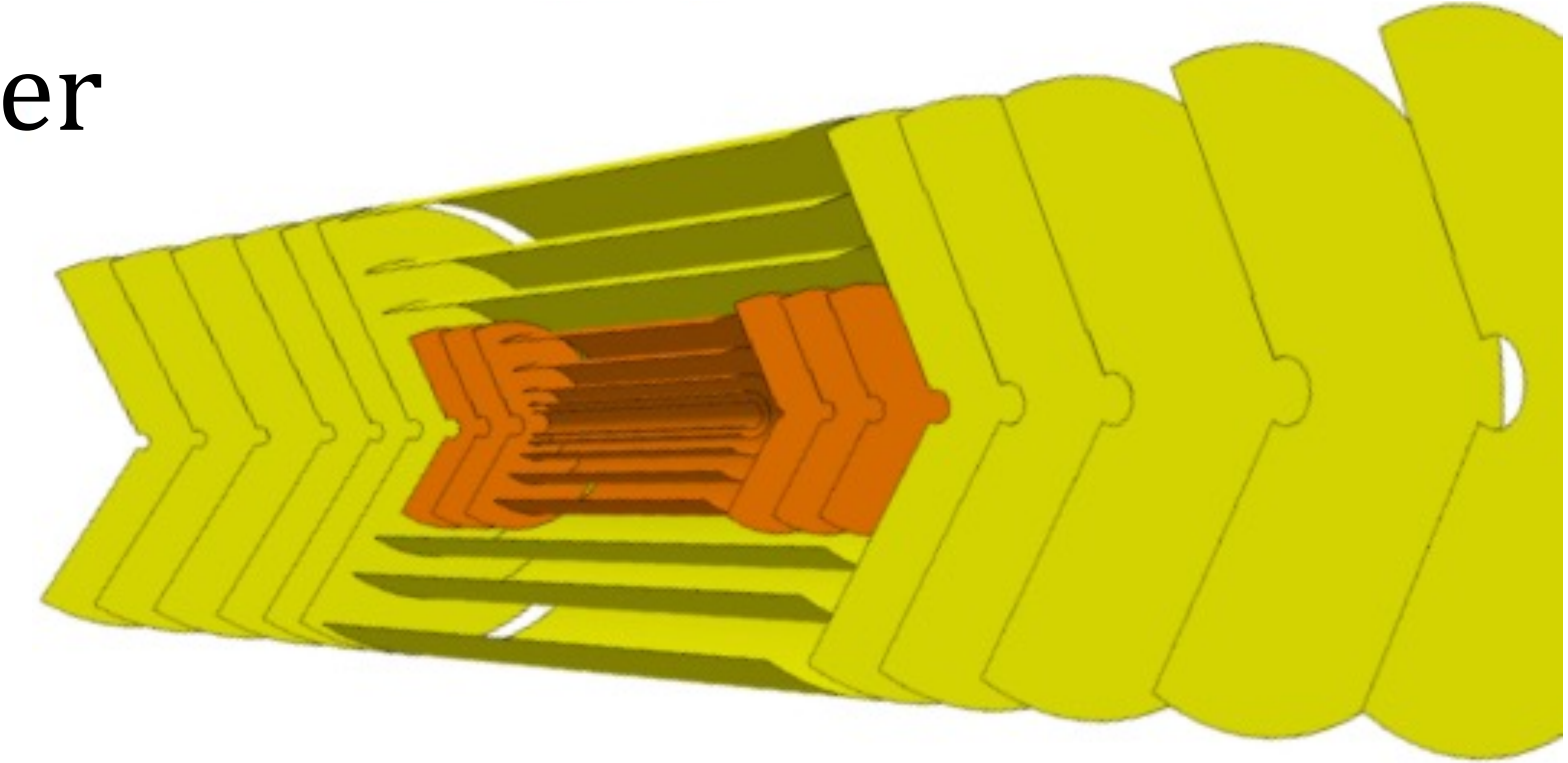
- Tracking precision **x 3:** 10 μm at p_T = 200 MeV/c
- Acceptance **x 4.5:** $|\eta| < 4$
- A-A rate **x 5** (pp x 25)

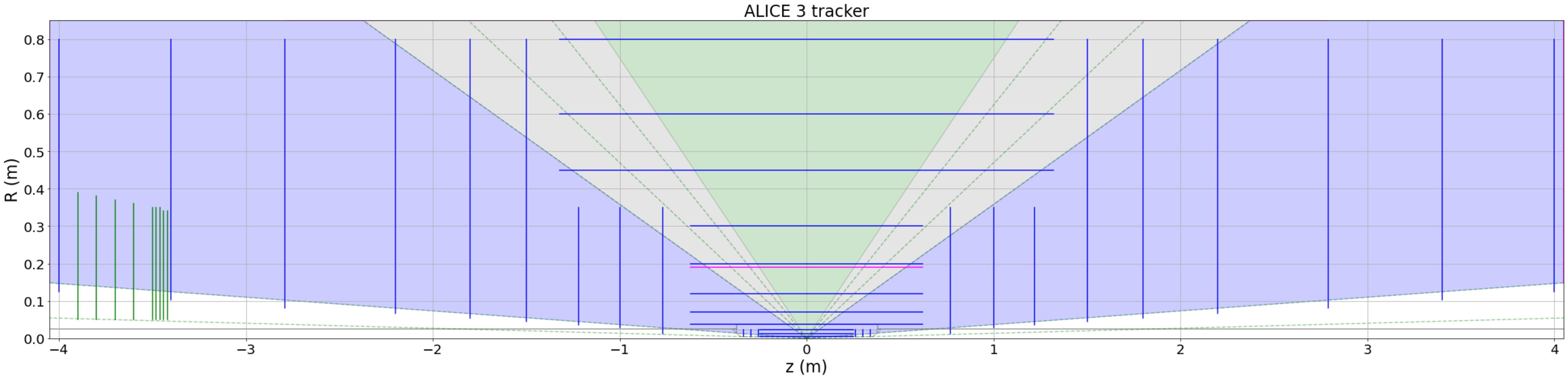


All-silicon tracker

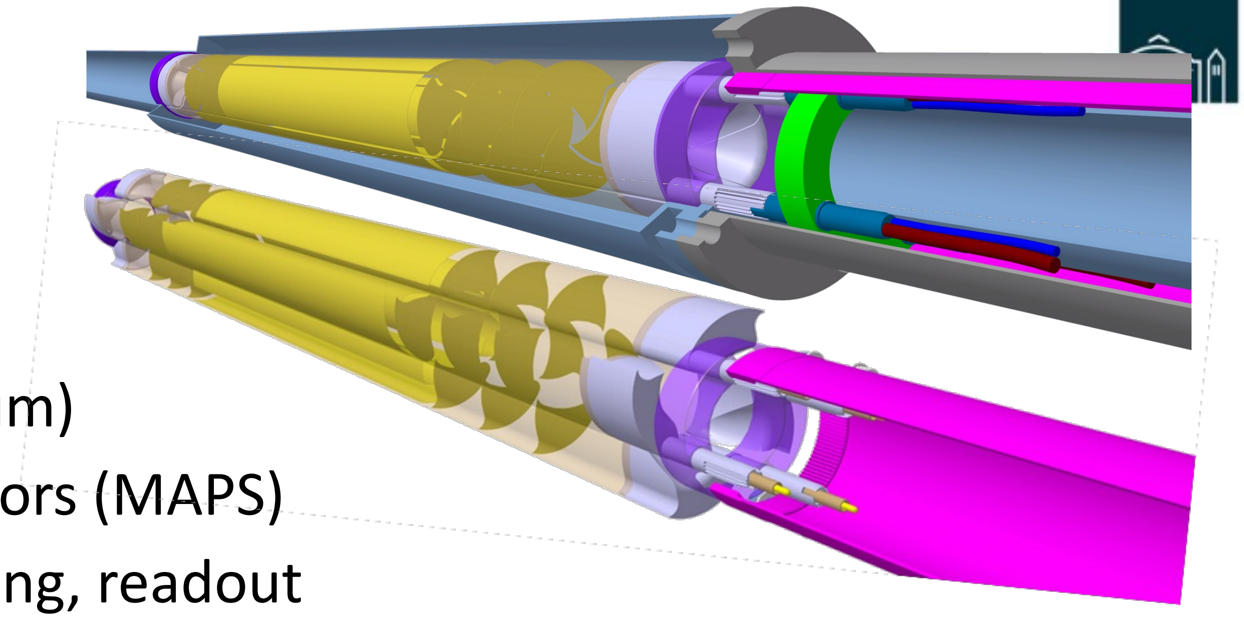
Baseline

- **11** barrel layers
- **12** discs per side
- Split into ***Vertex Tracker*** & ***Outer Tracker***
- **60 m^2** active area





Vertex Detector



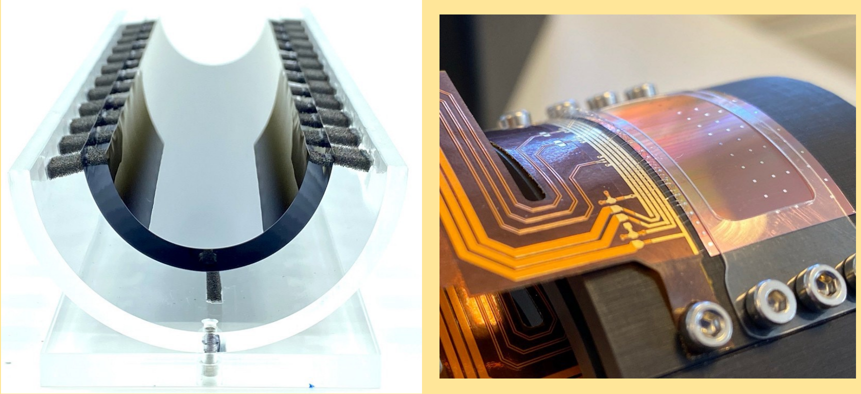
Pointing Resolution → 10 μm @ p_T = 200 MeV/c

Conceptual design

- 3 layers within beam-pipe (in secondary vacuum)
- Wafer-scale, bent Monolithic Active Pixel Sensors (MAPS)
- Rotary petals & feed-throughs for power, cooling, readout

R&D

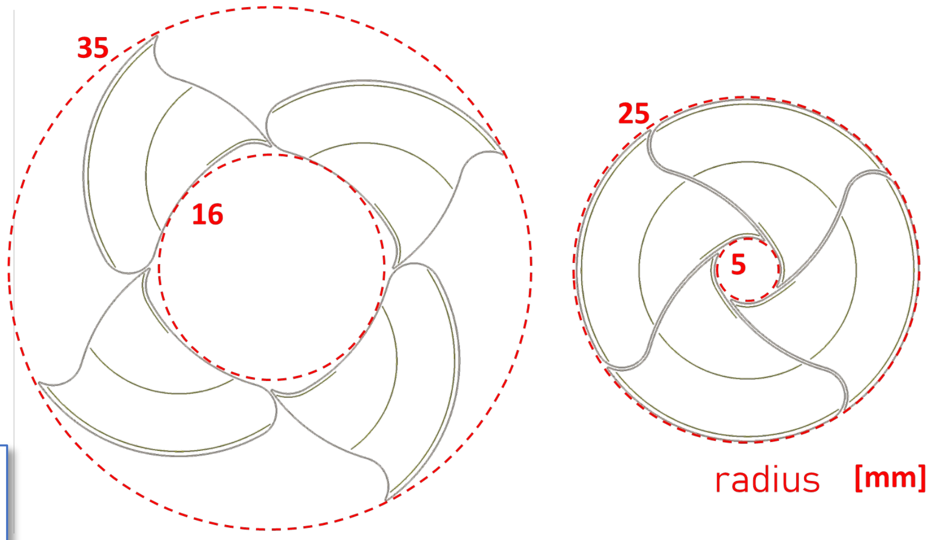
- Mechanics, cooling, radiation tolerance



ALICE ITS3 R&D

$\sigma_{pos} \sim 2.5\ \mu m$
→ 10 μm pixel pitch

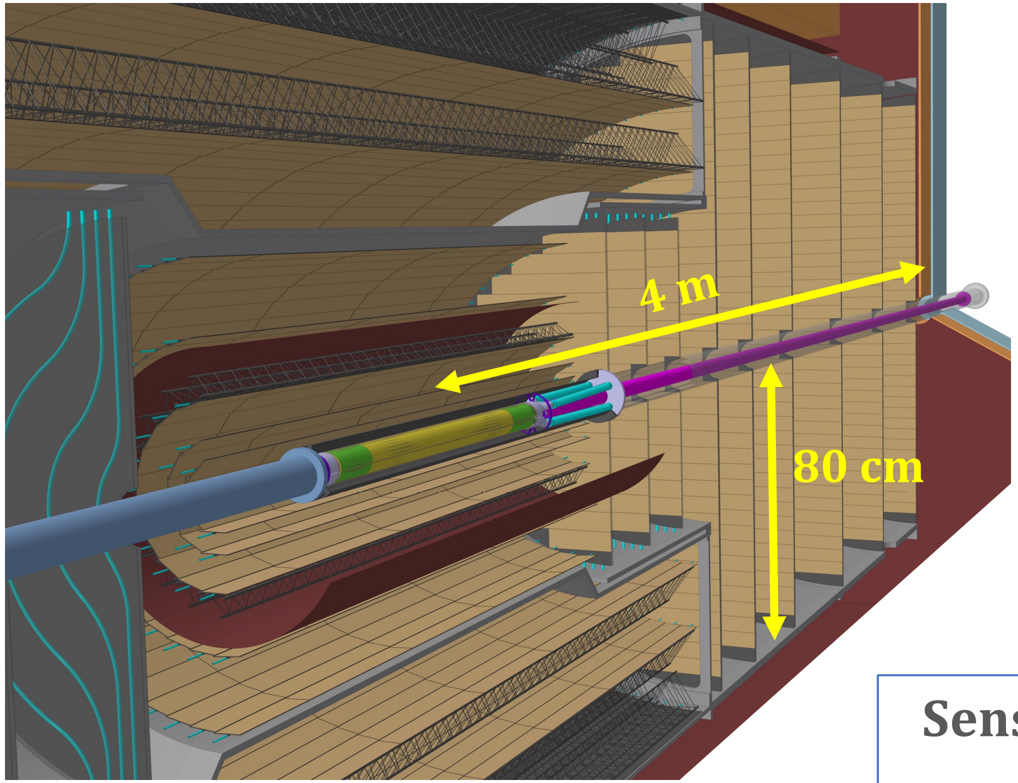
Sensor → Building on knowledge from ALICE ITS2 & ITS3



Retracted
R = 15 mm

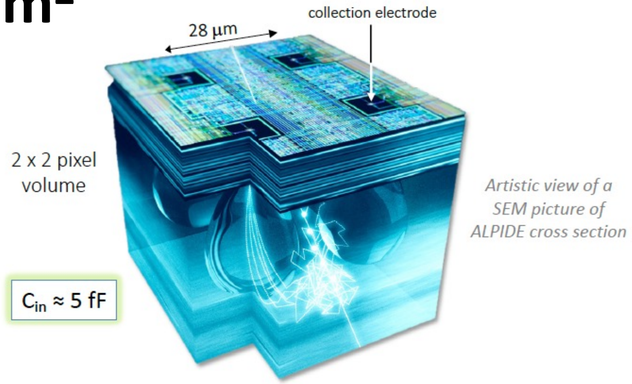
Data taking
R = 5 mm

Outer Tracker



- **60 m² MAPS**
- Large coverage: **$|\eta| \leq 4$**
- Compact: **$R_{out} \approx 80$ cm, $|z_{out}| \approx 4$ m**
- High-spatial resolution: **$\sigma_{pos} \approx 5\ \mu$m**
- Low material budget: **$X/X_0 < 10\%$ total**
- Low power: **~20 mW/cm²**

Sensor → Building on knowledge from ALICE ITS2 & ITS3



Artistic view of a SEM picture of ALPIDE cross section

R&D focuses on

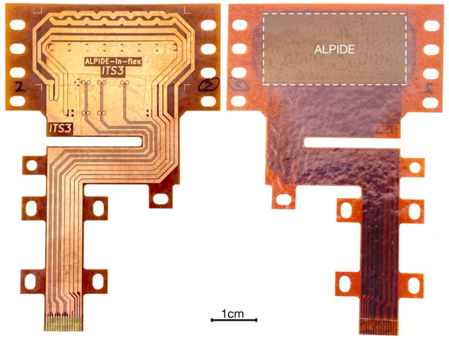
- **Module concept:** based on industry-standard processes for assembly & testing
- **Services:** reduce (eliminate) interdependency between modules (ability to replace single modules)

Summary

- MAPS provide low-mass, high-resolution options for many current & upcoming collider trackers
- **ALICE ITS2** & **sPHENIX MVTX** currently running and successfully taking data
- **ALICE ITS3** TDR in internal review → data taking expected in 2029
- **ePIC SVT** in final stages of R&D
  - MOSAIX wafer-scale, stitched for IB
  - EIC-LAS for OB, discs
- **ALICE 3** in early stages of R&D
  - Wafer-scale sensor for vertex tracker
  - Reticle size for rest of ~60 m^2 tracker
- **LBNL involvement in all of these projects** (RNC, Mech. Eng, IC design)

Outlook

- MAPS trackers are getting more complex & larger
- Sensor design can only do so much
  - Need dedicated R&D towards power, readout, mechanics, cooling in order to get all of the benefit from these low-material sensors
- New R&D planned for new/novel techniques
  - Kapton-embedded silicon
  - Corrugated carbon fiber
  - Carbon foam
  - CO2 cooling



- A lot that wasn't covered → MAPS w/fast timing for TOF, MAPS for FCC, etc.
- Exciting times ahead!